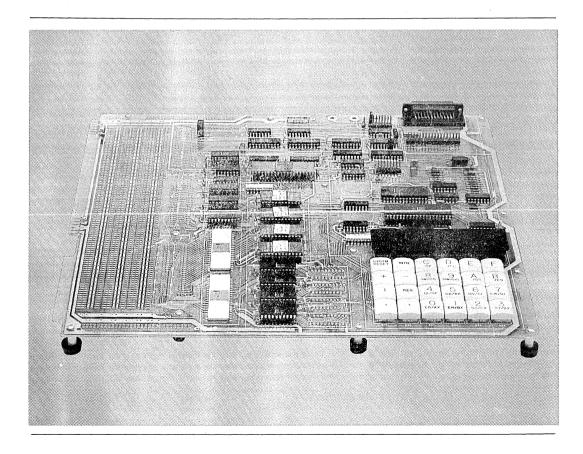


SDK-86 MCS-86™ SYSTEM DESIGN KIT

- Complete Single Board Microcomputer System Including CPU, Memory, and I/O
- Easy to Assemble Kit Form
- High Performance 8086 16-Bit CPU
- Interfaces Directly with TTY or CRT
- Interactive LED Display and Keyboard

- □ Wire Wrap Area for Custom Interfaces
- Extensive System Monitor Software in ROM
- Comprehensive Design Library Included

The SDK-86 MCS-86 System Design Kit is a complete single board 8086 microcomputer system in kit form. It contains all necessary components to complete construction of the kit, including LED display, keyboard, resistors, caps, crystal, and miscellaneous hardware. Included are preprogrammed ROMs containing a system monitor for general software utilities and system diagnostics. The complete kit includes an 8-digit LED display and a mnemonic 24-key keyboard for direct insertion, examination, and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal, CRT terminal, or the serial port of an Intellec system. The SDK-86 is a high performance prototype system with designed-in flexibility for simple interface to the user's application.



FUNCTIONAL DESCRIPTION

The SDK-86 is a complete MCS-86 microcomputer system on a single board, in kit form. It contains all necessary components to build a useful, functional system. Such items as resistors, caps, and sockets are included. Assembly time varies from 4 to 10 hours, depending on the skill of the user. The SDK-86 functional block diagram is shown in Figure 1.

8086 Processor

The SDK-86 is designed around Intel's 8086 microprocessor. The Intel 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor features attributes of both 8-bit and 16-bit microprocessors in that it addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance. Additional features of the 8086 include the following:

- Direct addressing capability to one megabyte of memory
- Assembly language compatibility with 8080/8085
- 14 word × 16-bit register set with symmetrical operations
- · 24 operand addressing modes
- · Bit, byte, word, and block operations
- 8 and 16-byte signed and unsigned arithmetic in binary or decimal mode, including multiply and divide
- 4 or 5 or 8 MHz clock rate

A block diagram of the 8086 microprocessor is shown in Figure 2.

System Monitor

A compact but powerful system monitor is supplied with the SDK-86 to provide general software utilities and system diagnostics. It comes in preprogrammed read only memories (ROMs).

Communications Interface

The SDK-86 communicates with the outside world through either the on-board light emitting diode (LED) display/keyboard combination or the user's TTY or CRT terminal (jumper selectable), or by means of a special mode in which an Intellec development system transports finished programs to and from the SDK-86. Memory may be easily expanded by simply soldering in additional devices in locations provided for this purpose. A large area of the board (22 square inches) is laid out as general purpose wire-wrap for the user's custom interfaces.

Assembly

Only a few simple tools are required for assembly: soldering iron, cutters, screwdriver, etc. The SDK-86 assembly manual contains step-by-step instructions for easy assembly with a minimum of mistakes. Once construction is complete, the user connects his kit to a power supply and the SDK-86 is ready to go. The monitor starts immediately upon power-on or reset.

Commands — Keyboard mode commands, serial port commands, and Intellec slave mode commands are summarized in Table 1, Table 2, and Table 3, respectively. The SDK-86 keyboard is shown in Figure 3.

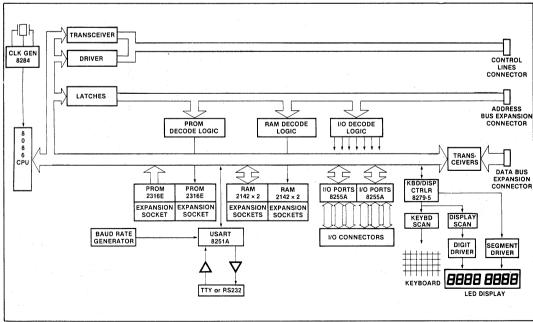


Figure 1. SDK-86 System Design Kit Functional Block Diagram

Documentation

In addition to detailed information on using the monitors, the SDK-86 user's manual provides circuit diagrams, a monitor listing, and a description of how the system works. The complete design library for the SDK-86 is shown in Figure 4 and listed in the specifications section under Reference Manuals.

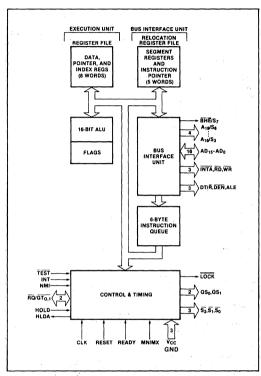


Figure 2. 8086 Microprocessor Block Diagram

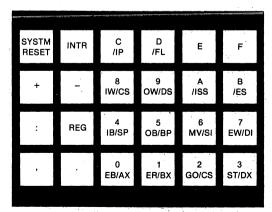


Figure 3. SDK-86 Keyboard

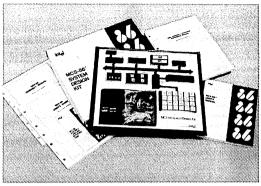


Figure 4. SDK-86 Design Library

Table 1. Keyboard Mode Commands

Command	Operation
Reset	Starts monitor.
Go	Allows user to execute user program, and causes it to halt at predetermined program stop. Useful for debugging.
Single step	Allows user to execute user program one instruction at a time. Useful for debugging.
Substitute memory	Allows user to examine and modify memory locations in byte or word mode.
Examine register	Allows user to examine and modify 8086 register contents.
Block move	Allows user to relocate pro- gram and data portions in memory.
Input or output	Allows direct control of SDK-86 I/O facilities in byte or mode.

Table 2. Serial Mode Commands

Command	Operation
Dump memory	Allows user to print or display large blocks of memory information in hex format than amount visible on terminal's CRT display.
Start/continue display	Allows user to display blocks of memory information larger than amount visible on terminal's CRT display.
Punch/read paper tape	Allows user to transmit fin- ished programs into and out of SDK-86 via TTY paper tape punch.

8086 INSTRUCTION SET

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able 4 contains a sed for the 8086 m	summary of processor instructions nicroprocessor.		in a few area and the first fire and the
	Table 4. 8086 Instru	ction Set Summary	•
Mnemonic and Description	Instruction Code	Mnemonic and Description	n eggin see, Instruction Code
Data Transfer	사람들은 사람들은 사람들이 되었다. 사람들은 사람들은 사람들은 사람들은 사람들이 되었다.		
10V = Meva:	78543210 78543210 78543210 78543210	CMP = Compare:	76543210 76543210 76543210 76543210
	100010d w mod reg r/m	Register/memory and register	0 0 1 1 1 0 d w mod reg r/m
	1.1 0.0 0.1 1 w moo 0.0 0 r/m data data if w-1	Immediate with register/memory	1 0 0 0 0 0 s w mod 1 1 1 r/m data data if s:w-01
nmediate to register demory to accumulator	1 0 1 0 0 0 0 w addr-low addr-high	Immediate with accumulator	0 0 1 1 1 1 0 w data data if w-1
ccumulator to memory	1 0 1 0 0 0 1 w addr-low addr-high	AAS=ASCII adjust for subtract DAS=Decimal adjust for subtract	00101111
egister/memory to segment register	1 0 0 0 1 1 1 0 mod 0 reg r/m	MUL=Multiply (unsigned)	1 1 1 1 0 1 1 w mod 1 0 0 r/m
egment register to register/memory	1 0 0 0 1 1 0 0 mod 0 reg r/m	IMUL=Integer multiply (signed)	1111011w mod101 r/m
USH = Push:	gazagas gatalija i jarang ali	AAM-ASCII adjust for multiply	11010100 00001010
	1 1 1 1 1 1 1 mod 1 1 0 r/m	BIV=Divide (unsigned)	1 1 1 1 0 1 1 w mod 1 1 0 r/m
legister	0 1 0 1 0 reg	IDIV-Integer divide (signed)	1 1 1 1 0 1 1 w mod 1 1 1 r/m
egment register	0 0 0 reg 1 1 0	AAD=ASCII adjust for divide	11010101 00001010
OP = Pop:	 And the second of the second of	CBW=Convert byte to word CW0=Convert word to double word	10011000
Register/memory	10001111 mod 000 r/m	SHE CONTENT HOLD TO DODDIE MOLD	
Register	0 1 0 1 1 1 reg	1.00	
egment register	0 0 0 reg 1 1 1		
		2.5 pt 10 =	A Charles to the transfer of the contract of t
CHG = Exchange:	(1000011 mlanting via)	Logic	
egister/memory with register	1 0 0 0 0 1 1 w mod reg r/m	NOT-Invert	1 1 1 1 0 1 1 w mod 0 1 0 r/m
register with accomplator	1001016	SHL/SAL=Shift logical/arithmetic left	1 1 0 1 0 0 v w mod 1 0 0 r/m
N = Input	The second secon	SHR-Shift logical right	1 1 0 1 0 0 v w mod 1 0 1 r/m
ixed port	1 1 1 0 0 1 0 w port	SAR=Shift arithmetic right	1 1 0 1 0 0 v w mod 1 1 1 r/m
ariable port	1110110w 1277 1277 1277 1277 1277	ROL-Rotate left ROR-Rotate right	1 1 0 1 0 0 v w mod 0 0 1 r/m
UT = Output		RCL-Rotate through carry flag left	1 1 0 1 0 0 v w mod 0 1 0 r/m
ixed port	1 1 1 0 0 1 1 w port	ACR=Rotate through carry right	110100v w mod 011 r/m
/ariable port	1110111w		
(LAT-Translate byte to AL	11010111	AND = And:	[Bod of a day [and are seen]
EA-Load EA to register	1 1 0 0 0 1 1 0 1 mod reg r/m	Reg./memory and register to either Immediate to register/memory	0 0 1 0 0 0 0 d w mod reg r/m
.DS=Load pointer to DS .ES=Load pointer to ES	1 1 0 0 0 1 0 0 mod reg r/m	Immediate to accumulator	0 0 1 0 0 1 0 w data data if w=1
AMF-Load AH with flags	10011111		
BANF - Store AH into flags	10011110	TEST = And function to flags, no resi	
PUBHF-Push flags	.1 0'0'1-1 1:0.01	Register/memory and register Immediate data and register/memory	1 0 0 0 0 1 0 w mod reg r/m
POPF=Pop flags	10011101	Immediate data and accumulator	1 0 1 0 1 0 0 w data data if w=1
A CALL DAMAGE ME	The state of the s		
The Landston Dis		OR = Or:	
		Reg./memory and register to either Immediate to register/memory	0 0 0 0 1 0 d w mod reg r/m
Arithmetic	Service Agents of Manager engineering	Immediate to register/memory	0 0 0 0 1 1 0 w data data if w=1
DD = Add:	The state of the s	tang ng tao ili	COUNTY CALL CALLS AND ASSESSMENT OF THE CALL CALLS AND ASSESSMENT OF THE CALL CALL CALL CALL CALL CALL CALL CAL
leg./memory with register to either. mmediate to register/memory	0 0 0 0 0 0 0 d w mod reg r/m 1 0 0 0 0 0 s w mod 0 0 0 r/m data data if s:w=01	XOR = Exclusive or:	
mmediate to register/memory mmediate to accumulator	1 0 0 0 0 0 0 s w mod 0 0 0 r/m data data if s:w=01	Reg./memory and register to either	0 0 1 1 0 0 0 w mod reg r/m 1 0 0 0 0 0 0 w mod 1 0 r/m data data if w=1
	Value 12 / Value 17 / Value	Immediate to register/memory Immediate to accumulator	1 0 0 0 0 0 0 w mod 1 1 0 r/m data data if w=1 0 0 1 1 0 1 0 w data data if w=1
IDC = Add with carry:		reviate to accumulator	Unit Un
	0 0 0 1 0 0 d w mod reg r/m		
mmediate to register/memory mmediate to accumulator	1 0 0 0 0 0 0 s w mod 0 1 0 r/m data data if s:w=01		
			그렇는 병이 뭐지 않는 지지 않는 그렇게 하면서
NC = Increment:		String Manipulation	그램 이번 그쪽 그렇는 범인 그는 그런 회원 학생이다.
Register/memory	1 1 1 1 1 1 1 w mod 0 0 0 r/m	REP-Repeat	1111001z
Register	0 1 0 0 0 reg	MOVS = Move byte/word	1:0,10010w
IAA-ASCII adjust for add	00110111	CMPS = Compare byte/word	1010011w
mn-vecimal aujust 10f 800	<u>provident in the contract of </u>	SCAS = Scan byte/word	1010111w
UB = Subtract:		LODS = Load byte/wd to AL/AX	
leg./memory and register to either	0 0 1 0 1 0 d w mod reg r/m	STOS = Stor byte/wd frm AL/A	eleka i a i a i a i a i a i a i a i a i a i
mmediate from register/memory	1 0 0 0 0 0 s w mod 1 0 1 r/m data data if s:w=01		그림 그 이 바다 보다는 경기를 받는다.
mmediate from accumulator	0 0 1 0 1 1 0 w data data if w-1	[일 10년 전 18 HES	민준이 나를 잃어나는 것이 하게 다른 것이다.
ニー・コンちばい かたさい ちょめいり	The second secon	Andrew Street	
BB - Subtract with borrow			그는데 그가 되지? 병원이 대원 중에 원리되었다. 일본 기회 위에
	0 0 0 1 1 0 d w mod reg r/m	Control Tennolos	
eg./memory and register to either nmediate from register/memory	1 0 0 0 0 0 s w mod 0 1 1 r/m data data if s:w=01	Control Transfer	그렇게 그는 그렇게 모든 사용하는 그 사건이 되었다.
eg./memory and register to either mmediate from register/memory		CALL = Call:	[1:171.0.1.0.0.0] disp-low disp-high
eg./memory and register to either mmediate from register/memory mmediate from accumulator	1 0 0 0 0 0 s w mod 0 1 1 r/m data data if s:w-01		1111 0 10 0 0 0 1 disp-low disp-high 1111 1 1 1 1 1 1 1 1 0 0 0 0 1 0 1 7 m
eg./memory and register to either mmediate from register/memory mmediate from accumulator DEC = Decrement:	1 0 0 0 0 0 s w mod 0 1 1 r/m data data if s:w=01	CALL = Call: Direct within segment Indirect within segment Direct intersegment	1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.
SBB - Subtract with borraw hep./memory and register to either mmediate from register/memory mmediate from accumulator DEC - Decrement: Register/memory Register/memory	1 0 0 0 0 0 0 s w mod 0 1 1 r/m data data if sw-01	CALL - Cell: Direct within segment Indirect within segment	1)11 1 1 1 1 1 mod 0 1 0 r/m

continued

SDK-86

Table 4. 8086 Instruction Set Summary (Continued)

Mnemonic and Description	Instruction Co	de	Mnemonic and Description	Instruction Code
JMP - Unconditional Jump:	78543210 78543210 7854	13210		78543210 78543210
Direct within segment		sp-high	JMS: Jump on not sign	0 1 1 1 1 0 0 1 , disp
Direct within segment-short	1 1 1 0 1 0 1 1 disp		LOOP Loop CX times	[11100010] disp
	1111111 mod 100 r/m		LOOPZ/LOOPE - Loop while zero/equal	1 1 1 0 0 0 0 1 disp
Direct intersegment		set-high .	LOOPNZ/LOOPNE Loop while not zero/equal	1 1 1 0 0 0 0 0 disp
		g-high	JCXZ-Jump on CX zero	1 1 1 0 0 0 1 1 disp
Indirect intersegment	1 1 1 1 1 1 1 1 mod 1 0 1 r/m		* * * * * * * * * * * * * * * * * * *	
RET = Return from CALL:				
Within segment	11000011		INT Interrupt	·
		ita-high	Type specified	1 1 0 0 1 1 0 1 type
	11001011		Туре 3	11001100
	1 1 0 0 1 0 1 0 data-low da	ita-high	INTO: Interrupt on overflow	11001110
JE/JZ-Jump on equal/zero	0-1, 1.1.0 1 0 0 disp		IRET Interrupt return	11001111
If / INCE - humo on lace (not greater	0 1 1 1 1 1 0 0 disp	THE SHAPE SHOW I		
JLE/JME-Jump on less or equal/not	0 1 1 1 1 1 1 0 disp			
greater	0'1110010 disp	A path aware	Decease Control	
or equal JBE/JMA-Jump on below or equal/ not above	0 1 1 1 0 1 1 0 disp		Processor Control	,
not above JP/JPE=Jump on parity/parity even	0 1 1 1 0 1 0 disp	ļ	CLC Clear carry	11111000
;			CMC Complement carry	11110101
·		Griff y 1, 19 a	STC Set carry	11111001
	0 1 1 1 1 0 0 0 disp		CLO Clear direction	1111100
 JNL/JGE-Jump on not less/greater: i 	0 1 1 1 0 1 0 1 disp	10 Jan 19 19 19 19 19 19 19 19 19 19 19 19 19	STO: Set direction	11111101
or equal	0 1 1 1 1 1 0 1 disp		CLI Clear interrupt	11111010
greater	0 1 1 1 1 1 1 disp	26 27 28 24 2	STI Set interrupt	11111011
	0.1 1 1 0 0 1 1 disp	Sec. 25 (1994)	HLT Hall	11110100
JMBE/JA-Jump on not below or equal/above	0 1 1 1 0 1 1 1 disp	2010 000000	WAIT Wait	10011011
- JNP/JPO-Jump on not par/par odd	0 1 1 1 1 0 1 1 disp	Jedan Cat	ESC Escape (to external device)	1 1 0 1 1 x x x mod x x x r/m .
JNO-Jump on not overflow	0 1 1 1 0 0 0 1 disp	200	LOCK Bus lock prefix	11110000
	9 4 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -			
Notes				am a marin sanat ili a kis imi
AL = 8-bit accumulator		to the transfer of the terminal	if s:w = 01 then 16 bits of imme	ediate data form the operand.
AX = 16-bit accumulator			if s:w = 11 then an immediate of	data byte is sign extended to
CX = Count register DS = Data segment		4 9 9 9	form the 16-bit operand.	
ES = Extra segment			if v = 0 then "count" = 1; if v :	= 0 then "count" in (CL)
Above/below refers to unsigned	d value.	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	x = don't care.	
Greater = more positive; Less = less positive (more nega	and a second control of the second	and the second	if v = 0 then "count" = 1; if v :	- 1 then "count" in (CL) register
			z is used for string primitives for	
if d = 1 then "to" reg; if d = 0 then if w = 1 then word instruction; if	n "from" reg		F 1	
if w = 1 then word instruction; i	n "from" reg		SEGMENT OVERRIDE PREFIX	
	n "from" reg		F 1	
. if w = 1 then word instruction; i	n "from" reg if w = 0 then byte instruction		SEGMENT OVERRIDE PREFIX	or comparison with ZF FLAG.
<pre>if w = 1 then word instruction; i if mod = 11 then r/m is treated</pre>	n "trom" reg if w = 0 then byte instruction		SEGMENT OVERRIDE PREFIX 001 reg 110 REG is assigned according to t	or comparison with ZF FLAG. the following table:
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0*, disp	n 'trom'' reg if w = 0 then byte instruction	absent	SEGMENT OVERRIDE PREFIX 001 reg 110 REG is assigned according to t 16-Bit (w = 1)	or comparison with ZF FLAG. the following table: 8-Bit (w = 0) Sagmant
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-lov	n "trom" reg if w = 0 then byte instruction as a REG field I-low and disp-high are absent w sign-extended to 16-bits, disp-high is	absent	SEGMENT OVERRIDE PREFIX 0.0.1 reg. 1.1.0 REG is assigned according to t 16-Bit (w = 1) 000 AX	or comparison with ZF FLAG. the following table: 8-Bit (w = 0)
if w = 1 then word instruction; if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-hig if mod = 10 then DISP = disp-hig	n 'trom'' reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is ht disp-low	absent	SEGMENT OVERRIDE PREFIX 0.0.1 reg 1.1.0 REG is assigned according to the second of t	or comparison with ZF FLAG. the following table: 8-Bit (w - 0) Segment
if w = 1 then word instruction; if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-low if mod = 10 then DISP = disp-light if r/m = 000 then EA = (BX) + (S	n 'trom'' reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is bit, disp-low ii) + DISP	absent	REG is assigned according to to the state of	the following table: B-Bit (w 0) Sagmant
if w = 1 then word instruction; if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-hig if r/m = 000 then EA = (BX) + (BX) + (BX) = (BX) +	n 'trom' 'reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is bit, disp-low 5) - DISP 1) - DISP 1) - DISP	absent	SEGMENT OVERRIDE PREFIX 0 0 1 reg 1 1 0 REG is assigned according to the second of t	the following table: 8-BIT (w = 0) Segment
if w = 1 then word instruction; if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-low if mod = 10 then DISP = disp-light if r/m = 000 then EA = (BX) + (S	n "trom" reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is h: disp-low 3) - DISP 1) - DISP 1) - DISP	absent	REG is assigned according to to the state of	the following table: B-Bit (w 0) Sagmant
if w = 1 then word instruction; if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-loy if mod = 10 then DISP = disp-loy if r/m = 000 then EA = (BX) + (0 if r/m = 001 then EA = (BX) + (0 if r/m = 010 then EA = (BP) + (0 if r/m = 010 then EA = (BP) + (0 if r/m = 011 then EA = (BP) + (0 if	n "trom" reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is ph; disp-low 3) + DISP 4) + DISP	absent	SEGMENT OVERRIDE PREFIX 0 0 1 reg 1 1 0 REG is assigned according to t 18-Bit (w = 1) 000 AX 001 CX 010 DX 011 BX 100 SP 101 BP	the following table: 8-Bit (w 0) Segment
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, dispinit mod = 01 then DISP = disp-loi if mod = 01 then DISP = disp-loi if r/m = 000 then EA = (BX) + (S if r/m = 001 then EA = (BY) + (S if r/m = 001 then EA = (BP) + (S	n "from" reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is jh: disp-low ii) + DISP ii) + DISP ii) + DISP II) + DISP SP	absent	REG is assigned according to t 18-Bit w = 1)	the following table: 8-Bit (w - 0) Segment
if w = 1 then word instruction; i if mod = 11 then r/m is treated if mod = 00 then DISP = 0° disp- if mod = 01 then DISP = disp- if mod = 10 then DISP = disp- if r/m = 000 then EA = (BX) + (n "trom" reg if w = 0 then byte instruction as a REG field -low and disp-high are absent w sign-extended to 16-bits, disp-high is ph: disp-low ii) - DISP ii) - DISP ii) - DISP SP SP SP SP	absent	REG is assigned according to t 18-Bit (w = 1)	the following table: 8-Bit (w 0) Sagment 000 AL 00 ES 001 CL 01 CS 010 DL 10 SS 011 BL 11 DS 100 AH 11 DS 110 DH 111 BH
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = 0'gisp-loy if mod = 01 then DISP = 0 disp-loy if mod = 10 then EA = (BX) + (0 if r/m = 001 then EA = (BX) + (0 if r/m = 010 then EA = (BP) + (0 if r/m = 010 then EA = (BP) + (0 if r/m = 101 then EA = (BP) + (0 if r/m = 101 then EA = (BP) + (0 if r/m = 101 then EA = (BP) + (0 if r/m = 111 then EA = (BP) + (0 if r/m = 111 then EA = (BP) + (0 if r/m = 111 then EA = (BX) + 0 if r/m = 111 then EA = (BX) + 0 if r/m = 111 then EA = (BX) + 0 if r/m = 110 th	n "trom" reg if w = 0 then byte instruction as a REG field allow and disp-high are absent w sign-extended to 16-bits, disp-high is bit disp-low ii) + DISP ii) + DISP iii) + DISP SP SP SP SP	absent	REG is assigned according to t 18-Bit (w = 1)	the following table: 8-Bit (w - 0) Segment
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0* disp if mod = 01 then DISP = disp-hig if mod = 10 then DISP = disp-hig if r/m = 000 then EA = (BX) + (0 if r/m = 001 then EA = (BY) + (0 if r/m = 010 then EA = (BP) + (0 if r/m = 101 then EA = (BP) + (0 if r/m = 101 then EA = (CF) + (0 if	n "trom" reg if w = 0 then byte instruction as a REG field allow and disp-high are absent w sign-extended to 16-bits, disp-high is bit disp-low ii) + DISP ii) + DISP iii) + DISP SP SP SP SP	absent	REG is assigned according to to 18-Bit (w - 1) 000 AX 001 CX 010 DX 101 BX 100 SP 110 SI 111 DI Instructions which reference the represent the file:	the following table: 8
if w = 1 then word instruction; if mod = 11 then r/m is treated if mod = 00 then DISP = 0°, disp if mod = 01 then DISP = disp-loy if mod = 10 then DISP = disp-loy if mod = 10 then DISP = disp-loy if r/m = 000 then EA = (BX) + (B) if r/m = 001 then EA = (BP) + (B) if r/m = 01 then EA = (BP) + (B) if r/m = 01 then EA = (BP) + (B) if r/m = 100 then EA = (SI) - 01 if r/m = 110 then EA = (BP) = 01 if r/m = 111 then EA = (BX) + 01 DISP follows 2nd byte of instructions:	n "trom" reg if w = 0 then byte instruction as a REG field allow and disp-high are absent w sign-extended to 16-bits, disp-high is bit disp-low ii) + DISP ii) + DISP iii) + DISP SP SP SP SP	absent	REG is assigned according to to 18-Bit (w - 1) 000 AX 001 CX 010 DX 101 BX 100 SP 110 SI 111 DI Instructions which reference the represent the file:	the following table: 8-Bit (w 0) Sagment 000 AL 00 ES 001 CL 01 CS 010 DL 10 SS 011 BL 11 DS 100 AH 11 DS 110 DH 111 BH

SPECIFICATIONS

Central Processor

CPU - 8086 (5 MHz clock rate)

Note

May be operated at 2.5 MHz or 5 MHz, jumper selectable, for use with $8086. \,$

Memory

ROM - 8K bytes 2316/2716

RAM — 2K bytes (expandable to 4K bytes) 2142

Addressing

ROM - FE000-FFFFF

RAM — 0-7FF (800-FFF available with additional 2142's)

lote

The wire-wrap area of the SDK-86 PC board may be used for additional custom memory expansion.

input/Output

Parallel - 48 lines (two 8255A's)

Serial - RS232 or current loop (8251A)

Baud Rate - selectable from 110 to 4800 baud

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Serial I/O — 20 mA current loop TTY or RS232

Note

The user has access to all bus signals which enable him to design custom system expansions into the kit's wire-wrap area.

Interrupts (256 vectored)

Maskable Non-maskable TRAP

DMA

Hold Request — Jumper selectable. TTL compatible input.

Software

System Monitor — Preprogrammed 2716 or 2316 ROMs Addresses — FE000-FFFFF

Monitor I/O — Keyboard/display or TTY or CRT (serial I/O)

Physical Characteristics

Width — 13.5 in. (34.3 cm)

Height - 12 in. (30.5 cm)

Depth — 1.75 in. (4.45 cm)

Weight - approx. 24 oz. (3.3 kg)

Electrical Characteristics

DC Power Requirement

(Power supply not included in kit)

Voltage	Current
V _{CC} 5V ± 5%	3.5A
$V_{TTY} - 12V \pm 10\%$	0.3A
	(VTTY required only if teletype is connected)

Environmental Characteristics

Operating Temperature - 0-50°C

Reference Manuals

9800697A — SDK-86 MCS-86 System Design Kit Assembly Manual

9800722 - MCS-86 User's Manual

9800640A — 8086 Assembly Language Programming Manual

8086 Assembly Language Reference Card

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number De

Description

SDK-86

MCS-86 system design kit

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