

**PC-Chips**

**M915i**

**MANUAL**

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## **M915i - DX9200 BIOS SETUP**

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### **SYSTEM BIOS SETUP**

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Due to frequent update of system BIOS, the actual options available in your system board BIOS setups may vary comparing with this manual. If technically necessary, we would provide a special insert for instruction of the difference in regard to any changes of the BIOS setup option.

### **LOAD SETUP DEFAULTS**

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There is a set of BIOS values stored in the ROM files:

#### *The "Bios" default values*

The "BIOS" default values are those which should provide optimum performance for the system. They are the best case default values.

#### *The "Setup" default values*

The "Setup" default values are the most conservative default settings but are also the most stable default values for the system. They are to be used if the system is performing erratically because of hardware problems.

### **STANDARD CMOS SETUP OPTIONS**

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#### *Date and Time Options*

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If you would like to set your date and time options, move your cursor to highlight the specific items and use PgUp/PgDn to modify the values.

#### *Primary Master & Slave, Secondary Master & Slave Drive Types*

According to your actual equipment, you can select the type of hard

disks for C, D, E, & F from 'Not Installed' to type 46 for standard hard disks. As for type 47, user may define by himself. If a ATAPI IDE CD-ROM is connected to any on-board IDE port, the HARD DISKS "Type" should be set to "None". The DOS CD-ROM driver or the Win95 built-in driver will handle the communication by themselves. You may also use the "IDE HDD Auto Detection" option in the Main Menu to allow the system to detect and enter these information for you.

#### *Floppy Drives A & B*

Sets your floppy drive type.

#### *Video*

Set your video type and if set to not installed, the system will ignore the primary display while doing the POST test.

#### *Halt On*

This option determines whether the system will stop if an specified error in this option is detected during power up

### **BIOS FEATURES SETUP**

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#### *Virus Warning*

This function, If enabled, will detects boot sector viruses and warning will be given when a program attempted to change boot sector information.

#### *CPU Internal & External Cache*

These options allows user to enable or disable the on-board (External) and the on-chip (CPU Internal) cache memories (SRAM) when special peripheral or software implemented indicate such requirement.

#### *Quick Power On Self Test*

This option speeds up the POST by shortening and skipping some test items during POST.

#### *Boot Sequence*

The system maybe set to seek the operating system during power up either from the floppy drive A: or from the hard drive C: by using this option.

#### *Swap Floppy Drive*

Floppy A: and B: will be swapped under DOS. For example, if the original definition of the floppy A: is 1.2M 5.25" and the B: is 144M 3.5", they will be swapped when this option is enabled.

### *IDE HDD Block Mode, 32-bit Transfer & PIO Mode 3 Support*

All three of these options, if enabled with the use of the on-board IDE controller will enhance you hard drive performance. Most new hard drives should support these functions, so be sure to check with you hard drive manufacturer before using this option.

### *Gate A20 Option*

Use the "Fast" option whenever possible, since it will enable the Fast Gate A20 and the fast reset for protected mode operation.

### *Security Option*

This option allow a password be set up so that a password will be needed to enter the CMOS Setup or to boot the system including entering CMOS Setup. After this option is enabled, you must use the "Password Setting" option in the main menu to setup your password. If in any case the password is lost or forgotten, the jumper JP 5A - Clear CMOS can be used to clear the configuration.

### *IDE Second Channel Control*

This option, in combination with the "PCI IDE Controller" option in the "PCI/Green Functions Setup" would enable the second onboard IDE channel (Drive E: & F:) or the BIOS will attempt to control the external second IDE port, if a external dual IDE controller card is installed.

### *System, Video & Adapter ROM Shadows*

Video and/or adaptor ROM shadowing is a procedure in which BIOS codes from your peripheral adapter's ROM are copied from slower ROM to faster RAM and executed from there. Each option allows for a segment of 8 KB to be shadowed from ROM to RAM. If one of these options is enabled and there is BIOS present in that particular 8 KB segment, then the BIOS will be shadowed.

## **CHIPSET FEATURES SETUP**

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*Most of the options in this group have major influence to the system. If options are not set properly, it may not only the performance will be greatly affected, but also it may bring the system down unexpectedly in most cases. Therefore, it is only wise to leave the defaults alone unless there are specific reason to do any change.*

### *Auto Configuration, and AT Bus Clock*

The Auto Configuration option should be always enabled for the system to automatically configure the AT bus clock to AT standard by detecting the system clock rate.

### *System & Video BIOS Cacheable*

The system and video BIOS shadows can be cached into external cache memory for improved performance.

### *L1 Cache Update Scheme*

This option would enable the CPU internal cache to use Write-Through or Write-Back schemes. The DX & DX2 CPUs from Cyrix and its compatibles support L1 Write-Back cache in comparison to the DX, DX2 & DX4 CPUs from Intel and its compatibles supporting only Write-Through cache.

It is very important to properly set this option according to the CPU installed. Do not turn on the L1 Write-Back cache if the CPU installed does not support this feature or the system will fail.

### *L2 Cache Update Scheme*

This option allows the external cache scheme to be changed to suit a particular application.

## **POWER MANAGEMENT SETUP**

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### *Power Management*

This option served as a master switch to turn-on the power management.

### *PM Control By APM*

APM function allows applications that use the Advanced Power Management interface to control the system's power management features.

### *Video Off Method*

If the Graphic Controller installed is VESA compliant, then you may want to use the V/H Syn+Blk option. Otherwise set the option to Blank Screen

### *HDD Standby Timer*

The HDD Standby Timer supports hard drives that have such a feature. However, if this option is enabled and you experience erratic hard drive behavior, this option must be disabled. This option uses the SMM/SMI specification for hard drive power saving control.

### *Doze, Standby, and Suspend Modes*

Defined the length of time of continuous inactivity before the system enters into different PM modes. The Suspend Mode is not implemented.

### *Mode Control*

The options under this category allow you to specify the system clock speeds at different power saving modes. The video can also be set to on or off at different modes by this option.

### *Monitor Event In Full On Mode*

These options allow you to specify what activities the system should monitor which will prevent the system from entering the power saving modes when activity is detected as defined in here.

### **PCI/Green Function Setup**

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#### *Slot 1 - 4 Using Int#*

Using Auto settings will work with most controllers. However, you may manually assign INT A - D to the 4 different slots according to the controller setting in that slot.

#### *1st- 4th Available IRQ*

These options tell the system which system's IRQ should be used first if any controller installed should need an IRQ. If an IDE HDD is installed, you may want to set the 1st Available IRQ to 14 since IDE HDD using IRQ14 is the de facto industry standard.

#### *PCI IRQ Activated By*

The "Level" setting should work most of the time, and it is the PCI standard. It may need to be set as "Edge" when the IDE controller requires to use a legacy connector or any other kind of direct hardware IRQ assignment scheme such as using the on-board JP1.

#### *PCI IDE Controller*

This option is the master switch to turn on the on-board dual channel IDE controller. If any IDE devices are installed on the connectors J17 and/or J18, this option has to be enabled after the "standard CMOS Setup" is properly configured. If the second IDE port (J17) is also being used, the "IDE Second Channel Control" in the "BIOS Features Setup" will be enabled. Disable this option when an add-on IDE controller is installed. In this case, the following option "PCI IDE IRQ Map To" will appear and it has to be configured in addition to the "1st - 4th Available IRQ" options.

#### *PCI IDE IRQ Map To*

Use "PCI-Auto" and it should work with most PCI IDE controllers or you may specifically inform the system which physical slot the IDE controller is inserted. If an ISA controller is inserted in one of the ISA slots, set the option to "ISA"; or if the PCI IDE controller requires to

use a legacy connector or any other kind of direct hardware IRQ assignment scheme, then the option should be set to "ISA."

#### *Wakeup Event In Inactive Mode*

These options allow you to specify what activities the system should monitor which will wake-up the system from power saving modes when activity is detected as defined in here.

#### **EXITING SETUP UTILITY**

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At this point, you can either choose to confirm your setup entries and exit by using "ESC" key and taking the "Save & Exit Setup" or the "Exit Without Saving" option to restore the original setup parameters and exit. After you highlight the desired option and press <<ENTER>>, the system will reset itself. The new or original setup parameters, depend on the option which you have chosen, will become the current setting.

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## **DX9200 JUMPER SETTINGS**

[JP3 - External Battery Connector/Clear CMOS](#)

[JP4 - Peripheral Power Control Connector](#)

[JP6 JP7 & JP8 - CPU Clock Selection Jumper](#)

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[JP41 - CPU Cooling Fan Power Connector](#)

[JP21 JP22 JP23 JP24 & JP42 - CPU Voltage Selector](#)

[CPU Type Selection Jumper](#)

**JP3 - External Battery Connector/Clear CMOS**

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=====

Jumper	Pin	Assignment
-----		
2 - 3		Normal Operation
3 - 4		Clear CMOS
	1	External Battery (+)
	4	External Battery (-)

=====

Please make sure the pins 2-3 are shorted before using the system board. The systemboard is shipped from the factory with pins 3-4 shorted to prevent battery drain during storage. Failure to reset this jumper at pins 2-3 would prevent the board from powering up.

**JP4 - Peripheral Power Control Connector**

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=====

Pin	Assignment
-----	
1	LED (+)
2	LED (-)

=====

**JP14 - Turbo Switch**

[TOP](#)

=====

Jumper	State
--------	-------



```

-----
OPEN      Turbo
1 - 2     Non-Turbo
=====

```

### JP15 - System Reset

[TOP](#)

```

=====
Pin    Assignment
-----

```

```

-----
1      Reset
2      Ground
=====

```

### JP16 - Green Mode Trigger Switch

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```

=====
Jumper  State
-----

```

```

-----
Trigger Once  Green Mode
Trigger Again Normal Operation
=====

```

This is a toggle switch so please do not keep this jumper shorted or else the system will have a problem waking up or booting after a reset. For this reason, do not use the Turbo button on the system chassis for this switch, since one may forget to release the button after triggering the system into green mode.

### JP18 - Keylock & Power LED

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```

=====
Pin    Assignment
-----

```

```

-----
1      LED Power
2      Not Connected
3      Ground
4      Keyboard Lock
5      Ground
=====

```

### JP19 - Speaker

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```

=====
Pin    Assignment

```

```

-----
1      Speaker Data Out
4      +5V
=====

```

#### JP20 - Turbo LED

[TOP](#)

```

=====
Pin   Assignment
-----

```

```

-----
1      LED (+)
2      LED (-)
=====

```

#### JP40 - On-Board IDE HDD LED

[TOP](#)

```

=====
Pin   Assignment
-----

```

```

-----
1      LED (+)
2      LED (-)
=====

```

#### JP41 - CPU Cooling Fan Power Connector

[TOP](#)

```

=====
Pin   Assignment
-----

```

```

-----
1      + 12V
2      Ground
3      Ground
4      + 5V
=====

```

#### JP6 JP7 & JP8 - CPU Clock Selection Jumper

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```

=====
CPU Clock  CPU Frequency   JP6    JP7    JP8
-----

```

```

-----
25MHz   DX2-50MHz   OPEN    OPEN    SHORT
33MHz   DX/SX-33MHz SHORT    SHORT    SHORT

```

DX2-66MHz  
 DX4-100MHz  
 40MHz DX-40MHz OPEN SHORT SHORT  
 DX2-80MHz

### JP(21-24) & JP42 - CPU Voltage Jumpers

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#### Voltage JP21 JP22 JP23 JP24 JP42

```

-----
5 Volts  2 - 3  2 - 3  2 - 3  2 - 3  OPEN
4 Volts  1 - 2  1 - 2  1 - 2  1 - 2  OPEN
3.3 Volts 1 - 2  1 - 2  1 - 2  1 - 2  SHORT
=====
  
```

### CPU Type Selection Jumper

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```

=====
|         486 NON-SL ENHANCED ||         486 SL ENHANCED |
|-----INTEL/AMD-----|----AMD----||-----INTEL-----|----CYRIX--
--|
|   SX   |   DX   |   DX4   ||   SX   |   DX, DX2 |   DX, DX2 |
|   DX2-66/80 |   DX4   ||   DX4   |   DX4   |   DX2-V80 |
=====
  
```

```

-----
JP25  2 - 3      1 - 2      1 - 2      2 - 3      1 - 2      1 - 2
      3 - 4      3 - 4
JP26  OPEN      3 - 4      3 - 4      OPEN      3 - 4      3 - 4
JP27  OPEN      OPEN      OPEN      1 - 2      1 - 2      1 - 2
JP28  OPEN      OPEN      OPEN      OPEN      OPEN      2 - 3
JP29  2 - 3      2 - 3      2 - 3      1 - 2      1 - 2      1 - 2
JP30  OPEN      OPEN      OPEN      1 - 2      1 - 2      2 - 3
JP31  OPEN      OPEN      OPEN      OPEN      OPEN      2 - 3
JP32  OPEN      OPEN      OPEN      2 - 3      2 - 3      1 - 2
      4 - 5      4 - 5      3 - 4
JP33  SHORT     SHORT     OPEN      OPEN      OPEN      OPEN
JP34  OPEN      OPEN      OPEN      OPEN      OPEN      OPEN
JP35  OPEN      OPEN      OPEN      OPEN      OPEN      1 - 2
JP36  2 - 3      2 - 3      1 - 2      2 - 3      2 - 3      OPEN
JP37  1 - 2      1 - 2      1 - 2      1 - 2      1 - 2      1 - 2
JP38  1 - 2      1 - 2      1 - 2      1 - 2      1 - 2      2 - 3
=====
  
```

The jumper settings for the AMD 5x86 133 are:

```

JP25  1-2, 3-4
JP26  3-4
JP27  1-2, 3-4
JP28  3-4
JP29  1-2
JP30  1-2, 3-4
JP31  OPEN
JP32  2-3, 4-5
JP33  OPEN
  
```

JP34 SHORT  
JP35 OPEN  
JP36 2-3 (1-2 FOR DX4 100/120)  
JP37 1-2  
JP38 1-2

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## **M915i - DX9200 MEMORY SETTINGS**

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### **THE CACHE MEMORY**

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This system board can support an optional 64KB, 128KB, 256KB, 512KB or 1MB external write back, direct-mapped cache.

### **SOME CACHE MEMORY CONSIDERATIONS**

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Since single bank cache installations (B, D, F) prevent the cache sub-system from using interleaving access, the "Auto Configuration" in the Advanced Chipset Setup must be disabled and the "Cache Read Wait State" must also be set to "3-2-2-2" to ensure proper operation.

### **CACHE MEMORY CONFIGURATIONS**

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=====

Type	Total Cache	Bank 0 (U33-36)	Bank 1 (U25-28)	TAG Ram (U32)	Pieces
A	64K	8K x 8	8K x 8	8K X 8	9
B	128K	32K x 8		8K X 8	5
C	256K	32K x 8	32K x 8	32K X 8	9
D	256K	64K x 8		32K X 8	5
E	512K	64K x 8	64K x 8	32K X 8	9
F	512K	128K x 8		32K X 8	5
G	1024K	128K x 8	128K X 8	64K X 8	9

=====

### **CACHE MEMORY JUMPER CONFIGURATIONS**

[TOP](#)

=====

TYPE	CACHE	JUMPER JP9	JP10	JP11	JP12	JP13
------	-------	------------	------	------	------	------

=====

```

-----
A   64K      OPEN      OPEN  OPEN  OPEN  OPEN
B   128K     1 - 2, 3 - 4    OPEN  OPEN  OPEN  SHORT
C   256K     2 - 3, 4 - 5    OPEN  OPEN  SHORT SHORT
D   256K     1 - 2, 3 - 4, 5 - 6  OPEN  OPEN  SHORT SHORT
E   512K     2 - 3, 4 - 5, 6 - 7  OPEN  SHORT SHORT SHORT
F   512K     1 - 2, 3 - 4, 5 - 6, 7 - 8  OPEN  SHORT SHORT SHORT
G   1024K    2 - 3, 4 - 5, 6 - 7, 8 - 9  SHORT SHORT SHORT SHORT
=====

```

## THE MAIN MEMORY

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There are 4 banks of 72 pin SIMM sockets on this board with each bank of 72 pin SIMM consisting of only one SIMM socket. The system board has auto-detection circuitry to sense which bank or banks are filled. Fill any SIMM module in the configurations listed below with Fast Page Mode, single or double sided memory.

## SOME MAIN MEMORY CONSIDERATIONS

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 Maximum memory on-board can not exceed 256 MB in any combination.

The memory installed in banks 0 & 1 must be more than or equal to the memory installed in banks 2 & 3.

If both of the SIMM sockets in any single group (i.e. banks 0 & 1) are filled then both of the SIMM modules must be of the same type.

Moreover, you do not have to fill up a single group with SIMM modules before starting on the next. See below for more clarification on these considerations.

## POSSIBLE MAIN MEMORY CONFIGURATIONS

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```

=====
|-----GROUP 1-----| |-----GROUP 2-----|
--|
#   BANK 0      BANK 1      BANK 2      BANK 3
-----
1   256KB-16MB  NONE        NONE        NONE
2   NONE        256KB-16MB  NONE        NONE
3   NONE        NONE        256KB-16MB  NONE
4   NONE        NONE        NONE        256KB-16MB
5   256KB-16MB  256KB-16MB  NONE        NONE
6   256KB-16MB  NONE        256KB-16MB  NONE
7   256KB-16MB  NONE        NONE        256KB-16MB
8   NONE        256KB-16MB  256KB-16MB  NONE

```

9	NONE	256KB-16MB	NONE	256KB-16MB
10	NONE	NONE	256KB-16MB	256KB-16MB
11	256KB-16MB	256KB-16MB	256KB-16MB	NONE
12	NONE	256KB-16MB	256KB-16MB	256KB-16MB
13	256KB-16MB	256KB-16MB	NONE	256KB-16MB
14	256KB-16MB	NONE	256KB-16MB	256KB-16MB
15	256KB-16MB	256KB-16MB	256KB-16MB	256KB-16MB

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