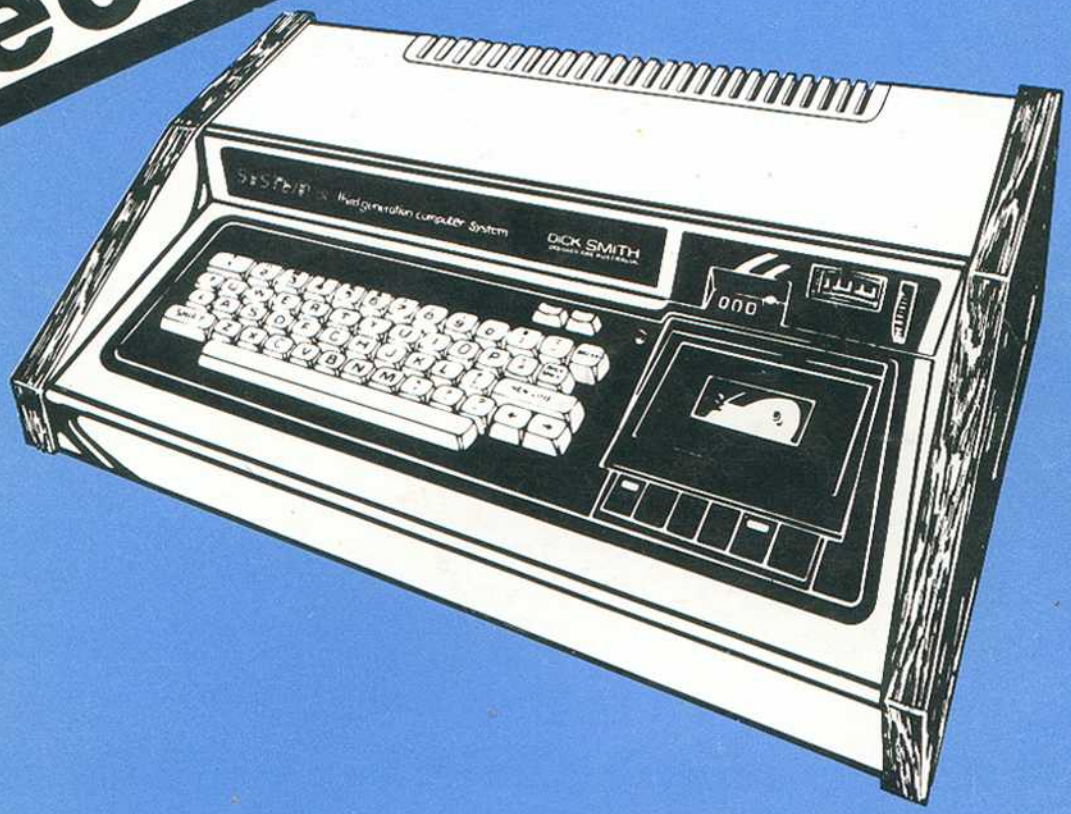
DICK SMITH SYSTEM 80 Technical Manual



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DICK SMITH

SYSTEM 80

Technical Manual

Preface

This manual is intended to provide owners of the Dick Smith System 80 with additional information to assist the understanding of operation and to facilitate easy repair should this be necessary.

In this manual, the operation inside each functional block is described. Troubleshooting flowcharts are provided, however, these flowcharts should be treated as guides rather than rules.

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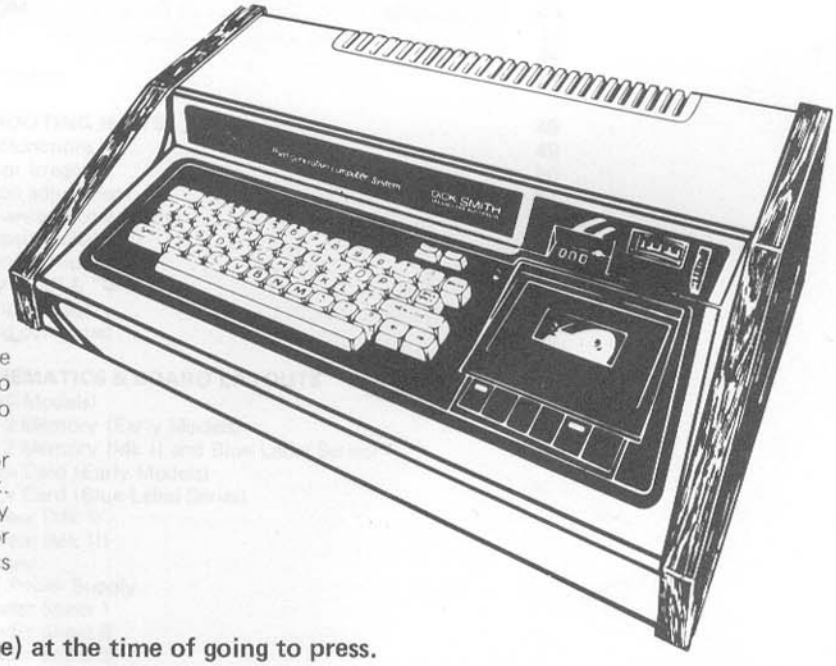


(All details are correct (to our knowledge) at the time of going to press.

Data compiled by Dick Smith Service Department in conjunction with EACA International.

We gratefully acknolwedge the assistance of EACA International in the production of this manual.

Introduction

This manual has been re-typed in its entirety. The font and layout has been standardized as has the paragraph formatting and numbering. The Diagrams have been reduced in size to a standard A4 sheet even though the original text has been retained and states that they are in a large fold out format.

Some grammatical corrections have been made where the meaning of what was being imparted was obvious. Where the issue was cloudier the original text was left unaltered to prevent further confusion over its intention. Because of variations in font and layout in the original a minor reduction of the number of pages has occurred. It was considered that preserving the original numbering sequence would serve no useful purpose as this was not intended to be a carbon copy of the original.

The schematics and printed circuit board layouts have been interspersed with blank pages. This was to avoid the problem of orientation of the pages that would be printed on the reverse sides. The TOC does not include page numbers for the schematics for this reason.

Although every effort has been made to ensure that the information contained herein has been transcribed accurately and without error, no responsibility will be accepted for any loss or damages occurring as a result of the use of this information.

I wish to thank Dick Smith Electronics (DSE) for permitting me to reproduce this manual.

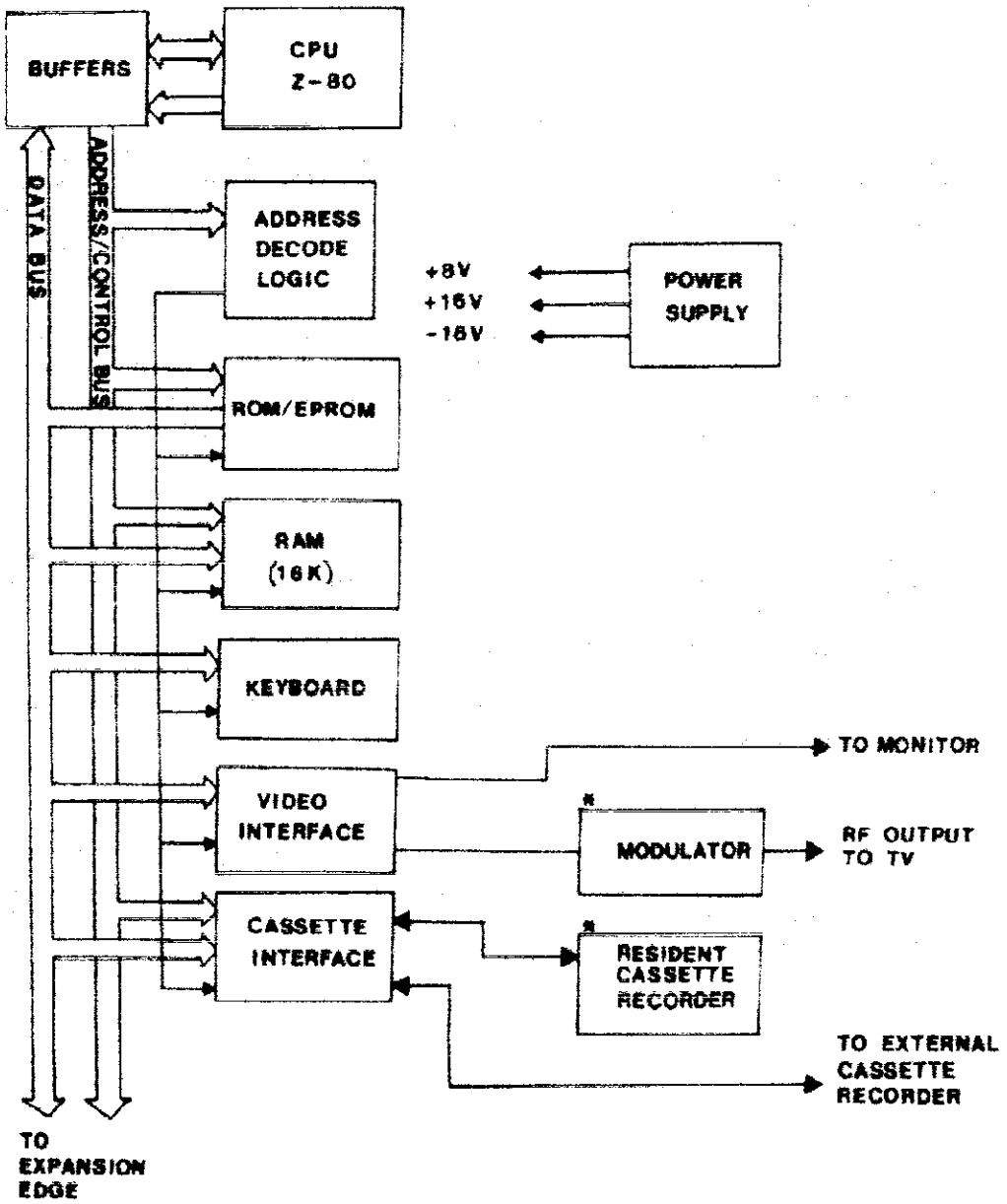
RJS

TABLE OF CONTENTS

1.0 THEORY OF OPERATION

The hardware of the System-80 is described one by one in this section. The computer consists of the following functional blocks: CPU, system ROM, user RAM, address decode and buffers, video interface, cassette interface, keyboard and power supply. These blocks are generally common to both MKI and MKII, and the differences will be mentioned in the appropriate sections. See Fig 1.1 on system blocks.

Fig 1.1 SYSTEM BLOCK DIAGRAM



* NOTE. This is absent in the MKII.

1.1 CPU

Z-80 is employed as the CPU chip which is an 8 bit N-channel microprocessor with 16 address lines. This 40 pin LSI requires a single +5V DC supply. It provides 158 software instructions including those of the 8080A CPU. For details refer to the data sheet of Z-80 in the appendix and the technical manual of the Z-80.

1.1.1 Clock

The CPU operates at 1.7MHZ, derived from a crystal oscillator of either 10.644MHZ or 10.48MHZ and a divide-by-six counter, Z38. The oscillator is implemented on the interface board with three inverters of Z31 and a crystal.

1.1.2 Reset

Power-on-Reset and System-Reset are provided for proper operation of the computer. Power-on-Reset is achieved by an RC delay circuit. Initially the capacitor C2 is discharged through a diode D1 as +5V DC is turned OFF. Once +5V DC is switched ON, C2 will slowly be charged up towards +5V. Pin 26 of Z-80 will experience a logic LOW as Vcc of the CPU reaches the operating supply voltage. Then the CPU will be initialized with the program counter set at 0000H.

System-Reset is done by pulling the input of $\overline{\text{NMI}}$ (pin 17 of Z-80) LOW. As $\overline{\text{NMI}}$ (Non Maskable Interrupt) is active LOW, the CPU will restart execution at location 0066H without altering the programs stored in memory. The system reset button is present on the back panel. A capacitor C1 is added across the switch to minimize switch bounce.

1.1.3 Buses

The bi-directional data lines from the CPU are immediately buffered by Z18, Z19 and Z20 (74LS367). The input buffers are enabled when either $\overline{\text{M1}}$ or $\overline{\text{RD}}$ is active LOW during op-code fetch, interrupt acknowledge, memory read or input cycles. The output buffers are disabled when the control signal $\overline{\text{ADDBS}}$/$\overline{\text{DODBS}}$ is LOW.

The 16 unidirectional address lines are also buffered by Z4, Z6 and Z17 (74LS367). These address lines can be isolated from the system bus by pulling $\overline{\text{ADDBS}}$/$\overline{\text{DODBS}}$ LOW.

The control lines for read/write and input/output are buffered by Z16 (74LS367), and are decoded by Z15 to get memory read/write ($\overline{\text{MRD}}$ and $\overline{\text{MWR}}$) and port input/output ($\overline{\text{IN}}$ and $\overline{\text{OUT}}$) control signals. These control lines can be disabled by making $\overline{\text{C/CDBS}}$/$\overline{\text{STADBS}}$ LOW

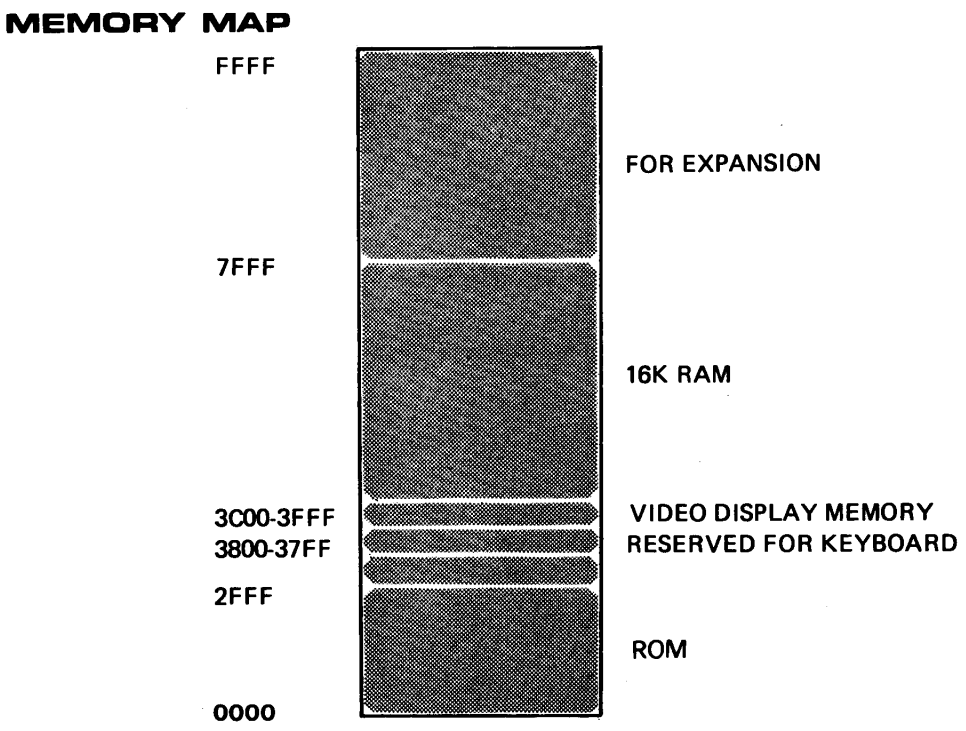
1.1.4 Address Decode

The address decode logic enables the CPU to access ROM, RAM, Keyboard and Video interface respectively. The logic is formed by Z22, Z25, Z35 and Z21. The decode scheme is illustrated as follows.

A15	A14	A13	A12	A11	A10	ENABLE	DECODED OUTPUT
0	0	0	0	X	X	ROM1 (Z10)	Z22 Pin 9, 10
0	0	0	1	X	X	ROM2 (Z11)	Z22 Pin 11, 12
0	0	1	0	X	X	ROM3 (Z12)	Z22 Pin 6, 7
0	0	1	1	0	X	EPROM (Z13)	Z22 Pin 5
0	0	1	1	1	0	Keyboard	Z35 Pin 11
0	0	1	1	1	1	Video RAM	Z35 Pin 3
0	1	X	X	X	X	16K RAM	Z35 Pin 11

Note: X means doesn't matter

Fig 1.2 Memory Map



I/O PORT ASSIGNMENT

CASSETTE INTERFACE – FF, FE
PRINTER INTERFACE – FD

1.2 ROM

All System-80 computers have 12K bytes of Microsoft Extended BASIC interpreter stored in three 4K x 8 ROM's, E3001, E3002, and E3003. These ROM's are pin compatible to standard 4K x 8 chips. There is a 2K x 8 EPROM (2716) providing some special routines. In the Blue Label computers the extended functions include upper case and lower case characters, flashing cursor, auto-repeat keyboard, screen-print, machine language monitor and renumbering. It occupies 1.5K bytes of the EPROM.

In the MKII computer, besides the upper and lower case characters, auto-repeat keys, flashing cursor and screen print functions, the extra routines provide two more features. They are a dumb terminal, HOST communication, and RS232 communication routines. These routines occupy 1.5K bytes of the EPROM. How to use these routines is detailed in the User's Manual.

The ROM's and EPROM share the data buffers (Z9) with the user RAM's. Z25 gives proper chip selection signals to these ROM's. When the ROM and EPROM are addressed, pin 11 of Z25 will be logic HIGH and disables the RAM select signal, $\overline{CAS}$ from Z37 pin 13. Conversely when the RAM's are addressed, pin 12 of Z25 becomes logic HIGH and pin 11 of Z25 logic LOW, that is, the ROM select decoder, Z22 is disabled.

1.3 RAM

Z-80 is capable of easily interfacing to dynamic RAM. The control signal, $\overline{MREQ}$ (Memory Request) facilitates the addressing and refresh of dynamic RAM. Both Genie I and II have 16K bytes of RAM which are 4116 with an access time of 250 nsec. They need a power supply of +5V DC, +12V DC and –5V DC.

1.3.1 Generation of $\overline{RAS}$, MUX and $\overline{CAS}$

Other than Read/Write control, $\overline{RAS}$ (Row Address Strobe), MUX (Address Multiplexing) and $\overline{CAS}$ (Column Address Strobe) are the essential control signals to the RAM array. $\overline{RAS}$ is the same signal as $\overline{MREQ}$. MUX and $\overline{CAS}$ are generated as in Fig 1.3.

Fig 1.3a $\overline{RAS}$, MUX and $\overline{CAS}$

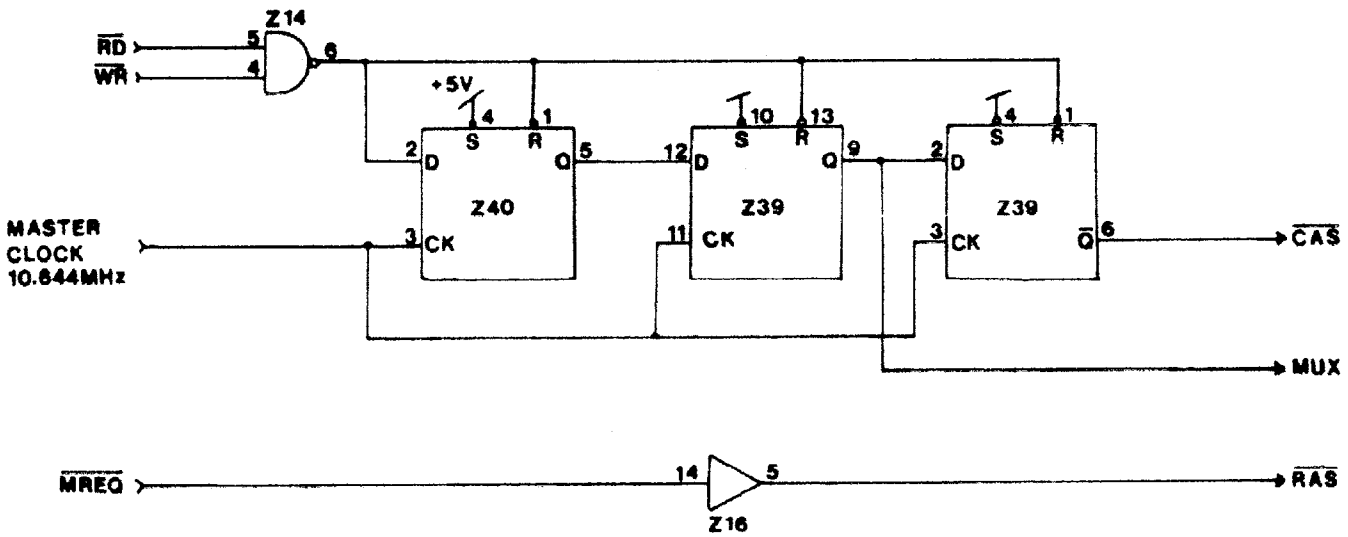
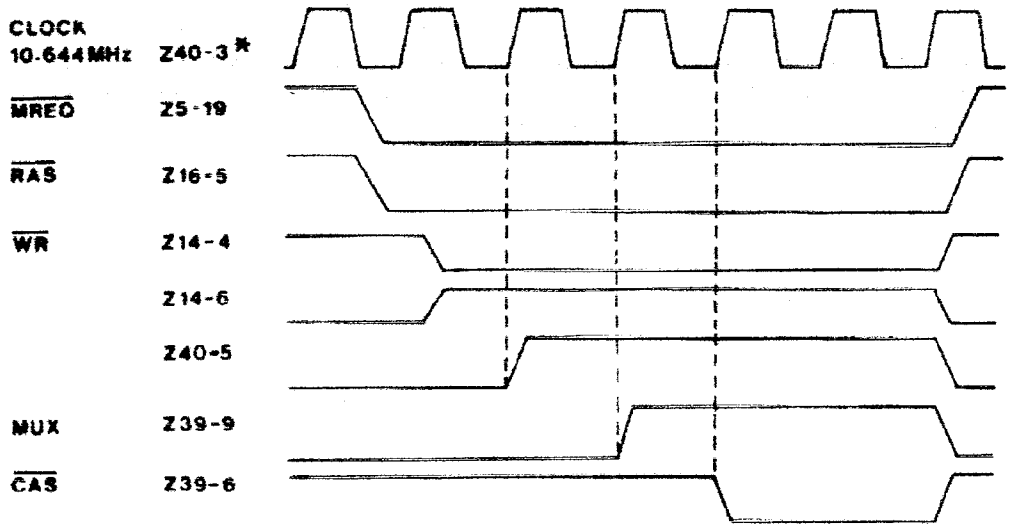


Fig 1.3b Timing of $\overline{RAS}$, MUX and $\overline{CAS}$



- Note: Z40-3 Means pin 3 of Z40

The generation of MUX and $\overline{CAS}$ is initiated and terminated by the $\overline{WR}$ or $\overline{RD}$ timing (Z14), and the active pulse width is determined by the time period of the master clock. When either $\overline{RD}$ or $\overline{WR}$ is active LOW, Z14-6 and Z40-2 will encounter a logic HIGH, and the D-type F/F (Z40-5) will change state from 0 to 1 upon the rising edge of the clock. Then MUX and $\overline{CAS}$ will become active at the following clocking edges respectively as shown in Fig 1.3b.

1.3.2 Memory Read/Write

Since the 4116 RAM has internal row/column address latches, the address lines to the RAM are multiplexed by Z23 and Z24 (74LS157), and are controlled by the signal MUX. The row (or low order) address will appear on the address inputs of the RAM as MUX is LOW, and will be latched into the RAM by $\overline{RAS}$. When MUX is HIGH, the column (or high order) address appears on the address inputs of the RAM, and will be latched into the RAM by $\overline{CAS}$.

The addressing is similar in the case of memory read and memory write although the strobe $\overline{CAS}$ appears earlier during memory read cycles than during memory write cycles. During memory read, $\overline{MWR}$ at pin 3 of 4116 is HIGH and the data output buffers (Z9) are enabled. The stored data will be put onto the data bus. During memory write, $\overline{MWR}$ becomes LOW, $\overline{MRD}$ becomes HIGH, and the output buffer (Z9) will then be disabled. The information on the data bus will be strobed into the register of the RAM by the falling edge of $\overline{CAS}$.

1.3.3 RAM Refresh

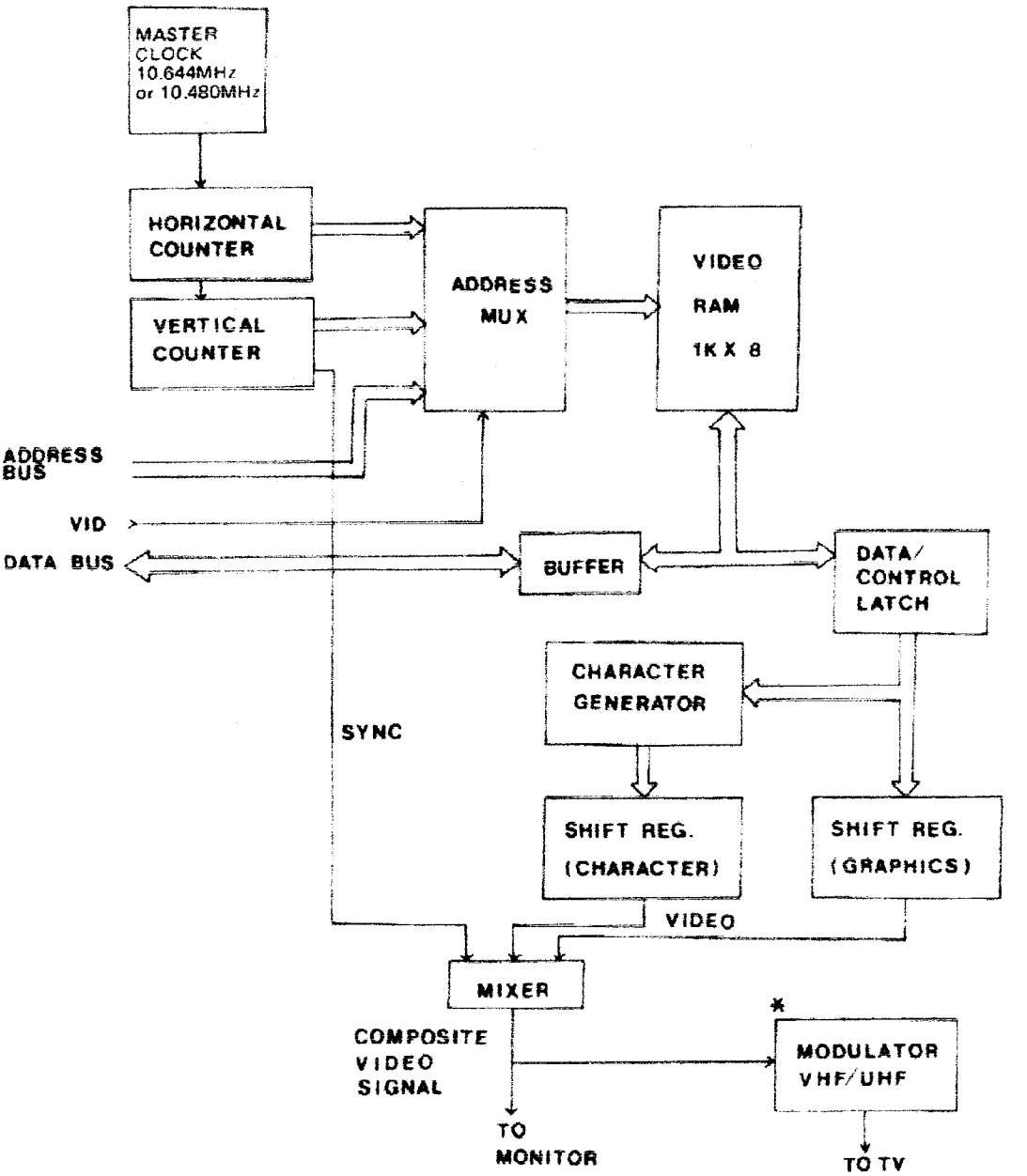
The memory cells of 4116 require a periodic refresh within every 2 msec. During clock states T3 and T4 of an op-code fetch cycle, the CPU puts a memory refresh address on the address bus, and $\overline{MREQ}$ becomes active. Since $\overline{RAS}$ is the same as $\overline{MREQ}$, the RAM receives a row address, and that row of memory cells is refreshed. The refresh address is incremented by one in every op-code fetch cycle. The related timings are referred to in the Z80 data sheet in the appendix.

1.4 Video Interface

This section will reveal how the horizontal and vertical synchronization signals and the video signals are generated. In addition, we shall discuss how the video RAM's are accessed by the CPU, and are used to store the information displayed on the screen.

The structure of the video signal interface is illustrated in the block diagram of Fig 1.4. It will be detailed in the following sub-sections.

Fig 1.4 Block Diagram of the Video Interface

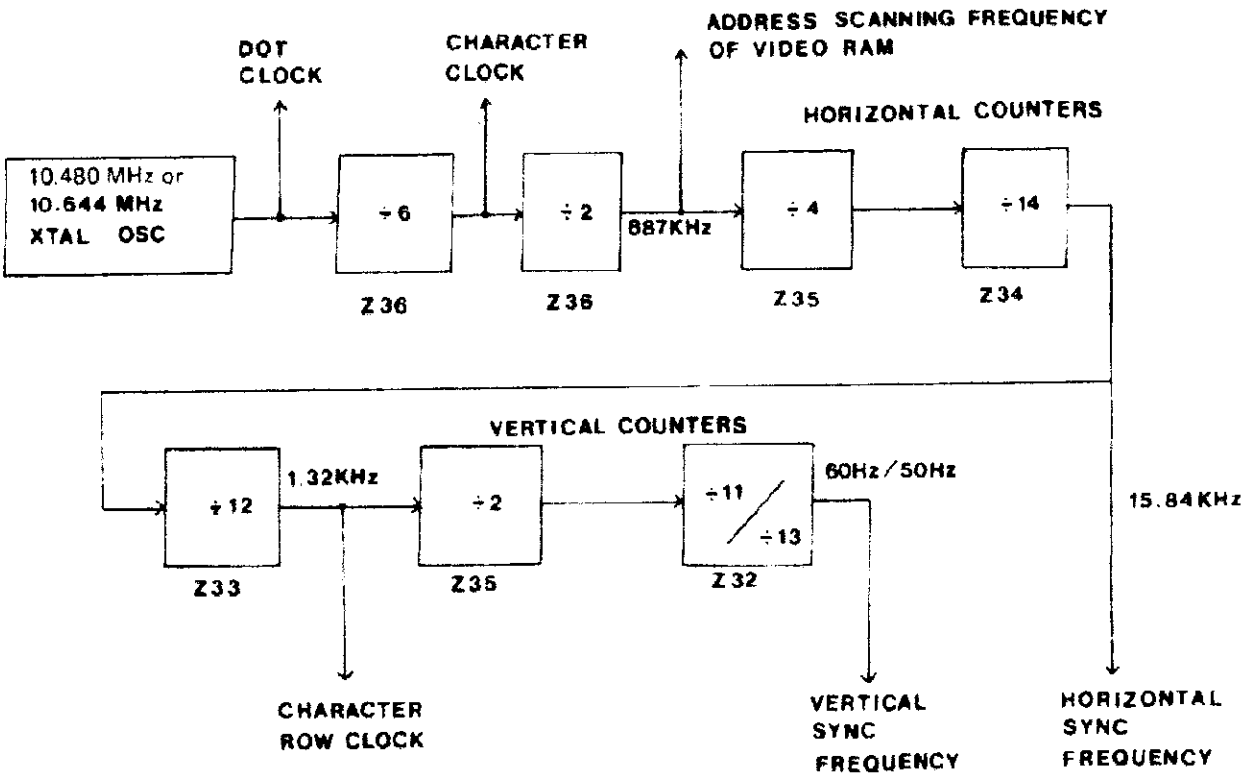


* NOTE Not present in MKII computers.

1.4.1 Horizontal and Vertical Sync Signals

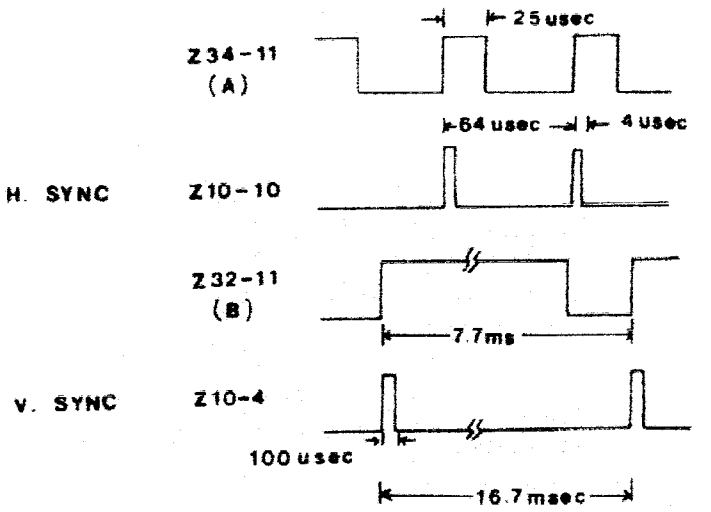
These two sync signals are generated by a divider chain with a master clock of 10.644 MHZ. The format of 64 characters/row x 16 rows is assumed in the following sections. Z36, Z35 and Z34 are the horizontal counters, and Z33 and Z32 are the vertical counters. The divider chain is shown in Fig 1.5. Note that a character or a graphic unit is inside a 6 x 12 dot matrix.

Fig 1.5 Divider Chain of the Video Display



The outputs at Z34-11 and Z32-11 are the horizontal and the vertical sync frequencies (15.84 KHz and 50/60 Hz) respectively. These two sync frequencies will be shaped into the required sync pulses to the video display unit. First, VR1, C17 and four inverters (4069) delay the horizontal sync clock from Z34, while VR2, C16 and four inverters delay the vertical sync clock from Z32. Hence, we can shift the picture position by adjusting VR1 and VR2. Then the two delayed signals are separately shaped into the desired sync pulses by a monostable circuit which contains an RC differentiating network and two inverters. The two sync pulses are shown in Fig 1.6. Z22 forms an exclusive OR gate, and sums up the horizontal and vertical sync pulses into the composite sync signal which is then fed to the video mixer to generate the composite video signal. (See section 1.4.3 on composite video signal).

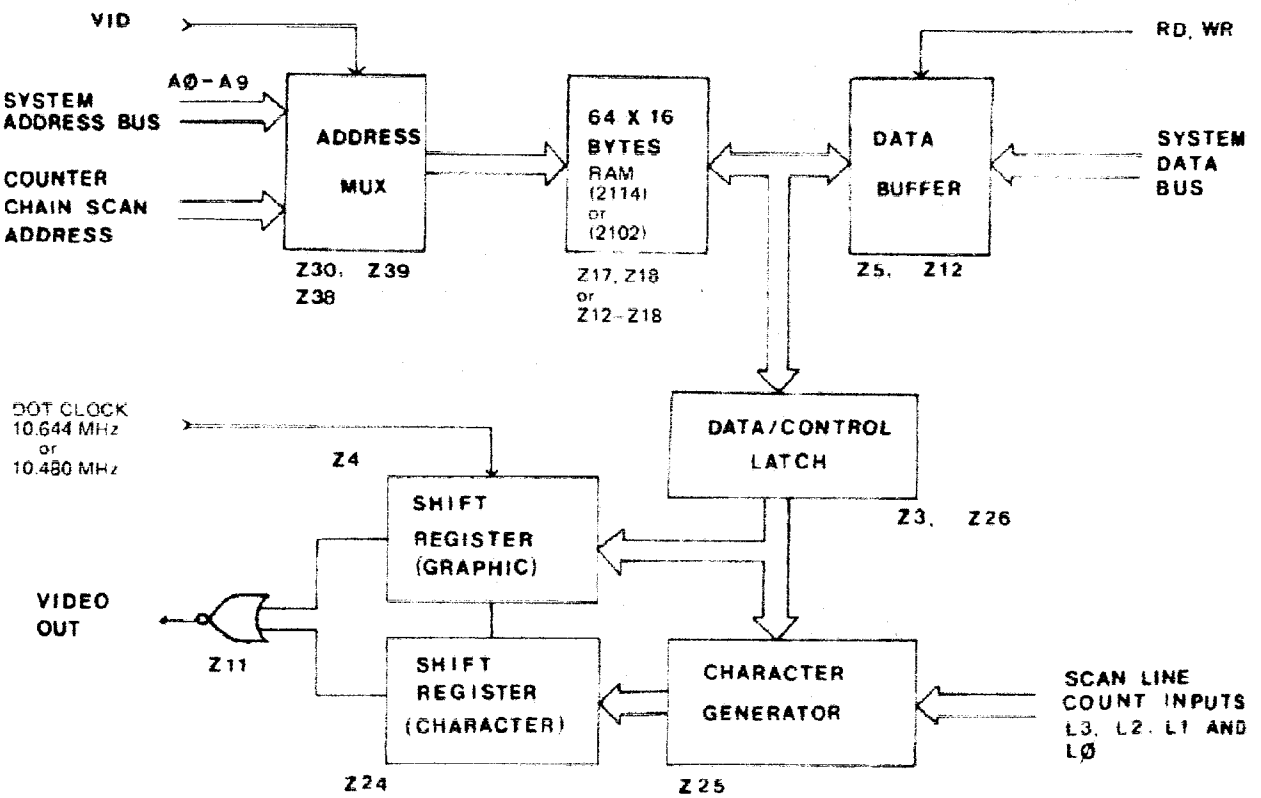
Fig 1.6 Horizontal and Vertical Sync Pulses



1.4.2 Video Memory

The video memory stores up the video information displayed on the screen. The memory is composed of two 2114 RAMs or, in older models, seven or eight 2102 RAMs.

Fig 1.7 Video RAM Interfacing



1.4.2.1 Video RAM Addressing

The video RAM is addressed by either the CPU or the counter chain. In order to display a character at a certain position on the screen, the CPU has to write the ASCII code of the character into the corresponding location of the video RAM. The video RAM has address bits, A0–A9 in which A0–A5 specify one of the 16 rows. The 64x16 characters are memory mapped into the 64x16 locations of the video RAM.

As the CPU is going to access the video RAM (C300H – 3FFFH), the address decoded signal, VID from the CPU board will be LOW. The address multiplexers Z30, Z39 and Z38 switch to the system address bus. At the write mode, the $\overline{WR}$ signal will set the RAM's $\overline{W}$/R line LOW and enable the input buffers, then the data on the data bus will be stored into the RAM. At the read mode, the $\overline{RD}$ signal enables the output buffers, and the RAM will put the addressed data onto the data bus. Notice that the display is blanked during the CPU's access to the video RAM because VID sets the data/control latch Z3 and Z26 to the CLEAR state through Z40-6.

It is required to maintain a continuous display of information on the screen so that the video RAM will be scanned periodically by the counter chain. 64 video memory locations are read in sequence during the scanning of each line. Each row of characters occupies 12 scanning lines, and therefore, the vertical address increases by one every 12 lines. The outputs of the counters are connected to the RAM's address inputs through multiplexers Z29, Z30, Z37, Z39 and Z38. They are listed below.

Horizontal Count	RAM Address	Vertical Count	RAM Address
Z36-8	A0	Z32-14	A6
Z35-9	A1	Z32-12	A7
Z35-8	A2	Z32-9	A8
Z34-12	A3	Z32-8	A9
Z34-9	A4		
Z34-8	A5		

1.4.2.2 Video Signal Generation

In alphanumeric mode, the character generator is the essential part in producing the video signals. The character generator is MM52116 FDW (or custom chip E3004) which provides upper and lower case characters in a 5x9 dot matrix. Recall that each row of characters is composed of 12 scanning lines. The line count signals L3, L2, L1 and L0 of the character generator come from pin 11, 8, 9 and 12 of Z33 respectively. Z33 is the divide-by-12 vertical counter.

D7 of a character data is zero whereas that of a graphic data is one. As the video RAM is addressed by the counter chain, Z17 and Z18 (2114) are set to the READ mode. The ASCII code of a character from the RAM is latched into Z26 and Z3 at the rising edge of the strobe at Z28-3. See Fig 1.8(a). The character generator Z25 is addressed by the six data bits from the latches, Z26 and Z3. The character generator will output the corresponding 5-bit dot signals of the character on the scanning line defined by L3-L0. When Z36 counts to 5, Z28-3 will be LOW and then Z2-6 will also be LOW. The output of the character generator will be loaded in parallel into the shift register Z24. When Z28-3 becomes HIGH again, the dot signals will be shifted out serially from Z24-13 at the rate of the dot clock 10.644 MHz. Meanwhile during the rising edge of the strobe at Z28-3, the next character will be latched into Z26 and Z3, ready to be shifted out next.

Fig 1.8(a) Video Display Timing of a Character

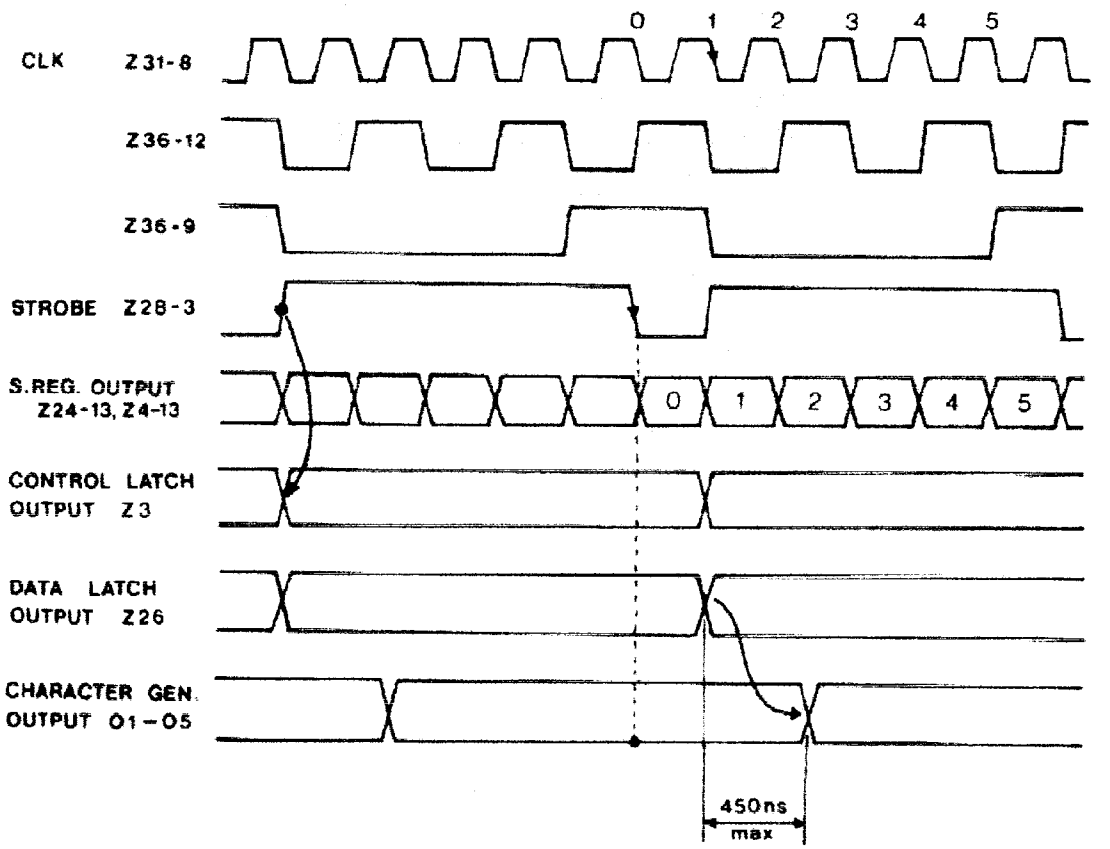
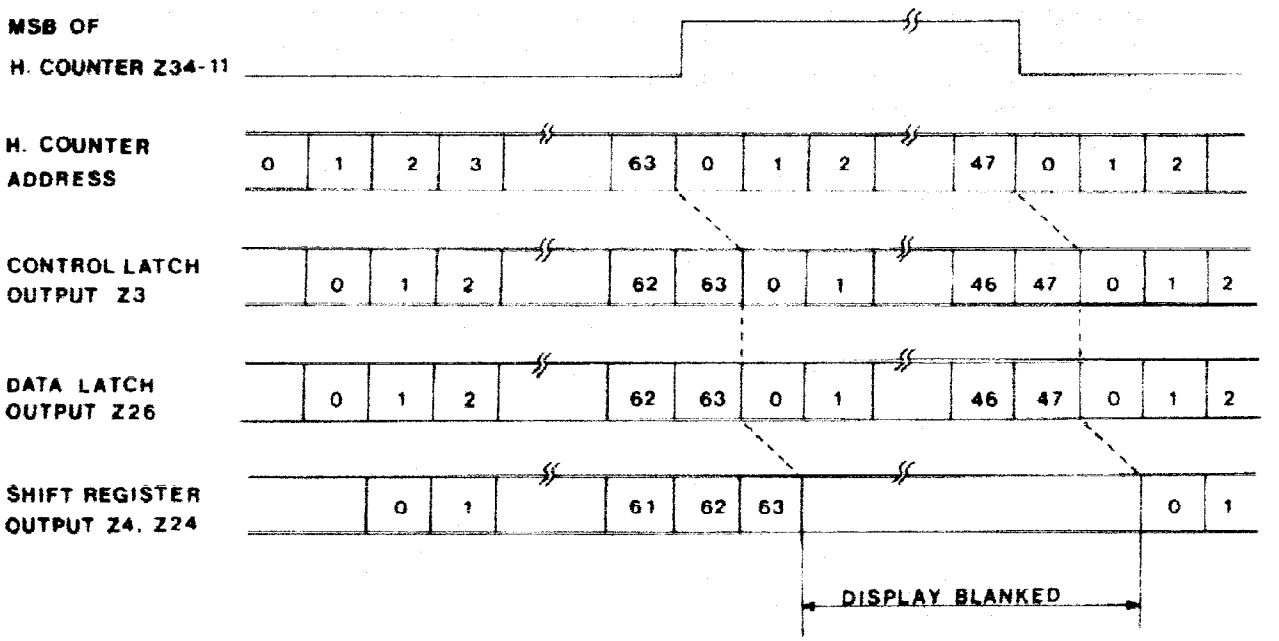


Fig 1.8(b) Video Display Timing of a Line



NOTE: The numbers in the control and data latch timings represent the control or data signals of the corresponding horizontal address.

In the graphics mode, each row contains 64 graphic units in 12 scanning lines, and each unit is made up of 6 cells. Each cell corresponds to one data bit in the RAM. For details refer to section 1.4.4.2.on graphic data.

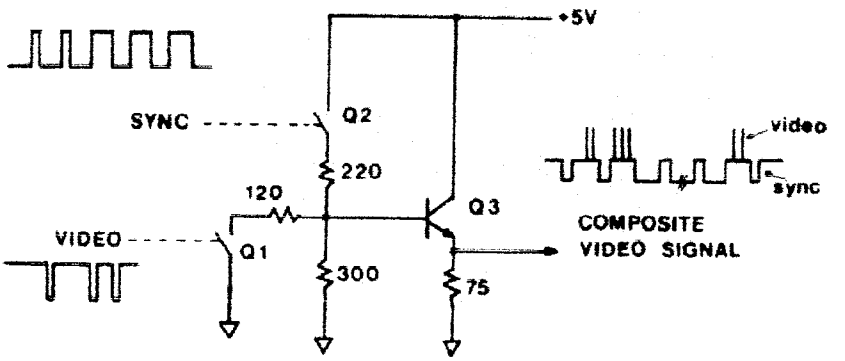
The generation of video signals in the graphic mode is similar to that in the character mode. They differ in that a multiplexer, Z27 and a shift register, Z4 are used in the graphic mode. Since D7 of a graphic data is one, and then Z3-7 is HIGH, Z4 will be enabled to accept the graphic data from Z27. The dot signals will be shifted out serially at Z4-13 at the rate of 10.644 MHz. Note that the multiplexer, Z27 is controlled by L3 and L2, and the graphic data from the latch, Z26 is fed to Z27 instead of the character generator, Z25.

Display blanking is achieved as follows. Scanning lines 9-11 in the character mode are automatically blanked because the outputs of the character generator will be zero during these three lines. The horizontal and vertical blanking signal comes from Z11-1 and inhibits Z24 and Z4 from getting parallel data from Z25 and Z27 respectively. The display is blanked during the period of screen boundary and retrace when the horizontal or vertical sync signal is HIGH at pin 2 or 3 of Z11 respectively. See Fig 1.8(b)

1.4.3 Composite Video Signal

The horizontal sync and the vertical sync signals are combined by Z22, and this composite sync signal is fed to the base of Q2. Q1 and Q2 act as two switches. Q3 forms a mixing circuit, and the sync and video signals are summed at the base of Q3. Fig 1.9 shows the simplified composite video mixer. The composite video signal so formed will be sent to the video monitor or the input of a built-in VHF or UHF modulator. Note that MKII does not have a modulator and cannot use a TV as the video display without modifications.

Fig 1.9 Equivalent Circuit of Video Mixer



1.4.4 Display Modes

The System 80 has two display modes, namely character mode and graphic mode. Data bit 7 of the video memory determines the display mode; character mode is selected when D7 is logical '0' and graphic mode when D7 is logical '1'.

1.4.4.1 Character Mode

The characters displayed are in alphanumeric format, and their ASCII codes are stored in the video RAM. In the preceding sections, 64 characters/line mode is assumed. The MKI System 80 has a push button, S1 on the back panel of the unit to select either 64 characters/line or 32 characters/line mode. The MKII System 80 has no 32 characters/line mode of display.

In 32 characters/line mode switch S1 is closed. Multiplexers Z29 and Z37 are switched to the other four inputs. The reference counter clock becomes CLOCK/2 so that the horizontal/vertical counting frequencies will be scaled down by two. The PAGE switch chooses the left page when LOW and the right page when HIGH. This is obvious because A5 of the video RAM is connected to the PAGE signal through the multiplexer Z37, and the address bits A0-A5 select one of the 64 columns in the 64x16 units of bytes of video memory.

1.4.4.2 Graphic Mode

D7 is logical one when graphics are to be displayed. The shift register Z4 is enabled. The graphic data from the video RAM is latched into Z26, the outputs of Z26 are multiplexed by Z27 (74LS153) selecting two out of six bits each time. The selection is controlled by the line count signals, L2 and L3. A graphic cell is shown below.

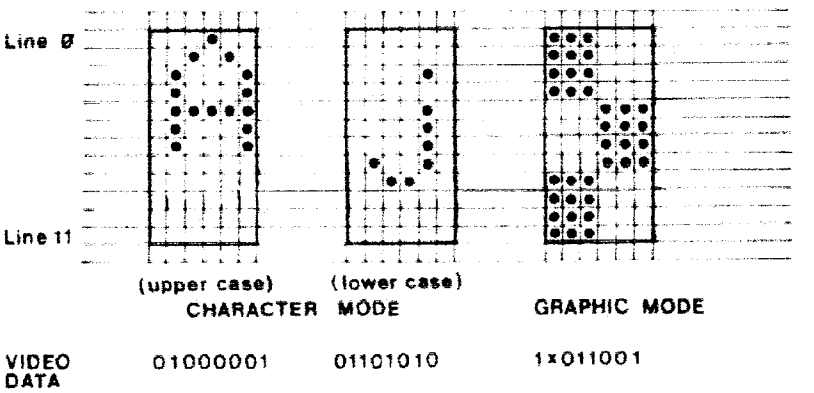
1 graphic unit

(6 graphic cells)

DØ	D1
D2	D3
D4	D5

D0 and D1 are selected for scan lines 00-03; D2 and D3 for scan lines 04-07; D4 and D5 for scan lines 08-011. The display formats of the character/graphic modes are shown in Fig 1.10

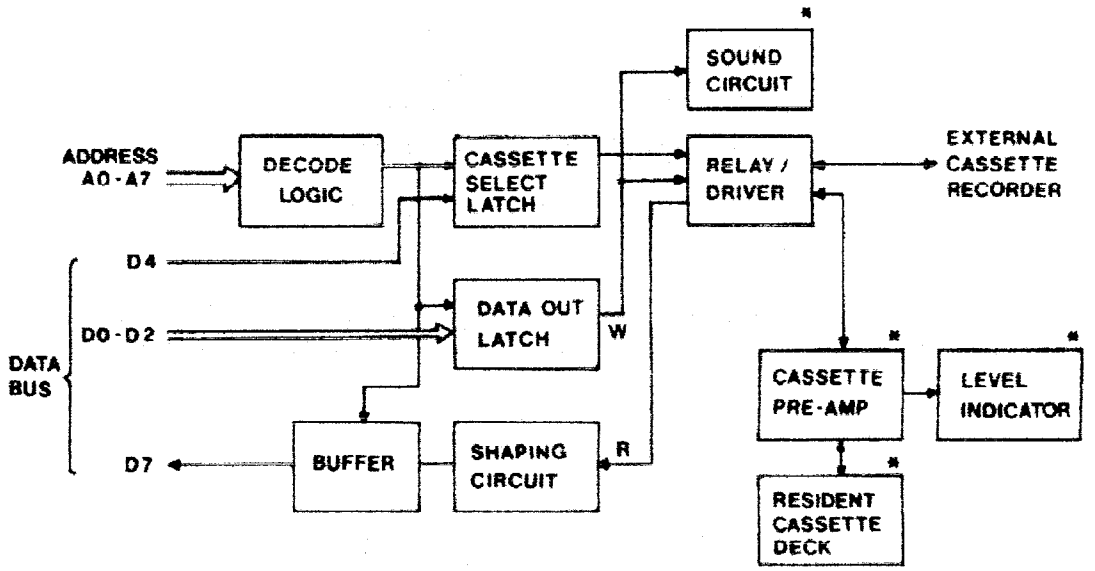
Fig 1.10 Character/Graphic Display Format



1.5 Cassette Interface

The cassette interface consists of the following parts: address decoding, latches, cassette select and relay drivers, rectifying and shaping circuit, cassette preamplifiers and output level indicator. The sound effects circuit also uses the cassette output port.

Fig 1.11 Cassette Interface



***Note:** These parts are absent in the MK II Systems

1.5.1 Addressing/Decode

Z19, Z31 and Z20 generate the address decode signals and the I/O control signals. Table 1.1 shows the I/O port assignments.

Table 1.1 Cassette I/O Port

Port	Data Bits		High	Low
Output, FF	D2		Cassette ON	Cassette OFF
	D0, D1	Signal Output		
Input, FF	D7	Signal Input		
Output, FE	D4		Cassette 2 Selected (External)	Cassette 1 Selected

1.5.2 Cassette Selection

The CPU selects either cassette #1 or cassette #2 through the output port FE with data line D4. The selecting signal from D4 is latched by Z40 and the outputs at Z40-8 ($\overline{Q}$) and Z40-9 (Q). Cassette #1 is selected as D4 is LOW, Q7 and Q8 will turn ON provided D2 (at Z6-2) is HIGH. Relay REL1 will be activated and the READ, WRITE and motor drive lines of the resident cassette #1 will be connected to the cassette interface.

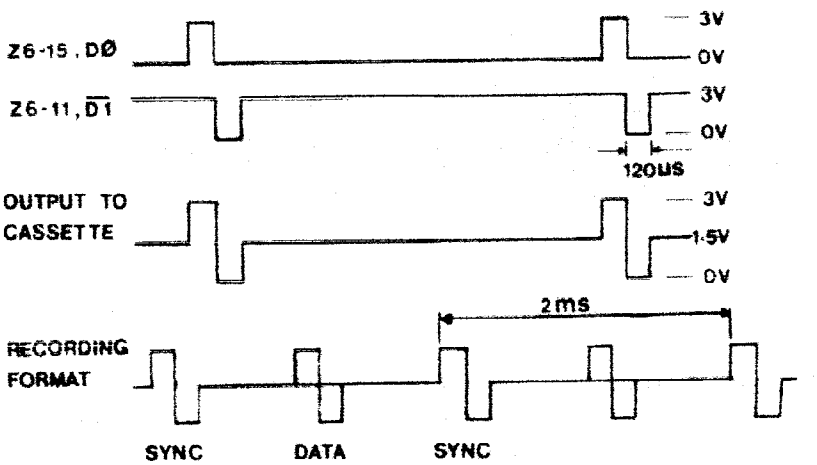
When D4 and then Z40-9 are HIGH, Q5 and Q6 will turn ON if D2 at Z6-2 is also HIGH. Relay REL2 will be activated and the cassette input, output and remote control lines of an external cassette recorder will be properly connected to the cassette interface through a 5 pin DIN socket K3.

The System 80 MK II is designed to operate with an external cassette recorder, so the circuitry for the resident cassette is omitted. Compare the schematics of the cassette interfaces for the System 80 MK I and MK II.

1.5.3 Cassette Write

The idealized recording signal to be stored on the cassette tape is shown in Fig 1.12. This signal is formed by data D1, D0 and a summing circuit at Z6-11 ($\overline{Q}$) and Z6-15 (Q). The logical outputs of D1 and D0 are software controlled to construct the desired recording signals.

Fig 1.12 Cassette Write Signals

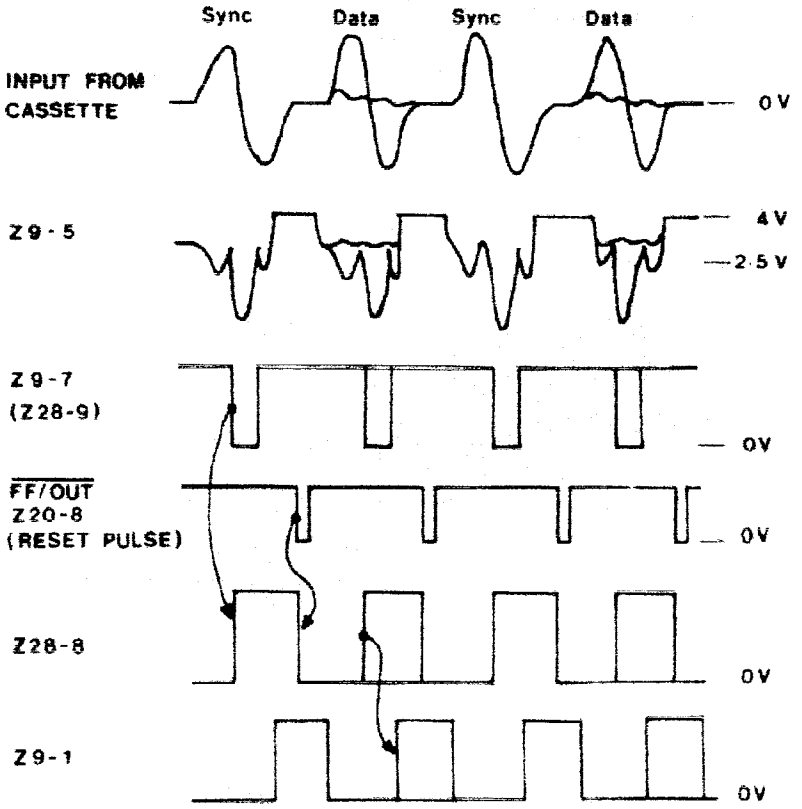


The data format stored on the cassette tape is as follows. At the beginning of cassette write (CSAVE) the CPU outputs 128 ZERO data bits followed by a code A5H. The CPU will detect this code during cassette read (CLOAD) for synchronization. Next comes a two byte starting address and a two byte ending address of the program in the RAM. After all data has been written a byte of check sum is added for detecting errors during cassette read/write.

1.5.4 Cassette Read

Before the CPU can recognize the information retrieved from a cassette tape the audio signal from the cassette recorder must be shaped into logical sync and data signals. The CPU and cassette routine will then convert the serial data into source programs that will be stored in the RAM. The filtering preamplifiers formed by Z1 (LM324) on the cassette board amplify the small signals from the Read/Write head. The amplified signal is buffered (Q1) and rectified to drive a level meter. This signal level indication is useful in reading various cassette tapes. We may obtain the proper signal level by adjusting the gain of Z1 (VR3).

FIG 1.13 Cassette Read Signals

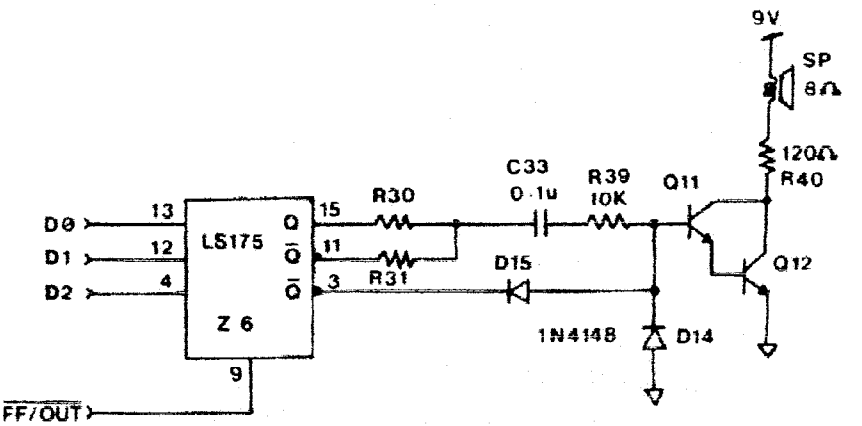


Z9 (LM324) on the interface board converts the audio signal from the recorder into serial digital data. The input signal is high-pass filtered then full wave rectified. Negative going pulses are obtained at Z9-7, the output of a level detector Z9-7 is connected to Z28-9. Z28 forms an R-S bi-stable latch, and Z28-8 is connected to the data line D7 through a buffer Z7. Z28-8 is triggered HIGH by the falling edge at Z9-7. As soon as the CPU has read a logical one at data line D7 it will reset the bi-stable latch after 500 usec. Upon detecting the leading zeroes and the sync code (A5H) the CPU should be synchronized with the serial data stream. It will strobe the data pulse at 1 msec after the sync pulse and reset the bi-stable latch. Pulses at Z28-8 are delayed for about 250 usec and output at Z9-1. The delayed pulse pulls the signal at Z9-5 up, therefore the signal to noise ratio is increased.

1.5.5 Sound Output (Blue Label Machines Only)

Apart from video display, sound effects are another way of communication between a man and the System 80 microcomputer. This is implemented simply by an audio driver (Q11 and Q12 darlington pair) and a built in loudspeaker. The sound circuit is connected to the cassette output port FFH. The sound output is determined by the software outputting various data streams to D0 and D1 of the output port. See Fig 1.14. The sound stops during CSAVE because the base of Q11 is pulled LOW by Z6-3 ($\overline{Q}$ of D2). D2 of the output port FFH becomes HIGH during cassette ON.

Fig 1.14 Sound Circuit (On Interface Board)



1.6 Keyboard

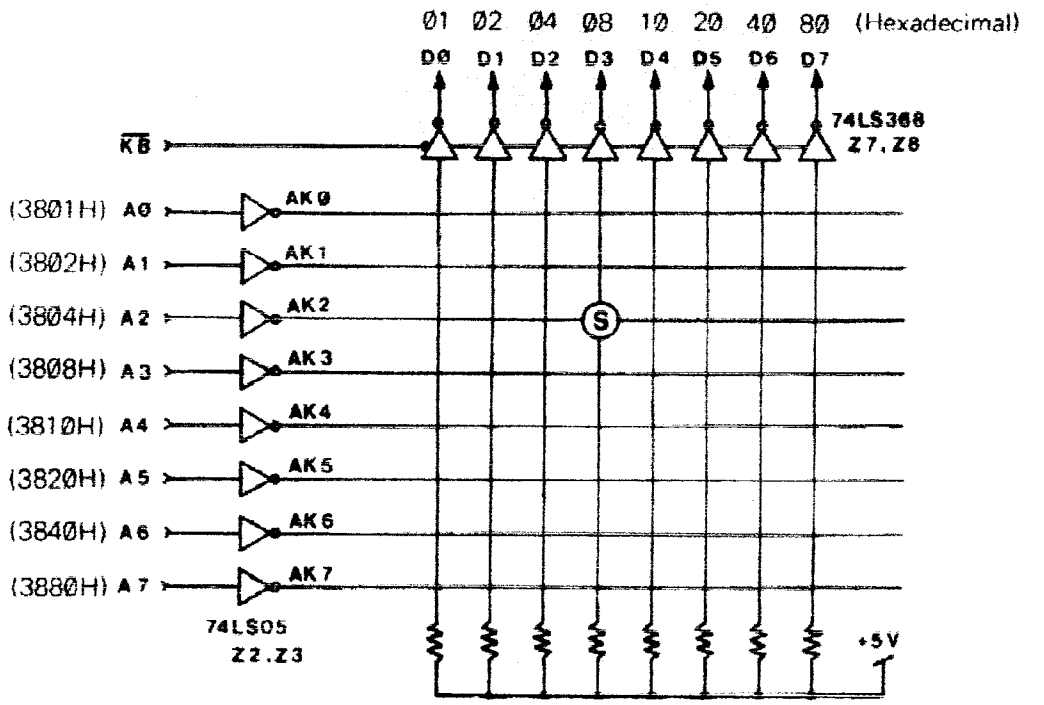
The key matrix is memory mapped with addresses from 3800H to 3880H; and locations 3800H to 3BFFH are reserved for keyboard use. Refer to the memory map in Fig 1.2.

There are two locked switches, F1 and PAGE, which are not included in the key matrix. They directly control the hardware of the resident cassette recorder and the display modes respectively. These two keys are absent in MK II machines which have no resident cassette recorder.

1.6.1 Key Matrix

The key matrix is formed by 8 inverted address lines, AK0-AK7, and 8 inverted data lines DK0-DK7. The matrix is illustrated in Fig 1.15.

Fig 1.15 Key Matrix



The inverting buffers Z7 and Z8 are controlled by the keyboard strobe $\overline{KB}$ which is derived from Z35-11 on the CPU board. Refer to Section 1.1.4. $\overline{KB}$ is active LOW when the CPU is accessing the memory locations 3800H-3BFFH. A0-A7 are the open collector outputs of Z2 and Z3 (74LS05).

While no key is pressed DK0-DK7 are all HIGH since they are pulled up to +5V by resistors. The CPU reads 00H, indicating no key is pressed. The keyboard routine in the system ROM scans through the A0-A7 lines repeatedly, making one address line logic HIGH each time. See Fig 1.15. When a key is pressed the CPU will detect a logic HIGH on the corresponding data line as soon as the corresponding address line is scanned. For example, key "S" is depressed. The DK3 line will be connected to the AK2 line and DK3 will be LOW as A2 is logic HIGH. Then the CPU will read 08H into the accumulator from the memory location 3804H. The keyboard routine will decode it into the ASCII equivalent of the character "S". Except for the command keys the ASCII codes of the characters or symbols keyed in will be written into the video RAM and displayed.

1.6.2 Numeric Keypad (MK II Machines Only)

This keypad contains the numeric keys and four function keys. The numeric keys have the same positions in the key matrix as the main keyboard. The function keys are user programmable and occupy the AK3 line of address 3808H. Refer to the schematic of the keyboard.

1.7 POWER SUPPLY

The power supply unit, which is in a heat resistant plastic box, delivers full wave rectified +8V DC, +16V DC and –16V DC. The two power transformers have secondary voltages of 9.6V x 2 and 15V x 2 respectively. At the primary side of the transformers there is a line filter network consisting of a parallel ceramic capacitor of 0.01 uF and two series RF chokes. Over voltage protection is provided by a varistor across the AC mains. The metal oxide varistor has a breakdown voltage of 275V with 55 joules. Overload and short circuit damages are minimized by a fuse of 0.5A in series with the AC mains.

Specifications for the Output Voltages:

Voltage	No Load Voltage		Full Load Voltage		Remarks
	Min	Max	Min	Max	
+8V	10.5V	11.5V	8V	9V	FL +8V @ 1.2A
+16V	20V	24V	15V	18V	FL +16V @ 150mA
-16V	20V	24V	15V	18V	FL –16V @ 100mA

Linear IC regulators 7805 and 7812 on the CPU board supply +5V and +12V respectively. A simple zener regulator provides –5V for the dynamic RAM. On the interface board +9V supply is obtained from +16V by a transistor/zener regulating circuit (Q10 and 10V zener diode) +9V DC is required for driving the relays on the interface board, the preamplifier (Z1, LM324) on the cassette board, and the motor of the resident cassette recorder.

1.8 RS-232C Interface

The X-4022 RS-232C Interface gives you the flexibility of:

i) a wide range of useful baud rate: 110, 300, 600, 1200, 2400, 4800, 9600 and 19200
ii) selectable word lengths: 5, 6, 7 and 8 bits
iii) selectable 1 or 2 stop bits
iv) optional parity bit, and selectable odd or even parity

On the RS-232C Interface card there are two dip switches. The one along the middle row is called DP1, (with red paint marking), and the other is called DP2.

If you wish to use the RS-232C Interface to operate serial printers, set switches 6,7 and 8 of DP1 to OFF, ON and OFF respectively. Then you can use the LPRINT and LLIST commands for your hard copy printout from a serial printer. While the serial printer interface is in use the parallel printer interface will be disabled automatically. Otherwise switches 6, 7 and 8 of DP1 should be set to ON, OFF and ON positions respectively for normal communication operation, and the serial printer function is recovered.

FUNCTION	DP1		
	S6	S7	S8
Serial Printer (W/O Handshaking)	OFF	ON	OFF
Serial Printer (With Handshaking)	ON	ON	OFF
Communication	ON	OFF	ON

Flip switches 1 to 5 of DP1 to select the desired functions that are suitable for your RS-232C device

DP1	FUNCTION	
	ON	OFF
S1	Parity Enabled	Parity Inhibited
S2	1 Stop Bit	2 Stop Bits
S3	Odd Parity	Even Parity

*Note If 5 bits/character is selected this will produce 1 ½ stop bits
Switch 3 and 4 of DP1 selects number of bits per character

No of Bits	DP1	
Per Character	S3	S4
5	ON	ON
6	ON	OFF
7	OFF	ON
8	OFF	OFF

Select the proper baud rate by flipping switches of DP2 in proper positions as below

Baud	DP2							
Rate	S1	S2	S3	S4	S5	S6	S7	S8
19200	ON	-	-	-	-	-	-	-
9600	-	ON	-	-	-	-	-	-
4800	-	-	ON	-	-	-	-	-
2400	-	-	-	ON	-	-	-	-
1200	-	-	-	-	ON	-	-	-
600	-	-	-	-	-	ON	-	-
300	-	-	-	-	-	-	ON	-
110	-	-	-	-	-	-	-	ON

Note: - denotes the OFF position

The address decode scheme is as follows

PORT FUNCTION	ADDRESS (HEX)	INPUT TO CPU	OUTPUT TO INTERFACE
Serial Input Port	F8	Data	Status
Serial Output Port	F9	Status	Data
Serial Printer	FD	Status	Data

Bit Assignment for Status Ports

DATA BIT	COMMUNICATION OUT PORT F8H	COMMUNICATION IN PORT F9H	SERIAL PRINTER IN PORT FDH
D0	Request to send DB-25 Pin 4	Data Available 1 = True	Not Used
D1	Data Terminal Ready DB-25 Pin 20	Overrun Error 1 = True	Unused
D2	UART Reset 1 = True	Framing Error 1 = True	Unused
D3	Unused	Parity Error 1 = True	Unused
D4	Unused	Carrier Detect DB-25 Pin 8	Carrier Detect DB-25 Pin 8
D5	Unused	Data Set Ready DB-25 Pin 6	Data Set Ready DB-25 Pin 6
D6	Unused	Clear to Send DB-25 Pin 5	Always LOW
D7	Unused	Transmitting Buffer Empty 0 = True	Transmitting Buffer Empty 0 = True

The Pin Assignment for the RS-232C Interface

PIN	SIGNAL	DESCRIPTION
1	PGND	Protective Ground
2	TXD	Transmit Data (Out)
3	RXD	Receive Data (In)
4	RTS	Request to Send (Out)
5	CTS	Clear To Send (In)
6	DSR	Data Set Ready (In)
7	SGND	Signal Ground
8	CD	Carrier Detect (In)
29	DTR	Data Terminal Ready (Out)

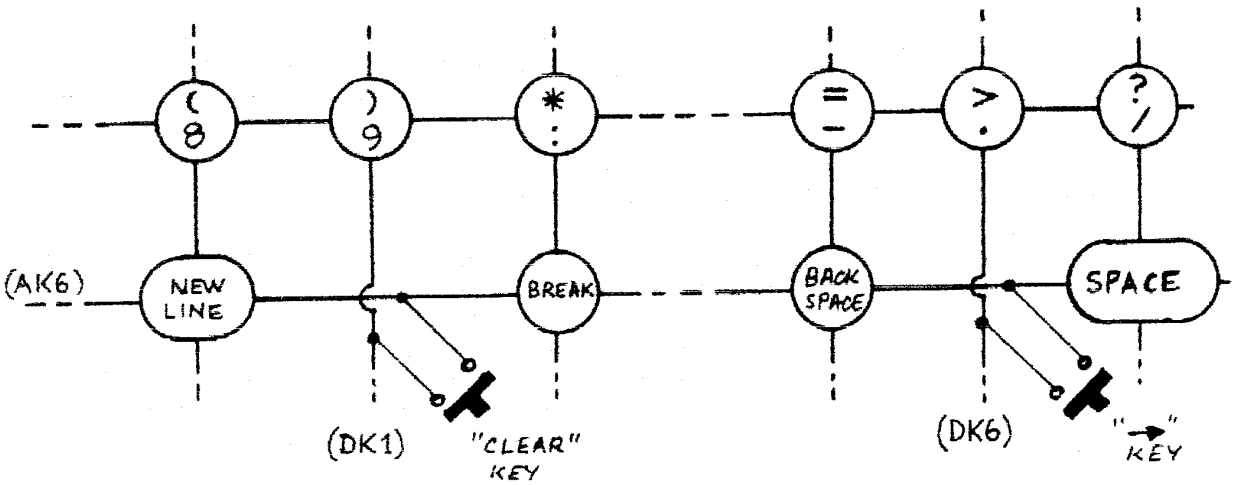
1.9 MINOR MODIFICATIONS TO EARLIER SYSTEM 80 COMPUTERS

1.9.1 Providing FORWARD ARROW and CLEAR Keys

The keyboard of earlier System 80 computers does not provide the "Forward Arrow" or "Clear" keys as provided on the TRS-80 machine. This is generally not a major problem, as neither key is used often. However there are some existing TRS-80 programs where one or the other is used.

Where such programs are written in BASIC, it is usually a fairly simple matter to modify the program so that it uses other keys. But this is generally not as easy to do with machine language or "System" programs.

As it happens, the addition of extra keys on the System 80 keyboard to provide the extra functions is electrically very simple. The key switches are arranged in a matrix, which is software scanned, and the matrix positions which, in the TRS-80, are occupied by both keys are currently vacant. So all that is needed are two additional pushbuttons or key switches, and four lengths of wire to connect them thus:



As you can see, the "FORWARD ARROW" key connects to the DK6 and AK6 scanning lines of the keyboard PC Board, while the "CLEAR" key connects to the DK1 and AK6 lines.

But while this modification is electrically simple, it is not so easy mechanically. Ideally perhaps, the switches would be mounted immediately to the right of the "BACKSPACE" key, but this would require cutting mounting holes in both the keyboard escutcheon and the metal mounting plate. The latter would mean removal of all the key switches, and few would be prepared to do this.

The exact approach used is a matter for the individual owner. Low cost bush buttons (like DSE Cat # S-1102) could be used, and mounted in holes drilled in the panel escutcheon at convenient locations.

Another possibility, and a rather neater one, is to fit the new key switches in place of the right hand SHIFT key. This requires removal of the present double width key top, replacement of the present dummy spring unit along side the SHIFT key switch with a second switch, rewiring the existing switch and wiring of the new switch to the scanning matrix, and fitting the switches with suitably marked single width key tops. This requires no cutting of the escutcheon and produces quite a neat job.

1.9.2 External Cassette Recorder Connection

One of the advantages of the System 80 is the inbuilt cassette tape deck, which allows for error free loading of both BASIC and System (Machine Language) program tapes. Because the deck circuitry is designed to do this even when the recorded level of the tapes varies over a wide range, it is not provided with a user accessible volume control. So there are normally fewer hassles in loading programs ... one less control to worry about.

However occasionally (Murphy's Law) there are tapes whose recorded level is either too high or too low to load correctly with the internal deck's preset circuit.

With BASIC tapes there is no problem, because the CLOAD#-2 command can be used to load them via an external recorder with an adjustable volume control. But this cannot normally be done with System tapes, as the SYSTEM command only loads tapes via the internal tape deck (Cassette # 1)

A similar problem occurs if you want to connect your System 80 to a low cost light pen designed for use with the TRS-80 (such as the X-3645). Such pens are designed to use the cassette recorder as a preamplifier; they plug into the recorder's MIC input. However, there is no MIC input provided for the System 80's inbuilt cassette deck.

The answer is to use an external recorder and plug the light pen into it. However the software normally supplied with the light pens is designed for a standard TRS-80, and accordingly it expects the pen to be connected to "Cassette #1". Although the software can be modified, this can be tedious and time consuming especially with machine language programs.

A better way of overcoming both of the above problems is to fit a simple switch to allow the internal cassette deck to be optionally disabled, and its functions transferred entirely to an external recorder. This effectively converts the System 80 cassette circuit into an exact replica of that in the TRS-80.

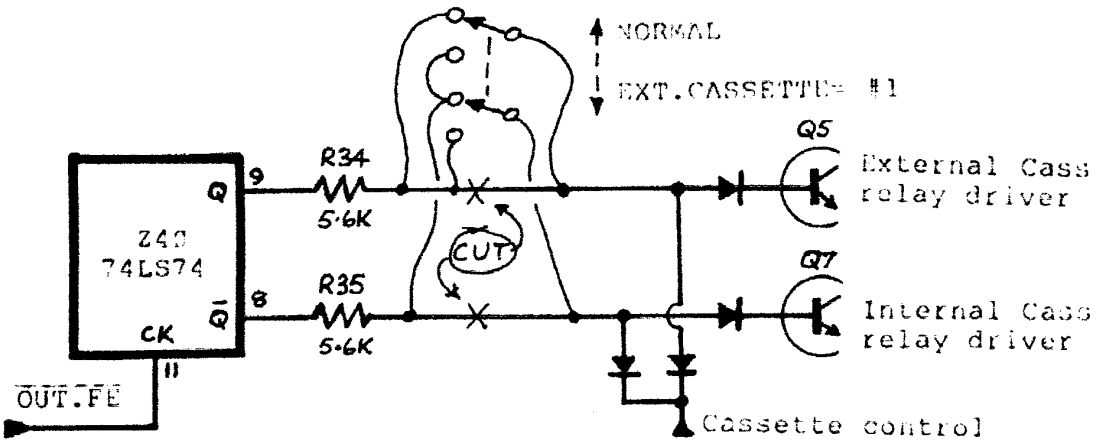
Basically, the System 80's cassette I/O circuit is exactly like that of the TRS-80 in that all data and control is transferred via I/O port address FF Hex (255 decimal). However because the System 80 has provision for two cassette recorders, additional circuitry has been added to allow connection of either one cassette or the other to the I/O circuitry.

The additional circuitry consists of a latch flip-flop provided with decoding so that it effectively resides at a second I/O address FE Hex (or 254 decimal). Each cassette recorder circuit is controlled by a small relay, and the relay driver circuits are enabled by the two outputs (Q and $\overline{Q}$) of the latch flip-flop. If Hex 10 (decimal 16) is fed to I/O port FE the latch flip-flop is set, enabling the "cassette #2" relay driver and allowing the external recorder to respond to normal tape communication via port FF. At the same

time the cassette #1 relay driver is disabled, preventing that recorder from responding. Conversely if Hex 00 (Decimal 0) is fed to I/O port FE, the latch flip-flop is reset, disabling the cassette #2 driver and enabling that for cassette #1. This is the normal circuit condition, with the internal cassette deck enabled.

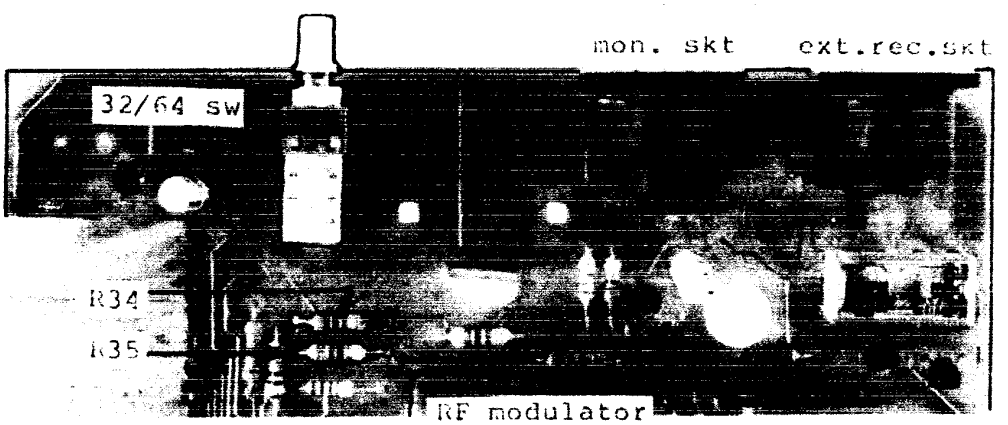
To enable the external recorder to be used instead of the internal deck, without software changes, all that is required is the addition of a DPDT switch to allow optional disabling of the cassette #1 relay driver, and connection of the other driver to the Q-bar latch output instead of the Q output. This makes the external recorder become cassette #1 as far as the software is concerned.

In schematic form the changes look like this:



Mechanically the mod is easiest done by lifting one end of the series resistors, R34 and R35 from the PC board. Four wires can then be run to a small slider, toggle or push button switch.

R34 and R35 are easy to find: they are on top of the System 80's interface PC board, at the rear end and just to the front of the push button switch for 32/64 character line selection. The resistor for the external cassette drive, R34, is nearest the switch.



Probably the easiest place to fit the extra switch is on the lower back of the case, below the space between the 32/64 character button switch and the video output socket. Quite short wires can then be used to connect it to the resistors and PC board.

Don't forget the link between the switch contacts.

1.9.3 Length of BASIC Statement Lines

As with the TRS-80, BASIC statement lines for the System 80 may by up to 255 characters long (total length including the line number). However in exactly the same fashion as the TRS-80, the System 80 will only allow you to key in up to 240 characters in the normal entry mode. This is normally far more than is needed. However if you really must have a line of the full 255 characters, you have to go to EDIT mode and use the "X" command to add the remaining 15 characters.

1.9.4 Key Top Legends

The following points should be noted about the legends used on the System 80 key tops.

a) The NEWLINE key is functionally identical to the ENTER key on a TRS-80.

b) The BACKSPACE key is identical to the "Back Arrow" (←) key.

c) The CTRL key is identical to the "Down Arrow" (↓) key.

d) The ESC key is identical to the "Up Arrow" (↑).

e) Although the "at" sign (@) shows a "backslash" sign as its shift mode character, this character is not available. Pressing the key with the shift key held down still gives the @ character. This is exactly the same as the TRS-80.

1.9.5 VAL String Functions

If the BASIC string function VAL is used with an argument in which the number part of the string is followed by a percent sign (%), the System 80's Level II interpreter will throw out the statement with an ?SN ERROR. This is also exactly the same as the TRS-80. The remedy is not to use a percent sign.

1.10 Differences Between TRS-80 and System 80

There are a number of small hardware differences between the Dick Smith System 80 computer and the Tandy TRS-80 Model 1, Level 2 computer that affects software compatibility.

It is important to realize however, that in general the hardware differences do not affect programs written in BASIC language, because in each machine the BASIC interpreter program built into the machines ROM is designed to suit the machine's hardware. Many machine language programs are also unaffected, either because the differences are not relevant or because the programs "call" driver routines in the BASIC ROM to communicate with the hardware. The only programs that are affected are those which use their own driver routines, and the routines are designed to communicate specifically with the hardware of one machine or the other.

1.10.1 Cassette Interface

The System 80 has a cassette deck built into the basic machine, as well as a socket for a second external recorder. It has circuitry inbuilt to allow software selection of recorders, whereas in the TRS-80 selection circuitry is provided only in the expansion interface. Because of this, programs that use the cassette port (either for communication with a cassette, or for operation of a light pen, sound effects unit etc), if they are written for the TRS-80, may not run properly on a System 80 without modification.

The cassette interface on both machines uses I/O address FF(H) as its data port, with bits B0 and B1 for the data itself. However the machines differ slightly in their use of bit B2, in the TRS-80 this is used solely for cassette motor control, whereas in the System 80 it is also used to enable data paths to both recorders. Unless this bit is set HIGH (B2=1) in a System 80, no output data can pass from the computer to the external recorder socket, and no input data can pass from the internal deck to the computer. Note that this bit must be set HIGH each time output data is fed to port FF.

The two machines also differ in the address used to perform software switching between the two recorders. In the System 80, the switching is done by a latch at I/O address FE(H), and specifically by bit B4 at that address. The corresponding latch in the TRS-80 Expansion Interface is at memory address 37E4(H), and responds to bit B0. In both cases setting the bit LOW corresponds to cassette #1, and setting it HIGH corresponds to cassette #2.

1.10.2 Printer interface

Both machines allow for a printer. However the printer port in the System 80 uses I/O address FD(H), whereas the TRS-80 uses memory address 37E8(H). This does not affect the BASIC command LLIST, or the statement LPRINT, or machine language programs that utilise the BASIC Interpreter's printer routine (like Microsoft's Editor/Assembler Plus). But it does affect programs having their own printer driver, like Tandy's Editor/Assembler and Word Processor.

Note however, that the System 80 Expansion Unit gives the user a choice of placing either the Centronics type parallel port or the RS-232C serial port at the printer address FD(H). This allows the use of a teleprinter in place of a parallel printer.

1.10.3 Serial Interface

The two machines differ here again in terms of the ports used for data and UART/terminal status interfacing. In the System 80, I/O addresses F8(H) and F9(H) are used, whereas the TRS-80 uses memory addresses 37DE(H) and 37DF(H).

With the System 80, output data to the UART is written to port F9(H), while input data from the UART is read from port F8(H). Conversely, output status control information is written to port F8(H) while input status information is read from port F9(H). In the TRS-80, address 37DF(H) is used for both input and output of data, while address 37DE(H) is used for input and output of status information.

1.10.4 Keyboard Differences

Early models of the System 80 as supplied do not provide two keys present on the TRS-80: the "Right Arrow" and "Clear" key, calling for either changes to the programs or addition of one or both keys.

1.10.5 Video Display of "Arrow" Keys

As explained overleaf there is a difference between the two machines in the video display of ASCII codes 91, 92, 93 and 94 (decimal). The System 80 displays the normal ASCII characters corresponding to these codes ("[","\", "^" and "]") whereas many, but not all, TRS-80 machines display four "Arrow" symbols (" ↑ "," ↓ "," → " and " ← ") to match their arrow keys. Note that some early TRS-80s do display the square opening bracket "[" for code 91, instead of the upward arrow.

1.11 SYSTEM 80 VIDEO DISPLAY CODES

1.11.1 Graphics Codes 128-191 (80-BF Hex)

There is no difference between the System 80 and the TRS-80 Level II in terms of the graphics characters displayed on the video screen for ASCII Codes 128-191 inclusive. To emphasize this and for reference, a full listing of these graphics characters is attached.

1.11.2 Space Compression Codes 192-255 (C0-FF Hex)

As with the TRS-80, the System 80 uses the codes 192-255 for space compression or horizontal tabulation. So in both cases, these codes give from 0 to 63 spaces: 192 gives no space, 193 gives one space, 194 gives 2 spaces and so on, up to code 255 which gives 63 spaces.

But Note: that these codes have this effect only when used in a PRINTCHR$(N) statement or command. When used in a direct POKE A,N statement to screen RAM, the codes simply duplicate the graphics codes 128-191, ie code 192 gives the same graphics character as 128, 193 the same as 129 and so on.

1.11.3 Alphanumeric Codes 32-127 (20-7F Hex)

For codes 32-90 inclusive and code 95, the System 80 gives exactly the same alphanumeric character set as the TRS-80 machine. A listing is attached. However for codes 91, 92, 93 and 94 the System 80 follows standard ASCII code rather than display the special ARROW characters displayed by the TRS-80 (although some TRS-80s also display the standard "square opening bracket" character for code 91).

Codes 96-127 are used for producing the normal lower case alphabetic characters with a printer. However it should be noted that if these codes are fed to the video display, the lower case characters are not generated. The characters which are displayed will depend again upon whether you used a PRINTCHR$(N) or a POKE A,N statement.

If your machine is not fitted with lower case software and hardware and you use a PRINTCHR$(N) statement or command, the code will duplicate the upper-case alpha codes 64-95. But if you use a POKE A,N statement or command, the codes will generate the punctuation and numeric codes 32-63 as shown in the third attached listing.

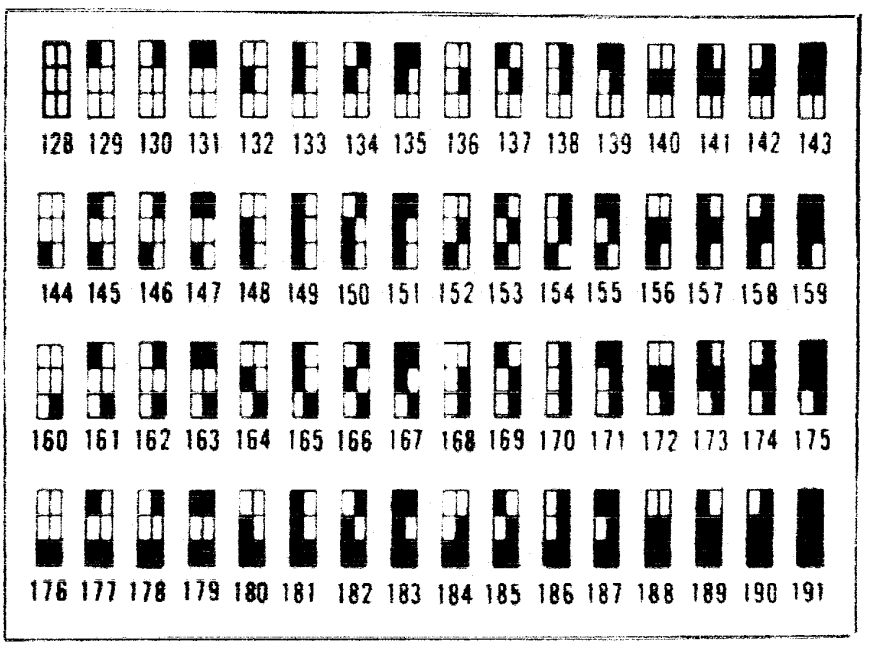
These codes may now be used flexibly now that you know what the results will do.

1.11.4 Control Codes 0-31 (00-1F Hex)

As explained in the System 80 manual, these produce exactly the same results as for the TRS-80. Note, however that codes 10-13 inclusive all produce a carriage return/line feed combination on the video screen (even though codes 11 and 12 control TOF functions on a printer.

Note also that the System 80's "32 character/line" mode, as produced by a PRINTCHR$(23) statement, is not identical with that on a TRS-80. In the System 80 this mode simply causes any new characters added to the screen RAM to be separated by single spaces. They remain normal width, not double width as with the TRS-80. Reversion to normal 64 characters/line mode will occur upon resetting, execution of a CLS command or statement, or execution of a PRINTCHR$(28) command or statement.

System 80 Computer – ASCII codes 128-191



SYSTEM 80 COMPUTER -- ASCII CODES 32-127 AS DISPLAYED ON VIDEO SCREEN:

CODE	CHARACTER	CODE	CHARACTER	CODE	CHARACTER
32		64	@	96	
33	!	65	A	97	!
34	"	66	B	98	"
35	#	67	C	99	#
36	$	68	D	100	$
37	%	69	E	101	%
38	&	70	F	102	&
39	'	71	G	103	'
40	(	72	H	104	(
41	)	73	I	105	)
42	*	74	J	106	*
43	+	75	K	107	+
44	,	76	L	108	,
45	-	77	M	109	-
46	.	78	N	110	.
47	/	79	O	111	/
48	0	80	P	112	0
49	1	81	Q	113	1
50	2	82	R	114	2
51	3	83	S	115	3
52	4	84	T	116	4
53	5	85	U	117	5
54	6	86	V	118	6
55	7	87	W	119	7
56	8	88	X	120	8
57	9	89	Y	121	9
58	:	90	Z	122	:
59	;	91	[	123	;
60	<	92	\	124	<
61	=	93	]	125	=
62	>	94	^	126	>
63	?	95	_	127	?

SYSTEM 80 COMPUTER -- ASCII CODES 32-127 AS PRINTED:

CODE	CHARACTER	CODE	CHARACTER	CODE	CHARACTER
32		64	@	96	`
33	!	65	A	97	a
34	"	66	B	98	b
35	#	67	C	99	c
36	$	68	D	100	d
37	%	69	E	101	e
38	&	70	F	102	f
39	'	71	G	103	g
40	(	72	H	104	h
41	)	73	I	105	i
42	*	74	J	106	j
43	+	75	K	107	k
44	,	76	L	108	l
45	-	77	M	109	m
46	.	78	N	110	n
47	/	79	O	111	o
48	0	80	P	112	p
49	1	81	Q	113	q
50	2	82	R	114	r
51	3	83	S	115	s
52	4	84	T	116	t
53	5	85	U	117	u
54	6	86	V	118	v
55	7	87	W	119	w
56	8	88	X	120	x
57	9	89	Y	121	y
58	:	90	Z	122	z
59	;	91	[	123	{
60	<	92	\	124	|
61	=	93	]	125	}
62	>	94	^	126	~
63	?	95	_	127	

1.12 System 80 Memory Map and I/O Map

Presented here is a map showing most of the important Memory and I/O space addresses for the System 80 Computer. Both decimal and hexadecimal addresses are given for your convenience.

Address		Significance
Decimal	Hexadecimal	
0	0000	Start of Level II BASIC ROM
12287	2FFF	End of ROM space
12288-13823	3000-35FF	Custom EPROM (if Fitted)
13824-14303	3600-37DF	Unoccupied
14304	37E0	Interrupt Latch Address
14305	37E1	Disk Drive Select Latch Address
14316	37EC	Disk Controller Address
14336-15359	3800-3BFF	Keyboard Matrix Addresses
15360-16383	3C00-3FFF	Video Refresh Memory
16384-16402	4000-4012	Start of RAM – RST Vectors
16405	4015	Keyboard device control block. 4016/7 are used to store the calling address of the keyboard driver routine.
16413	401D	Video display block. 401E/F are used to store the calling address of video driver routine. 4020/1 to store the cursor position.
16421	4025	Line printer control block. 4026/7 are used to store the calling address of the printer driver routine. 4028 to store the lines/page and 4029 the number of lines printed on the current page.
16464	4050	Disk Controller Interrupt Vector
16466	4052	Communications Interrupt Vector
16548-16549	40A4-40A5	Pointer to start of BASIC program
16561-16562	40B1-40B2	Pointer to top of BASIC memory

16598-16599	40D6-40D7	Memory size stored here
16607-16608	40DF-40E0	Pointer for entry address for SYSTEM programs
16620-16621	40EC-40ED	EDIT line number
16629-16630	40F5-40F6	Last line number executed
16637-16638	40FD-40FE	Free space size
16870-17127	41E6-41E7	I/O buffer area
17128	42E8	Always zero
17129	42E9	Normal start of a BASIC program. Text is stored first, then simple variables and arrays String space and stack are stored down-wards from the top of memory, or from the bottom of any space at the top[of memory which has been reserv3ed for machine language routines.
20479	4FFF	End of 4K RAM
32767	7FFF	End of 16K RAM
49151	8FFF	End of 32K RAM
65535	FFFF	End of 48K RAM

I/O Addresses

248	F8	RS-232 port (data in/status out)
249	F9	RS-232 port (data out/status in)
253	FD	Printer port address
254	FE	Int/Ext cassette latch (bit 4)
255	FF	Cassette data port

HEX-TO-DECIMAL CONVERSION CHART

HEX CODE	Most Significant Bytes		Least Significant Bytes	
	IV	III	II	I
0	0	0	0	0
1	4096	256	16	1
2	8192	512	32	2
3	12288	768	48	3
4	16384	1024	64	4
5	20480	1280	80	5
6	24576	1536	96	6
7	28672	1792	112	7
8	32768	2048	128	8
9	36864	2304	144	9
A	40960	2560	160	10
B	45056	2816	176	11
C	49152	3072	192	12
D	53348	3328	208	13
E	57344	3584	224	14
F	61440	3840	240	15

For each hexadecimal digit, go down the hex code column at the left until you find the right digit. Then move across to the right column. When all four digits have been converted into their decimal equivalents I, II, III, IV, add these all together to get the final answer. I.e.,

Decimal Value = IV + III + II + I

2.0 TROUBLE SHOOTING

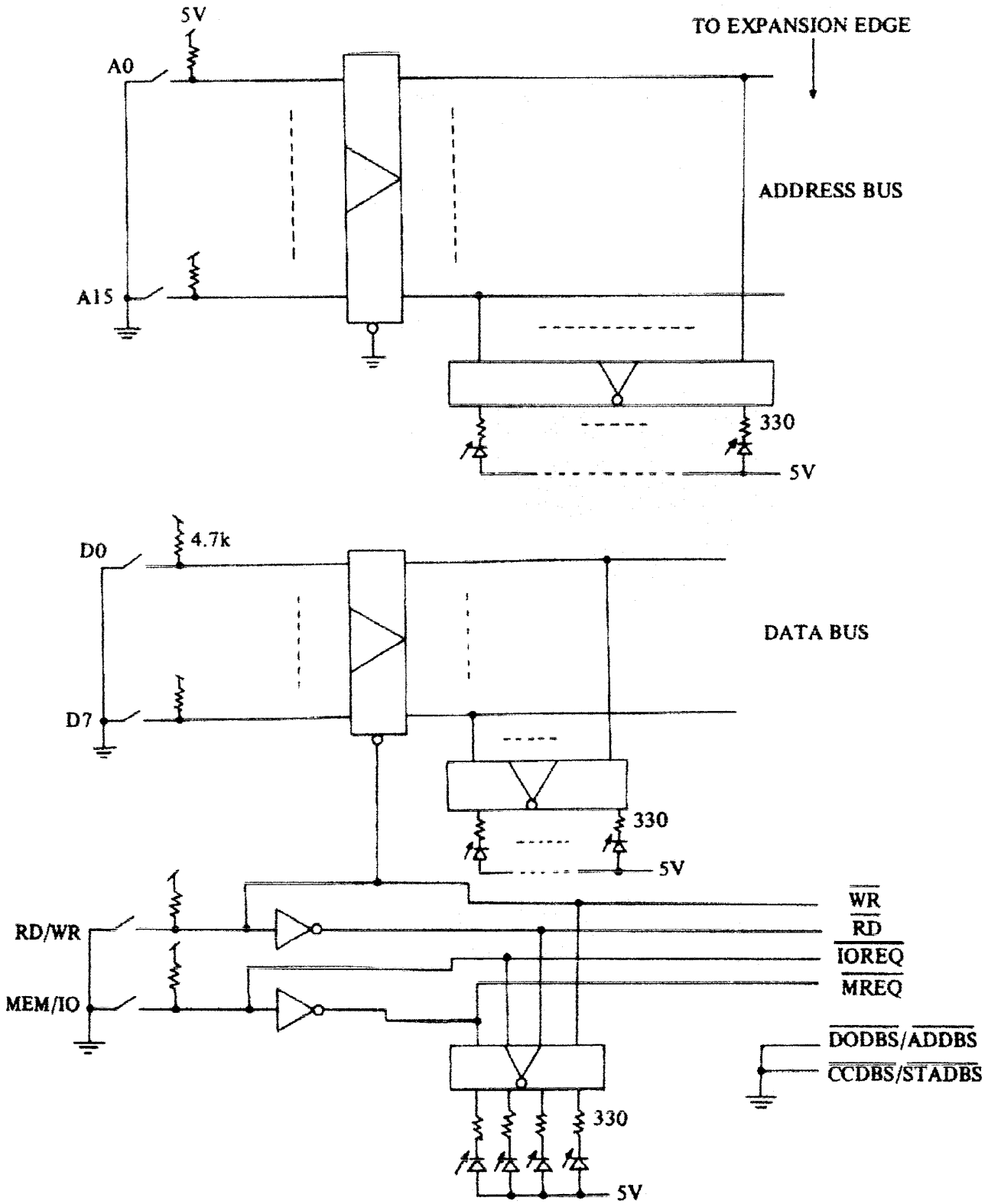
2.1 Introduction

Three common types of fault are: Component failure, open circuit and short circuit. Since the System 80 has to pass a very strict quality checking procedure, a short circuit seldom occurs. Open circuit and failure of components are more common. These faults may be caused by shock during transportation or running the computer under adverse conditions (eg high temperature and high humidity).

2.2 Bus check – Data, Address and Control Buses

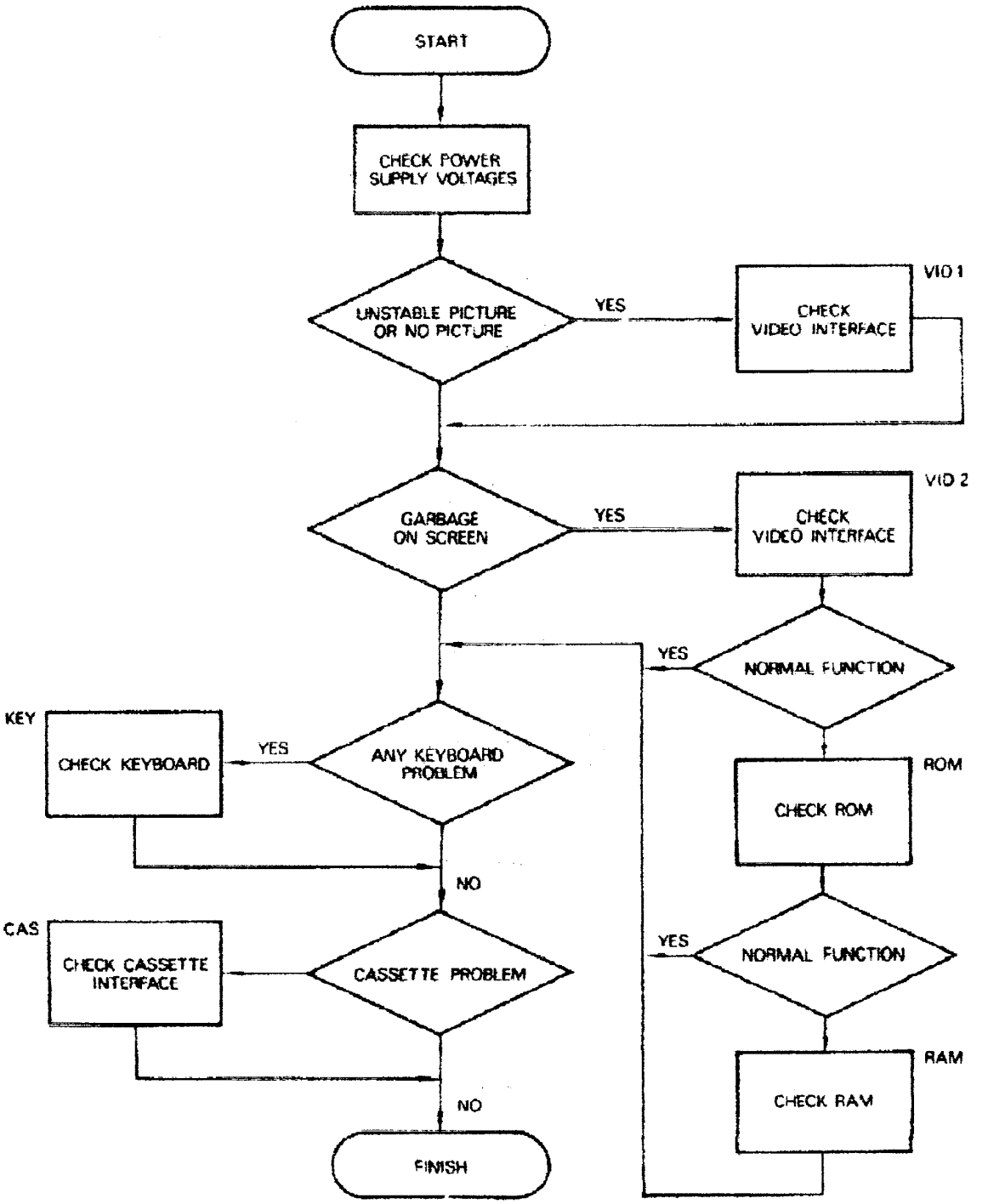
A bus check can be facilitated by a simple tester. It disables the CPU buffers and puts data, address and control signals on the buses. Therefore, short circuits and open circuits can be tested under static conditions.

Fig. 2.1 TESTER CIRCUIT DIAGRAM



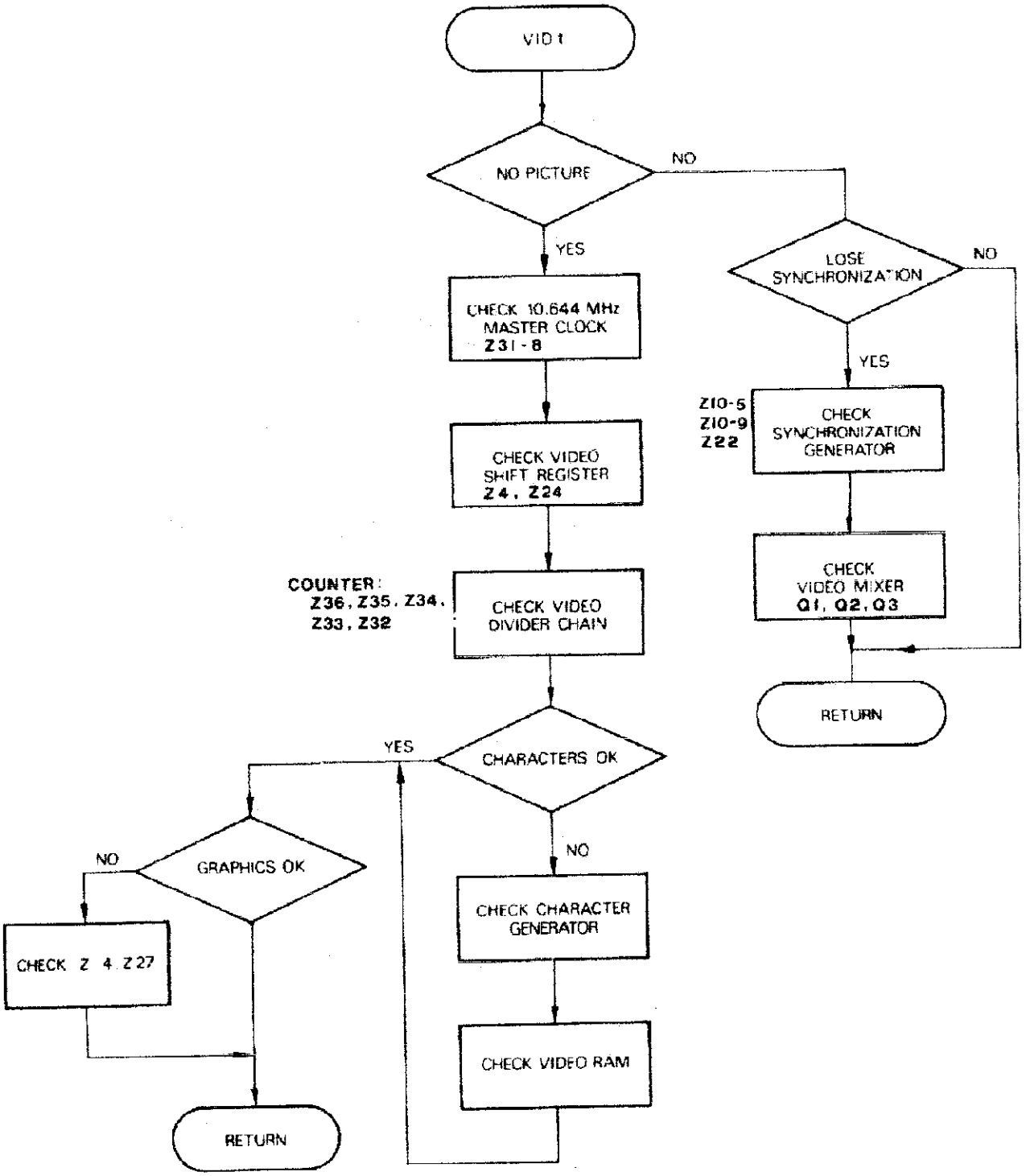
2.3 Trouble Shooting Flowcharts

General Flowchart In Trouble Shooting

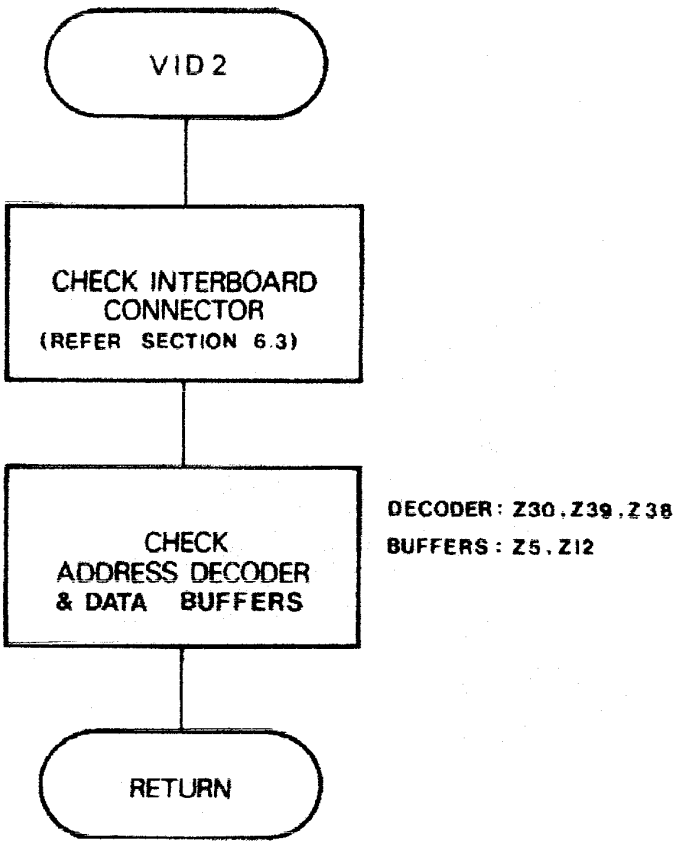


2.3.1 Video Interface

Interface Board



Interface Board



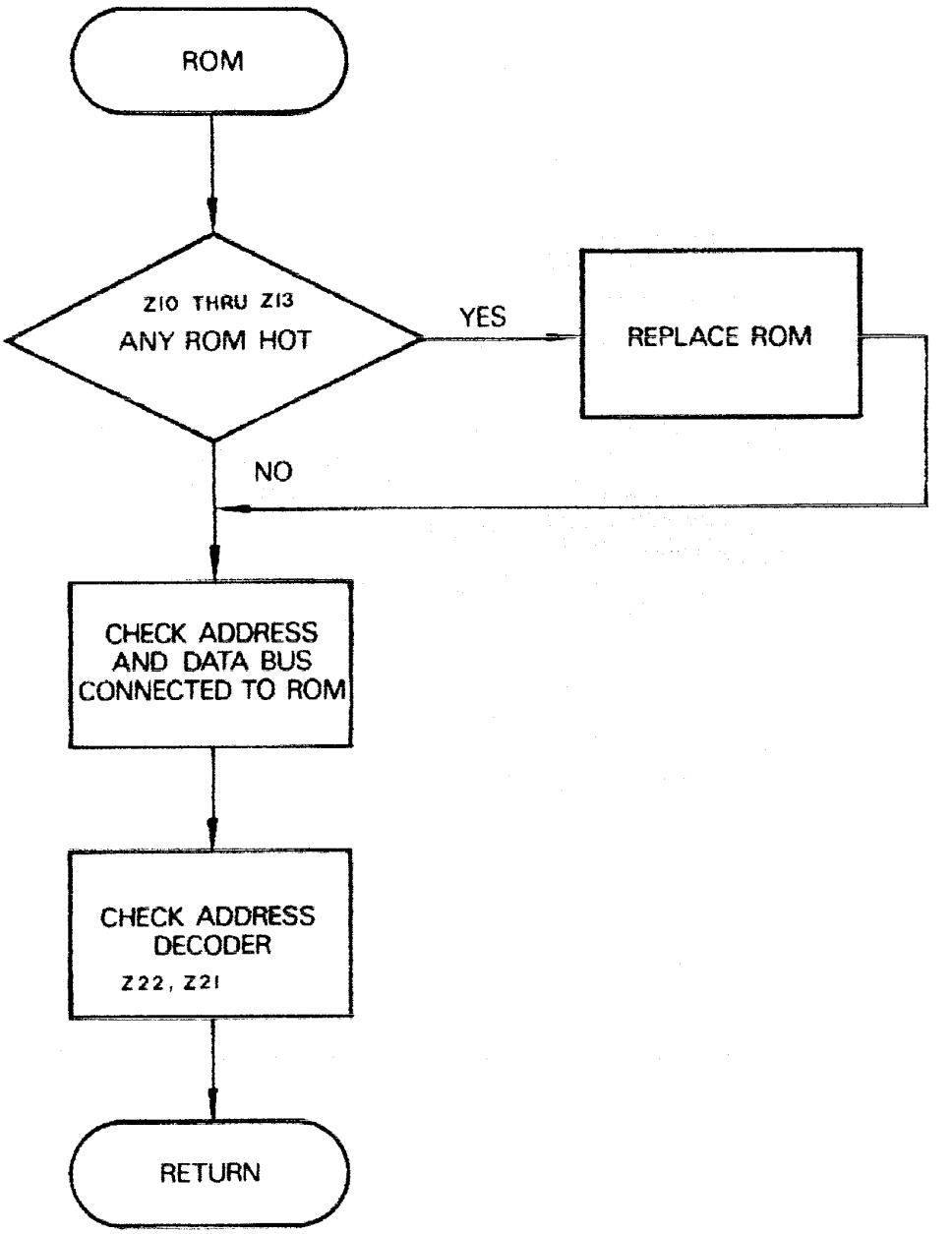
Remarks:

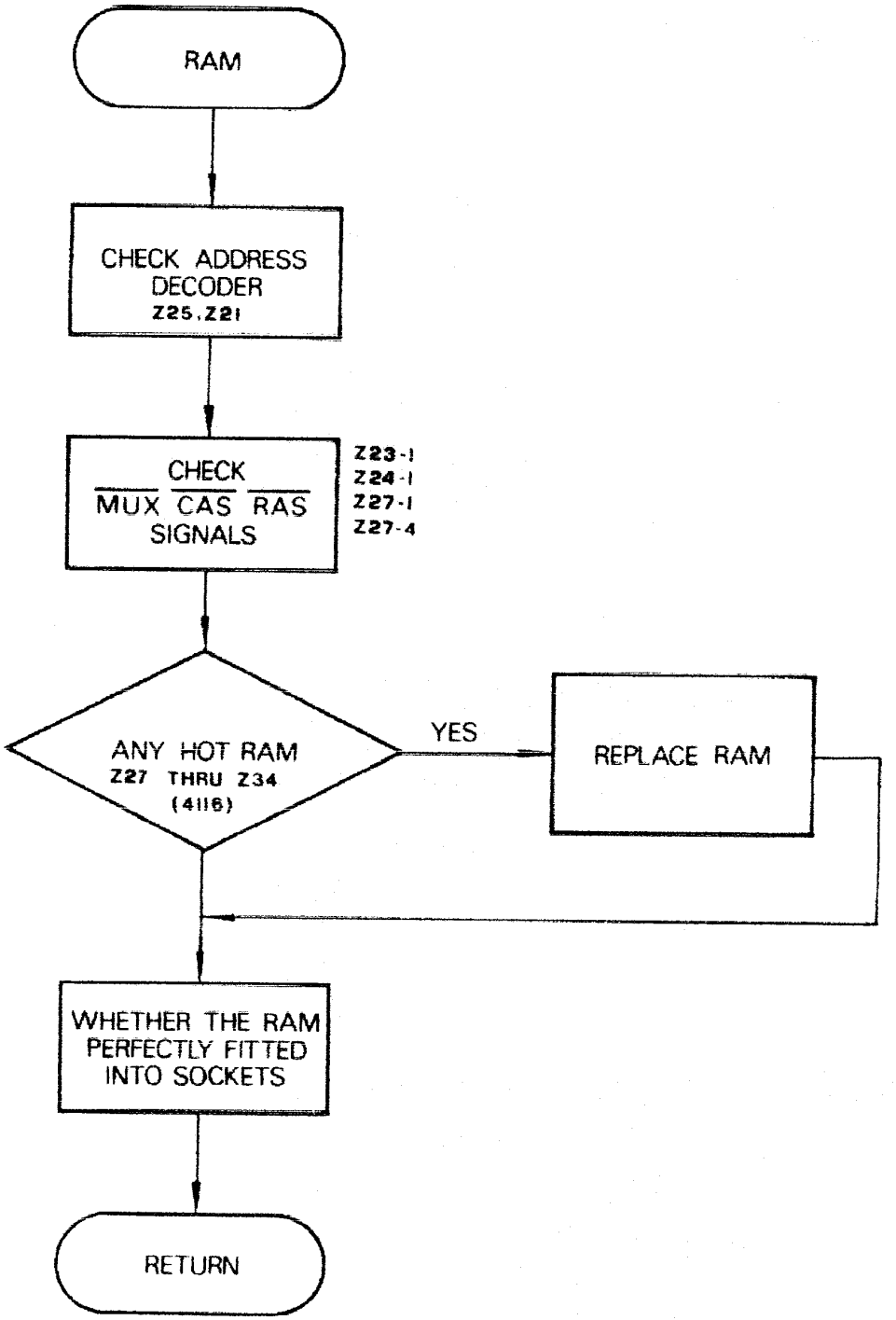
1) A system that mis-spells words usually has data errors in the video RAM, or the data input to the character generator is being grabbed by a defect around latch Z26

2) If the display oscillates up and down it may be due to low supply voltage, See whether there is any ripple at the +5V supply.

2.3.2 System ROM

CPU Board

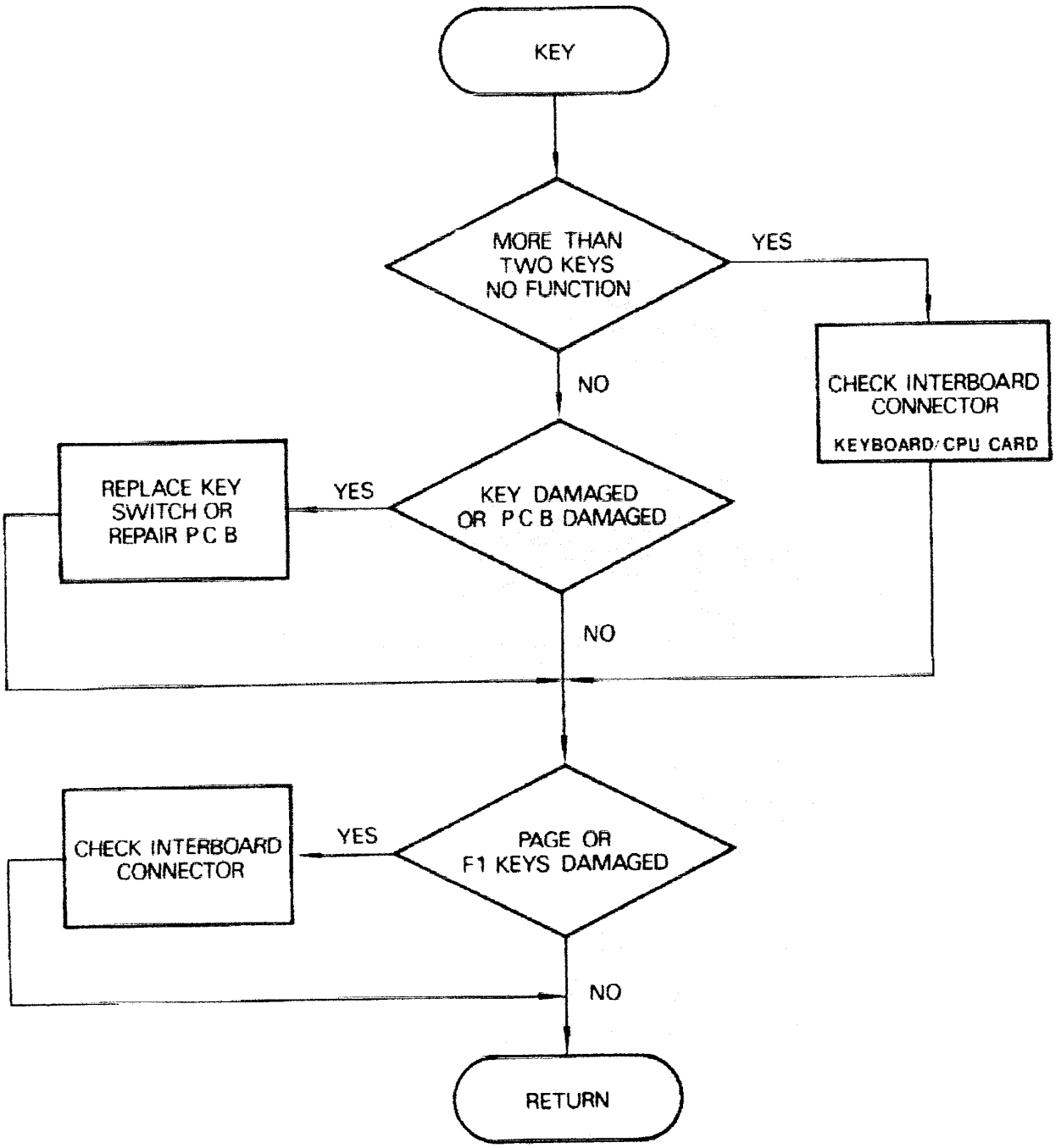




Remarks:

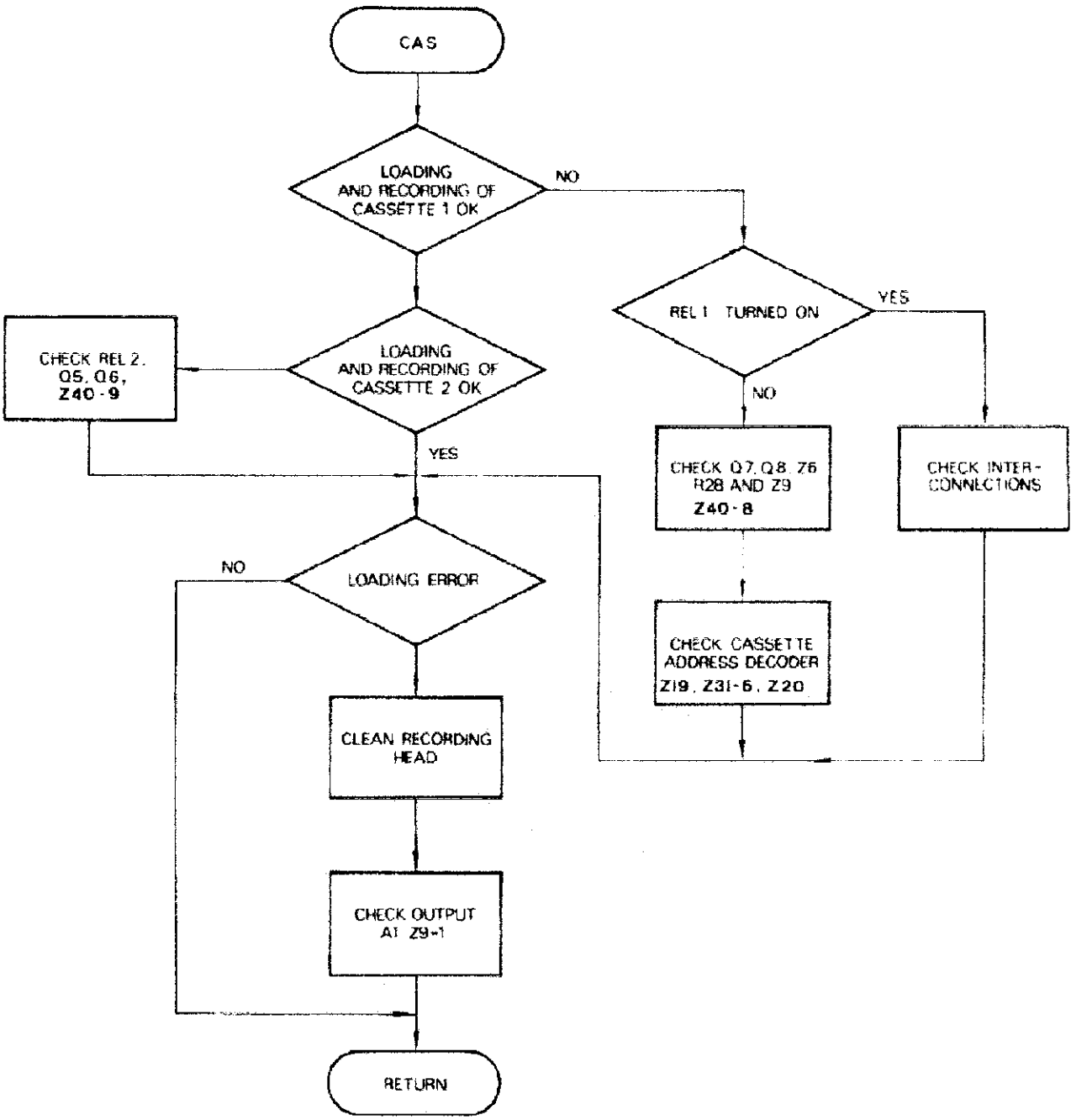
The flow charts of RAM and ROM checking seem quite simple, but actually it is most difficult to determine whether a component is damaged. The best way to check these sections is to replace the RAM or ROM with good chips if other sections of the circuits are working normally. **Caution:** CPU, ROM and RAM chips should be placed on conductive material after removing from the circuit.

2.3.4 Keyboard



2.3.5 Cassette Interface

Interface Board



Remarks:

Sometimes cassette loading errors may not be caused by circuit faults, but due to poor quality cassette tapes.

3.0 Trouble Shooting Hints

3.1 Keyboard Malfunctions

Symptom: **Keyboard has bounce**

Fault: Incorrect typing style

Cure: Adjust typing technique to overcome bounce, generally your technique should be slower than that used on a conventional electric typewriter, due to the scan rate of the System 80 keyboard.

Fault: Keyswitch Bounce

Cure: Replace the offending keyswitch by removing the keyboard, desoldering the keyswitch and replacing with a new keyswitch.

Symptom: **Keyboard not operating.**

Fault: Keyboard connector dislodged.

Cure: Remove cover, re-insert ribbon cable into connector on keyboard. Ensure that no wires are bent or broken.

Symptom: **One key not working.**

Fault: Dry joint or broken track on keyboard.

Cure: Remove the cover and the 8 keyboard retaining screws, examine the circuit board under the faulty key, resolder and test for continuity and correct switch operation.

Symptom: **Several keys not operating on the keyboard.**

Fault: Ribbon connector with wire/s broken on circuit board due to fatigue.

Cure: Refer to circuit diagram. Keys will probably be related by either the horizontal or vertical matrix. Examine the ribbon connection on the CPU board and re-terminate any broken wires with a soldering iron. If this does not cure the problem, remove the keyboard and check for continuity along the copper tracks. Resolder any breaks or dry joints as necessary.

Fault: Ribbon cable not slotting into keyboard connector correctly.

Cure: Check that the cable is slotted into the keyboard.

3.2 Video Absent or Irregular

Symptom: **No video on the screen when used on TV monitor, power indicator on cassette working normally.**

Fault: Video cut switch and page key depressed, monitor displays RHS of screen only.

Cure: Check and put keys in appropriate settings.

Fault: Monitor at fault.

Cure: Try computer on another monitor or TV set.

Fault: Lead from computer to monitor plugged into tape instead of video or loosely fitted.

Cure: Check connections to TV and computer. Computer end of cable can be particularly hard to insert. Exchange components to isolate faulty component.

Fault: Video output transistor in computer faulty.

Cure: Remove cover from computer and locate Q3 on the circuit board. Q3 is the transistor closest to the 5 pin socket. Using a multimeter on the lowest OHMS scale, check the emitter to collector resistance of the transistor in both directions. If it appears to have low resistance (in the order of 30 Ohms) in both directions, then it is likely to be short circuited. This transistor can be readily replaced with a DS549 (Note pin orientation). The flat on the transistor will face the rear of the computer. If the computer is still faulty return the unit to your System 80 agent for repair.

Fault: Cable or RCA plug at fault.

Cure: Try another cable.

Symptom: **Video on the screen wavering in a slow snaking motion.**

Fault: Diodes in the power supply faulty.

Cure: Replace the two largest diodes in the power supply box with 1N5408 diodes.

Fault: Capacitor in the power supply faulty.

Cure: Replace 22000uF capacitor with a new one. Also check for broken tracks under capacitor. Secure the capacitor body to PC board with rubberized glue.

Fault: Monitor receiving magnetic interference from another appliance.

Cure: Remove monitor from influence of the other appliance.

Symptom: **No video LED, Indicator off.**

Fault: Power supply unplugged.

Cure: Ensure that the power supply is plugged into the mains socket properly. Remove the lid of the computer and ensure that the lead going from the power box to the CPU board is plugged in at both ends. Check for broken wires.

Fault: Power supply not operating.

Cure: Check fuse on rear of computer. Measure output of power supply for +8V, +16V and –16V with respect to ground. A handy grounding point is the negative side of the 22000uF electrolytic in the PSU. If any of these voltages are absent check the AC outputs of the two transformers. Replace if necessary. Also test the input voltages to the 7812 and the 7805 regulators.

Fault: Regulator/s Faulty.

Cure: Check the output voltage of the 7805 regulator on the CPU board. It should measure 5V. This is easiest to access by measuring across diode 3 on the CPU board. If there is no voltage or a lower voltage than 5V, suspect the regulator or a short circuit on the 5V rail. Isolate the output of the 7805 IC regulator from the rest of the circuit and measure the output voltage again. If the voltage is now 5V, then the fault is elsewhere in the circuit and the unit should be returned to your dealer.

3.3 Picture Position Adjustment

After the video interface has been serviced the picture position should be adjusted to position the picture in the middle of the screen. Enter and run the following simple program. A rectangle showing the screen boundary will be drawn. VR1 and VR2 should be adjusted with a non-metallic screwdriver.

```
10 CLS
20 FOR X=0 TO 127
30 SET(X,0):SET(X,47)
40 NEXT X
50 FOR Y=0 TO 47
60 SET(0,Y):SET(63,Y):SET(64,Y):SET(127,Y)
70 NEXT Y
75 PRINT @522,"LEFT";:PRINT @554,"RIGHT",
80 GOTO 20
90 END
```

3.4 Cassette Mechanism Not Working

Symptom: **Cassette light comes on but mechanism does not turn**

Fault: Cassette drive belt broken or run off flywheel or pulley.

Cure: Remove cassette mechanism and inspect the drive belt. Correct as necessary. If the mechanism appears to be OK turn the pulley or flywheel to check free movement of the mechanism. If mechanism is jammed manipulation should free it.

Fault: Power regulating transistor faulty.

Cure: Replace Q10 with a TIP31B transistor. Note that orientation of the new transistor is the same as the original.

Fault: Relay not operating or contracts faulty.

Cure: Replace relay as necessary.

3.5 Modifications to Improve Cassette Reliability

1) In some units Q9 on the interface board has been deleted and a wire link substituted between the collector and the emitter. This drops the output from the regulator Q10 by 1.5V. In these units change zener diode Z1 from 8.2V to 10V. This will improve cassette loading.

2) For optimum performance from the cassette loading circuitry, C1 (0.0047uF) on the cassette amplifier board (located below the cassette mechanism) must be changed to 0.047uF. In addition C5 (0.1uF) should be changed to 0.27uF.

Note: All Blue Label and some earlier models are factory fitted with the correct value components.

3.6 Cassette Loading Difficulties

Symptom: **Cassette not loading, asterisks staying on. (BASIC tapes only)**

Fault: Cassette volume set too high.

Cure: Reduce volume level and repeat loading procedure until volume setting causes asterisks to flash.

Fault: Cassette heads out of alignment.

Cure: Re-align heads by either method below.

a) Remove the computer lid and locate the green wire and its associated harness of red, black and yellow wires leading away from the cassette deck to the four-way connector on the Interface Board. Earth an

oscilloscope lead to the metal tab of the 7812 regulator and place the probe into the connector socket of the green wire. While monitoring the output waveform gently insert a small Phillips head screw driver into the left hand spring loaded screw fastening the cassette playback head. Applying minimal downwards pressure, slowly rotate the screw up and down until maximum amplitude is obtained on the oscilloscope. Once this has been achieved apply a small dab of nail polish to secure the head of the screw.

NOTE: Use a commercially recorded computer cassette to align heads, otherwise there will be great difficulty loading tapes not recorded on the computer.

b) Remove the lid from the computer. Insert and play a high quality, commercially recorded computer cassette in the deck. While monitoring the signal meter in the computer insert a small Phillips head screwdriver into the left hand spring loaded screw fastening the playback head. Adjust the screw, applying minimum downwards pressure, until maximum reading is obtained. Lock screw in position with a small dab of nail polish to prevent head from vibrating out of alignment.

Symptom: **Cassette not loading. Left hand asterisk changing into a "C" (System tapes only).**

Fault: Insufficient volume.

Cure: Increase volume level and reload so that asterisks flash normally.

Fault: Dirty or magnetized heads.

Cure: Gently clean the surface of the playback head with a cotton wool buds immersed in an alcohol solution. Demagnetize the playback head using a cassette demagnetizing tool.

Fault: Heads out of alignment.

Cure: Refer to method of aligning heads in Section 3.6.

Symptom: **Asterisks flash normally and program appears to load successfully until run. When run or listed, numerous errors are discovered in the program.**

Fault: Faulty cassette, either poorly saved or corrupted.

Cure: Try another pre-recorded cassette to determine where the fault lies, ie in the cassette or in the computer's cassette player.

Fault: Cassette playback head out of alignment.

Cure: Refer to method of aligning heads in Section 3.6

Symptom: **Cassette Loading Intermittent.**

Fault: Dry joint on cassette board.

Cure: Remove the computer lid and undo the five retaining screws holding the cassette deck and associated meter into the case. Unplug the cassette harness and turn the deck over to reveal the circuit board. Remove the two retaining screws and turn the board over – component side up. Check all component leads to ensure proper connection. Visually examine all leads connected to the board for short or open circuits. Turn the circuit board over and resolder any suspicious looking joints, reassemble and test. **NOTE:** Do not use excessive force to pull wires.

Fault: Alignment Problems.

Cure: Re-align heads as outlined in previous section – "Cassette loading but asterisks not flashing".

Fault: Capacitors Dry.

Cure: Intermittent loading may be due to dry electrolytrics in the cassette circuitry. Replacement of the following electrolytics in the cassette circuit will overcome the faults attributable to dry electrolytics. Replace C7, 10uF with a 47uF 16V electrolytic. **NOTE:** observe the correct polarity for electrolytics. Refer to manual if unsure.

Symptom: **Cassette loads but program will not run. If listed program lines are all rubbish.**

Cure: Reload the program and turn the volume on the cassette deck up one notch.

Symptom: **Information being displayed changes at random.** Similarly graphics characters appear at the bottom of the screen. Another symptom is that the READY display will change characters, ie. HEADY, PEADY, READ etc.

Fault: Screen RAM is faulty – these are either 21L02 or 2114's depending on your machine.

Cure: Remove cover and keyboard. Screen RAM IC's are located on the right hand side and are positioned in a vertical row. Rather than change all eight (21L02), try changing two at a time.

3.7 Screen Displaying "S's" and "@'s"

Symptom: **Computer shows "S's" and "@'s" on entire screen and will not clear.**

Fault: Faulty RAM

Cure: Check all RAM and determine whether any IC's are abnormally hot. Exchange RAM for new IC's to check if RAM is faulty. Use only prime 4116 type Dynamic RAM of 250 msec or faster access time. These are available at Dick Smith stores (Cat # 79310).

Fault: 12V supply rail faulty.

Cure: Check +12V rail on RAM IC's. Check +5V and –12V rails as well. Ensure that the 0.1uF bypass capacitors across the 12V rail of the memory IC's are not short circuited.

Fault: Fault somewhere other than RAM or CPU board.

Cure: Exchange ROM, if the fault still prevails return computer to supplier for servicing.

3.8 Screen Showing Garbage

Symptom: **Screen shows garbage at switch on and will not clear.**

Fault: Insufficient time given for power supply to discharge when computer was switched off.

Cure: Allow at least 30 Seconds after switching computer off.

Fault: Connection between CPU board and Interface board either broken or some wires unplugged.

Cure: Inspect the connector cables between CPU board. Resolder any broken terminations. Re-insert any unsocketed wires.

Fault: Faulty RAM, ROM or CPU.

Cure: Ensure all RAM, ROM and CPU IC's are properly inserted. Check that no pins are bent under the IC's. Methodically replace RAM, ROM and CPU. If the fault still persists we suggest you return the computer for service.

NOTE: In some cases it may be necessary to hold BREAK and press RESET together to reset the computer. If this happens when the computer is not connected to an Expansion Interface Unit then it is an indication that the data bus is being unduly loaded. To test this try reading from an unused address – eg PRINT PEEK(-16384). The result should always be 255 (0FFH), ie all data bits floating high.

3.9 Programs Being Corrupted

Symptom: **Computer continually corrupts certain program lines.**

Fault: RAM Faulty

Cure: Test RAM using Dick Smith RAM/Disk Diagnostic Tests (Cat # X-3763).

Fault: ROM Faulty

Cure: Exchange ROM and test.

Fault: CPU faulty.

Cure: Replace CPU and test.

Fault: Misloading of program.

Cure: See cassette loading errors section of manual.

Fault: Faulty Tapes.

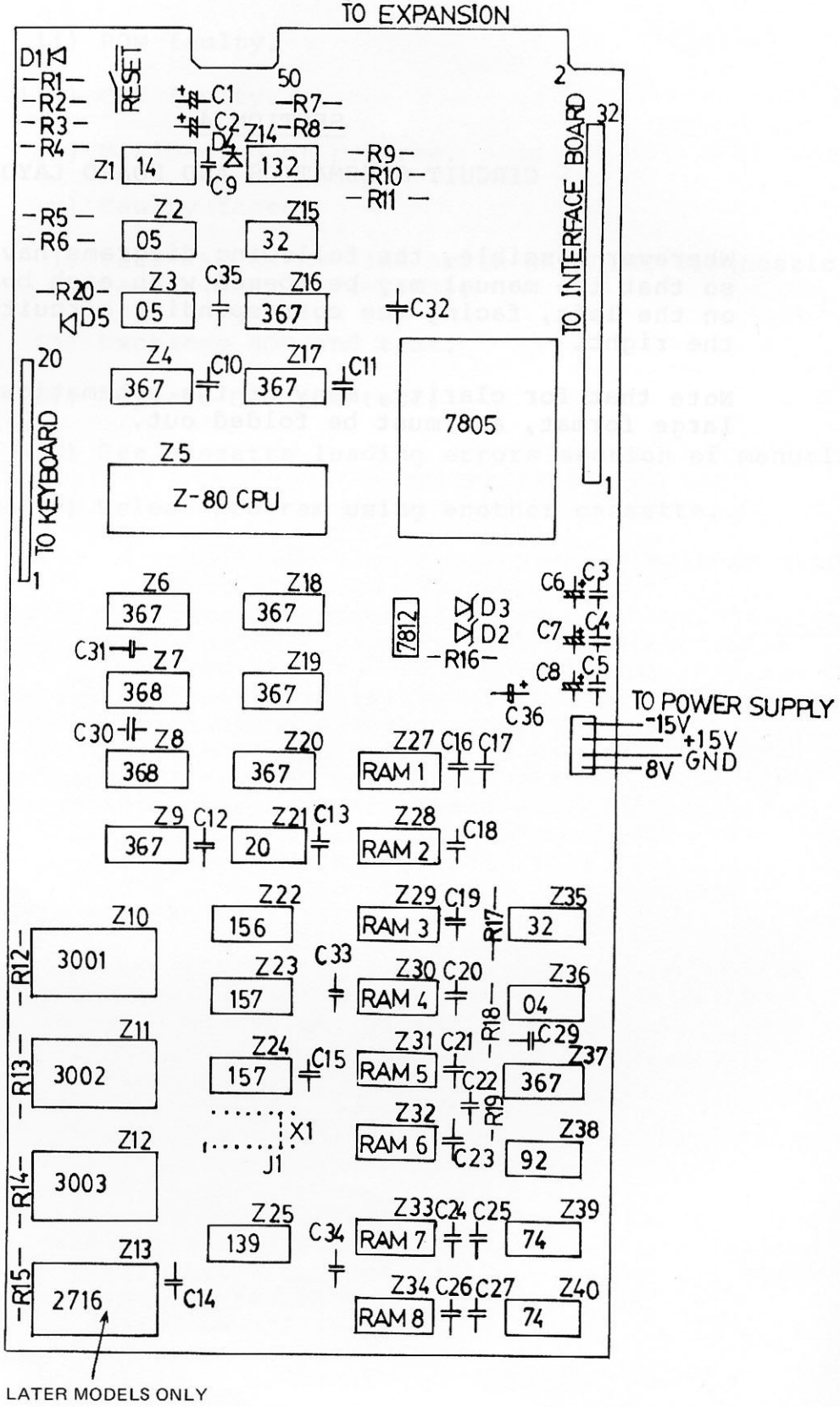
Cure: Reload program using another cassette.

4.0 CIRCUIT SCHEMATICS AND BOARD LAYOUTS

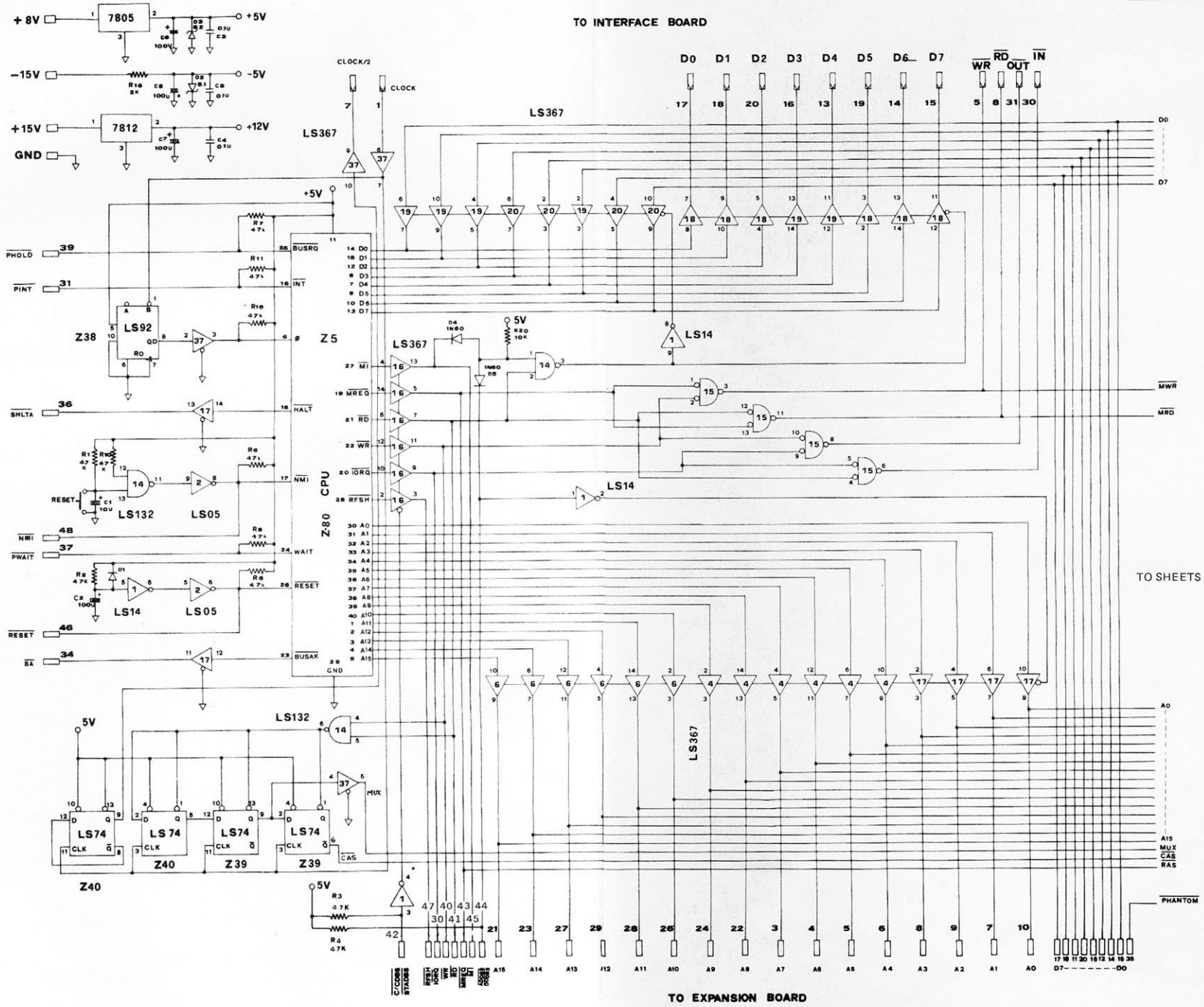
Wherever possible, the following diagrams have been positioned so that the manual may be opened with each board layout diagram on the left, facing the corresponding circuit schematic/s on the right.

NOTE: for clarity many of the schematics are reproduced in large format, and must be folded out.

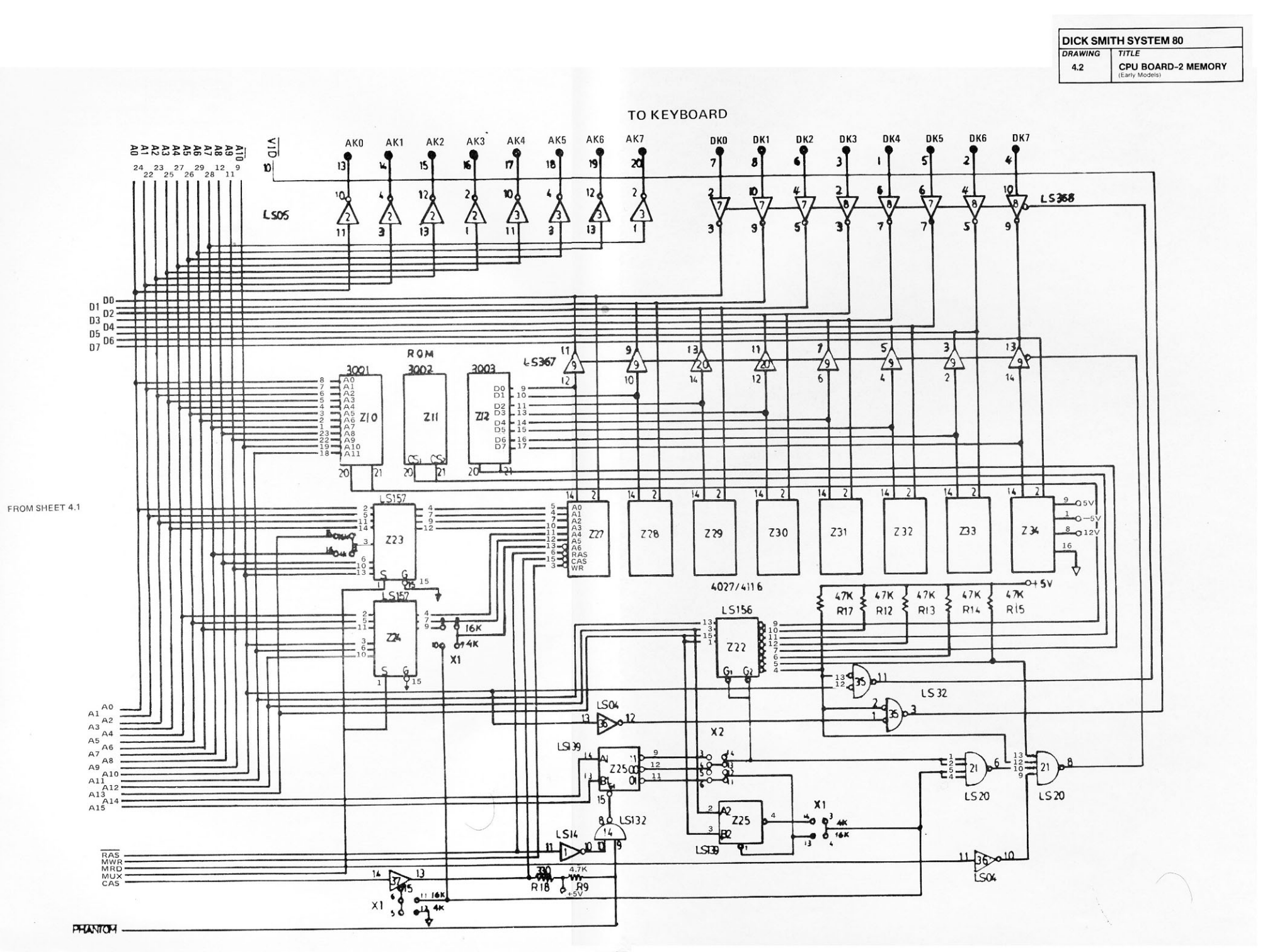
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.1	**CPU BOARD** (All Models)



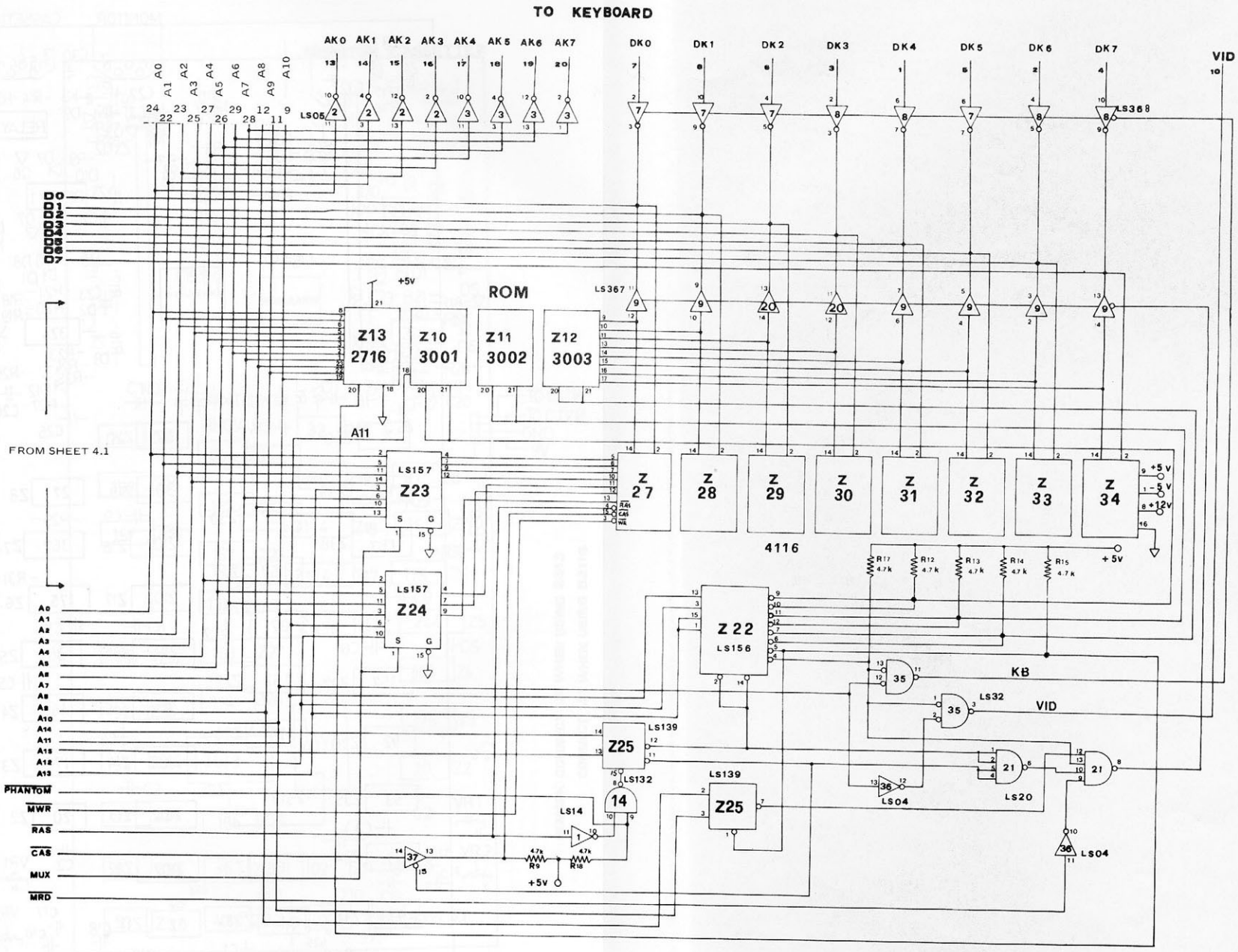
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.1	CPU BOARD (All Models)



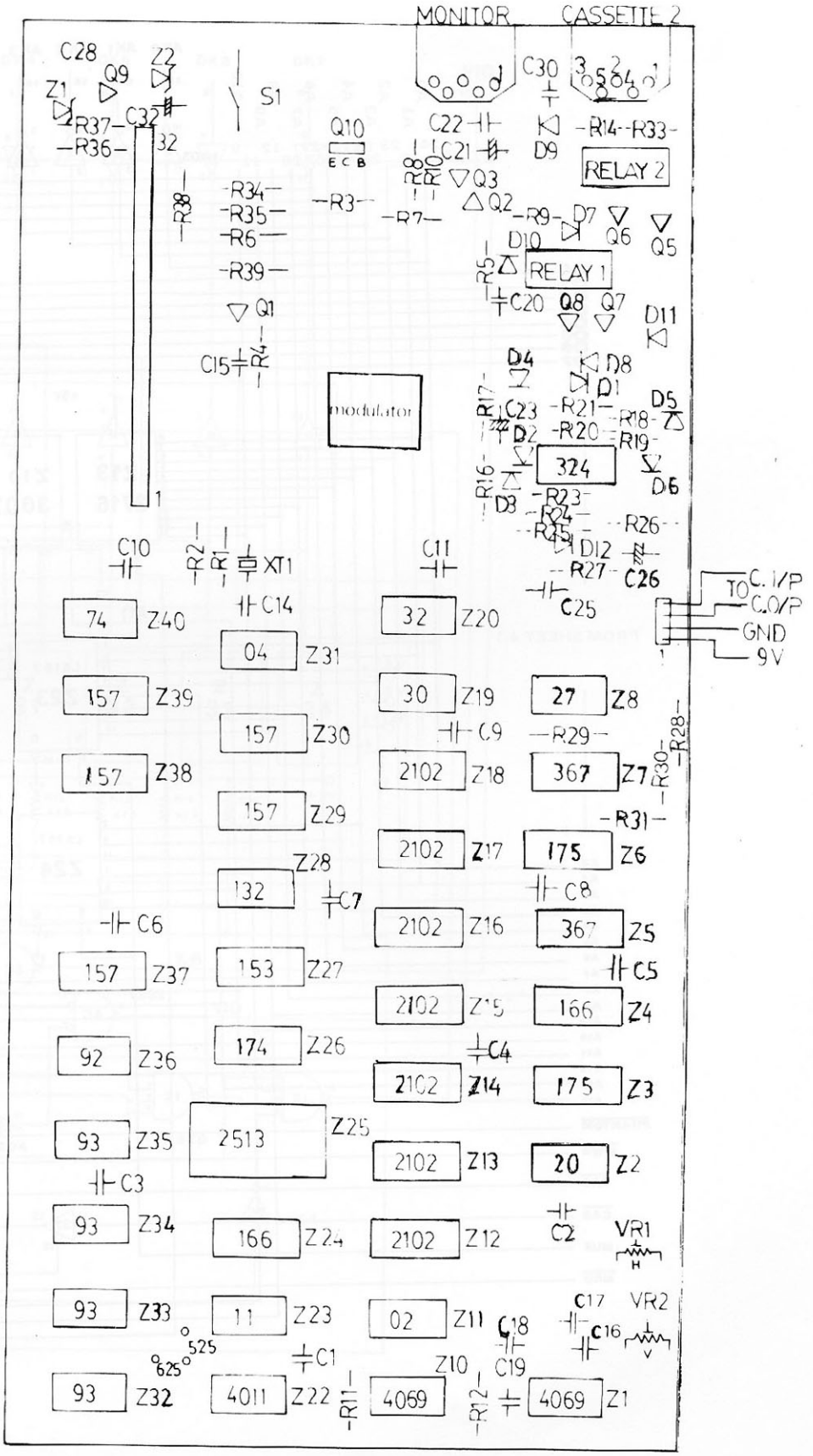
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.2	CPU BOARD-2 MEMORY (Early Models)



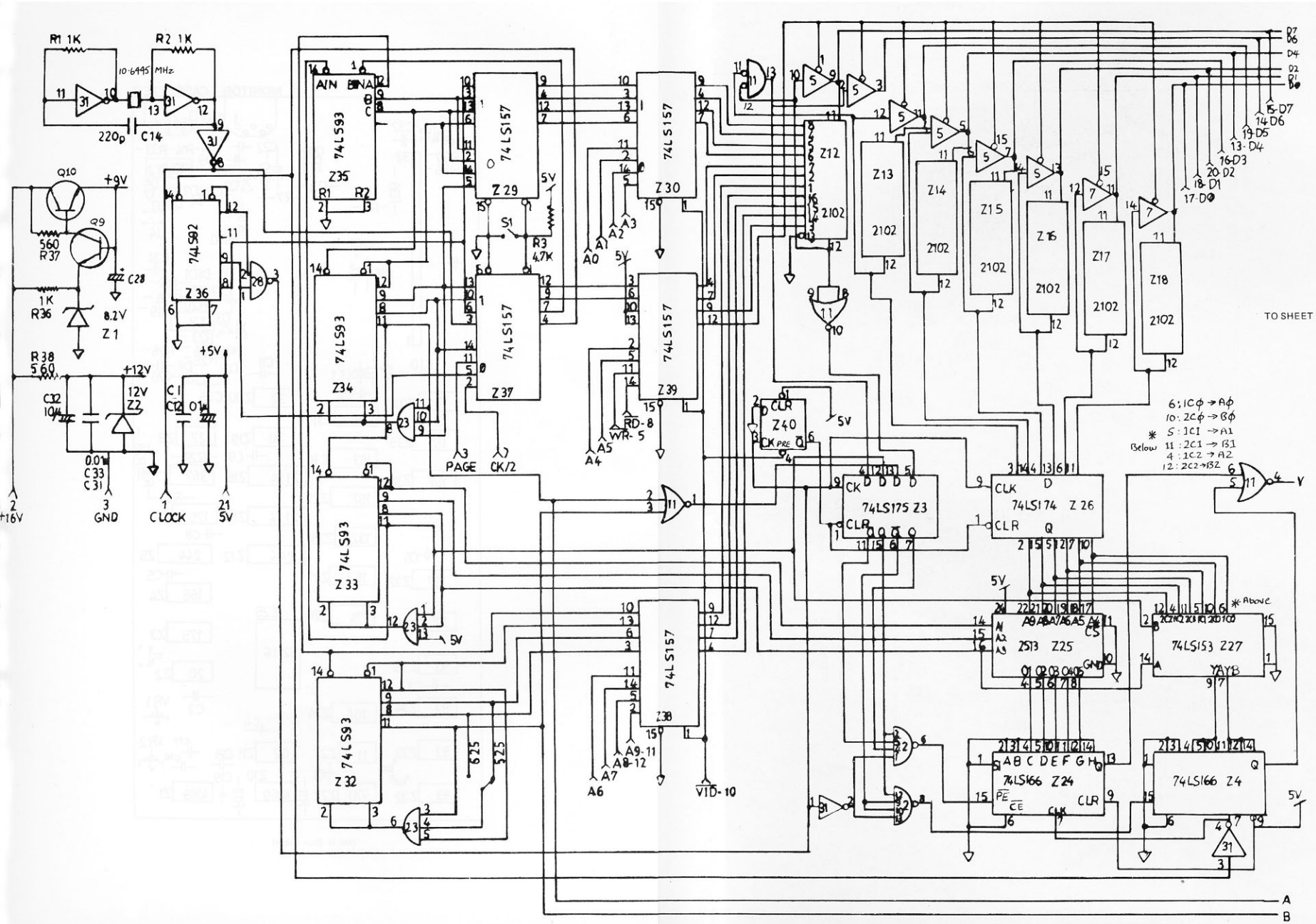
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.3	CPU BOARD-2 MEMORY (Mkll and Blue Label Series)



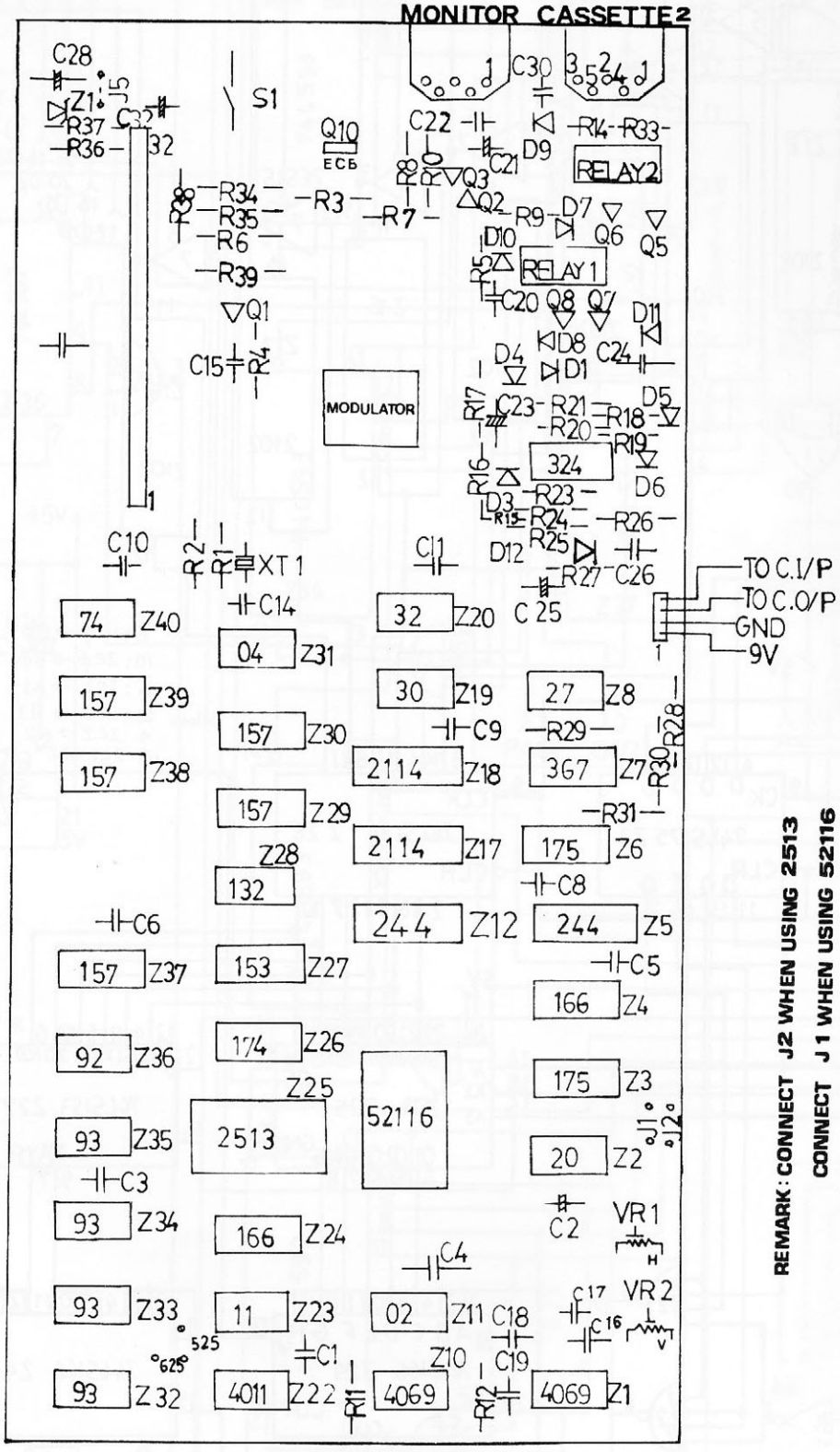
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.4	**VIDEO INTERFACE CARD** (Early Models)



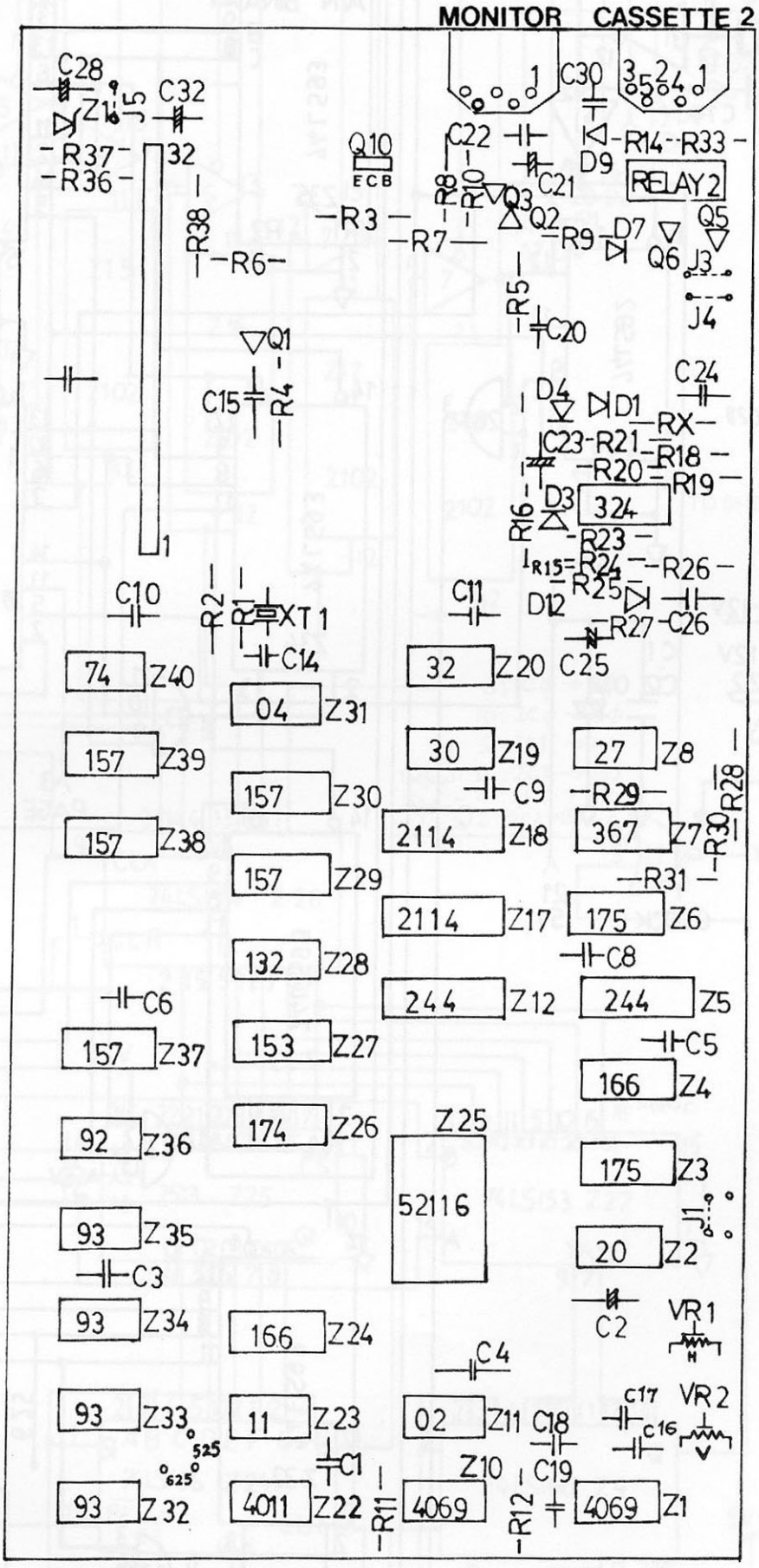
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.4	VIDEO INTERFACE CARD (Early Models)



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.5	**VIDEO INTERFACE CARD** (Blue Label Series)

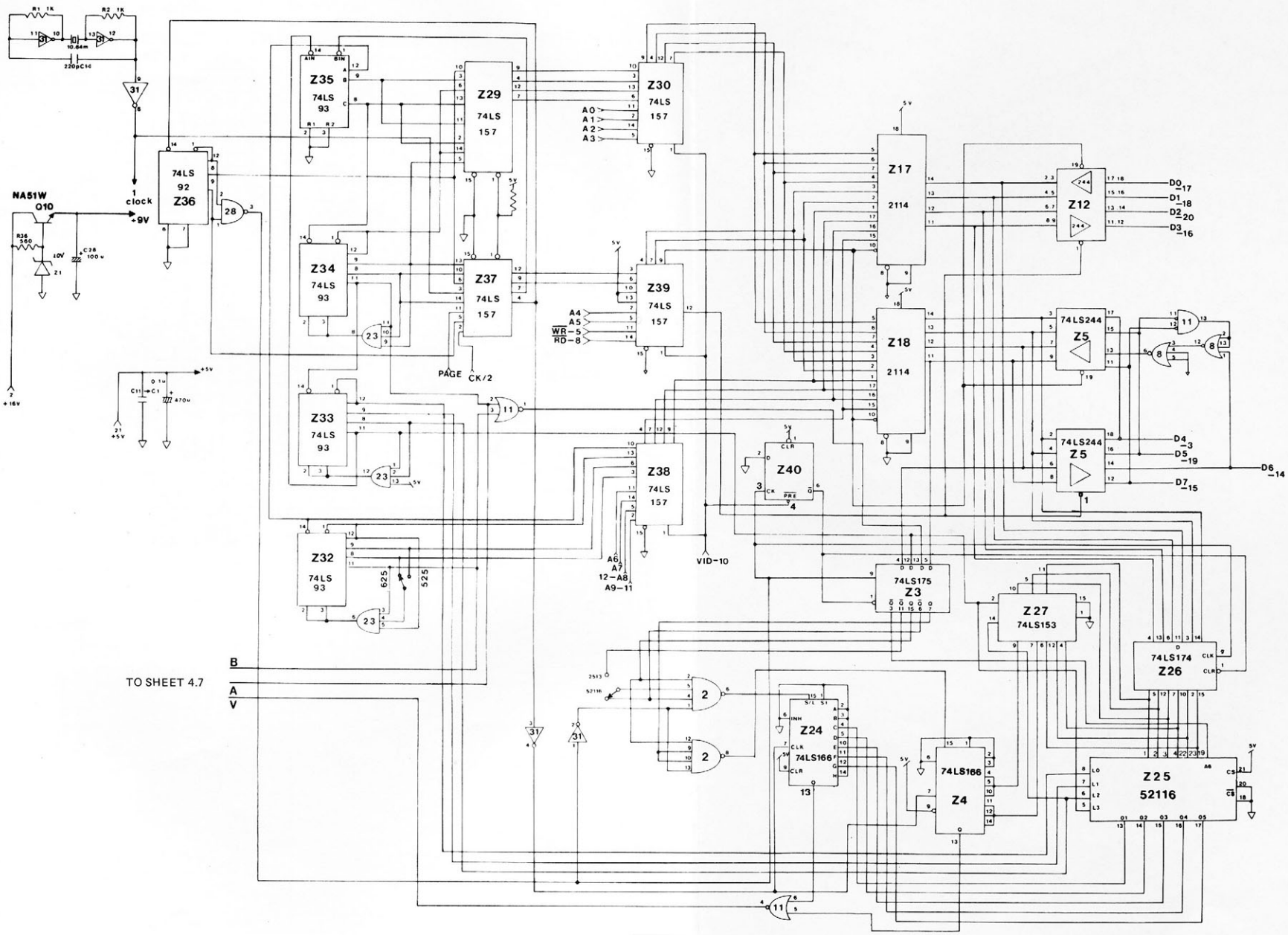


LATER Mk I

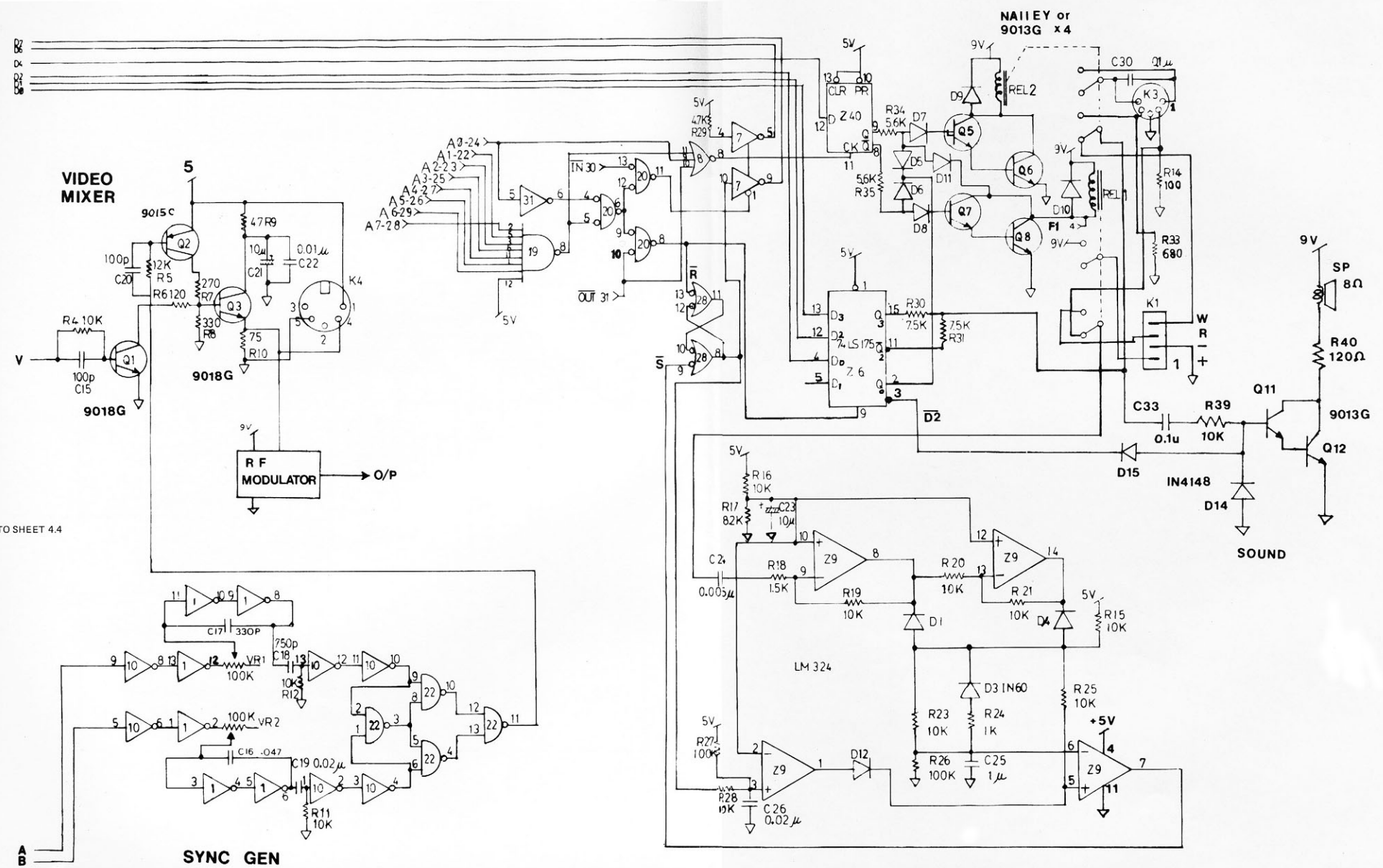


(Mk II Blue Label)

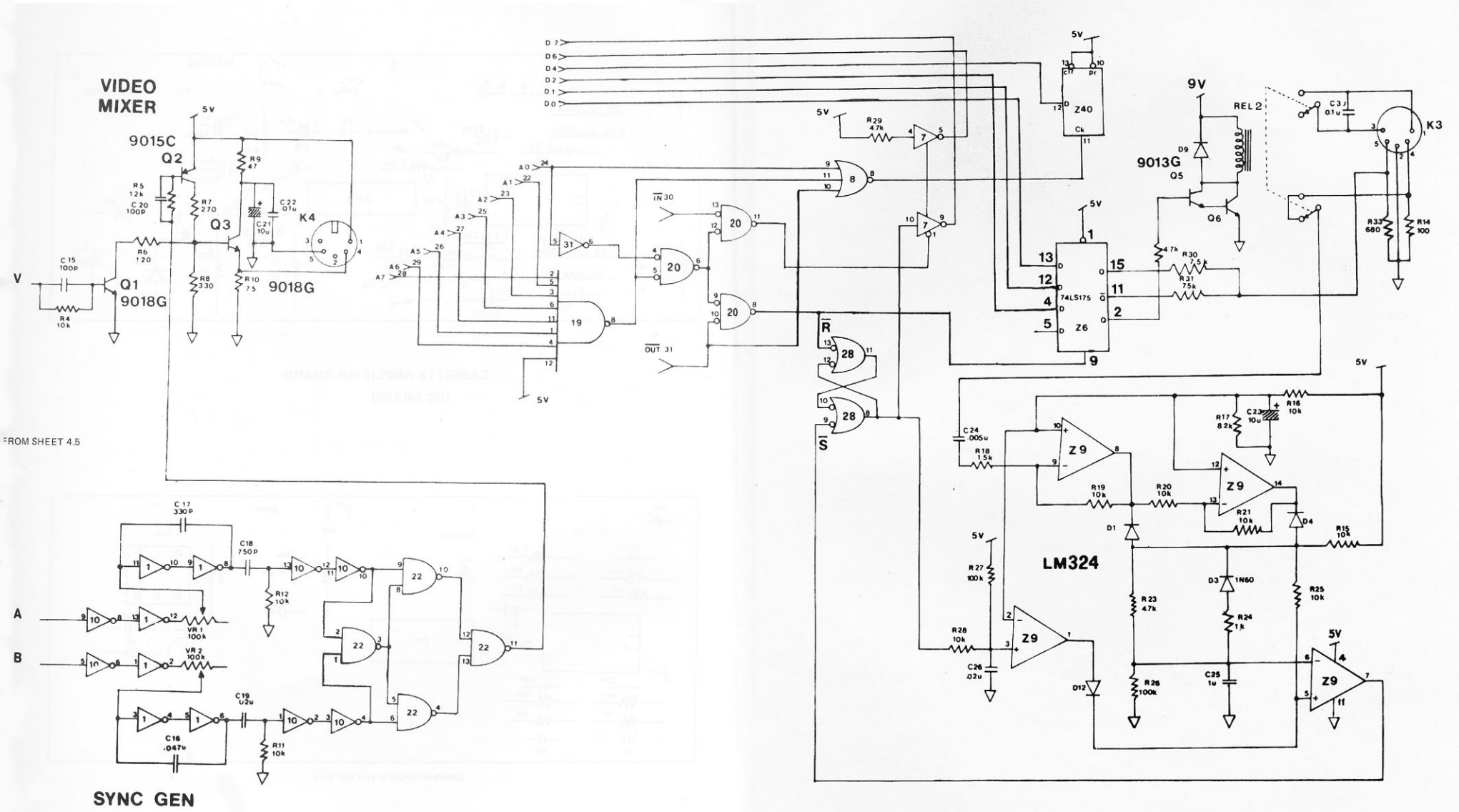
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.5	VIDEO INTERFACE CARD (Blue Label Series)



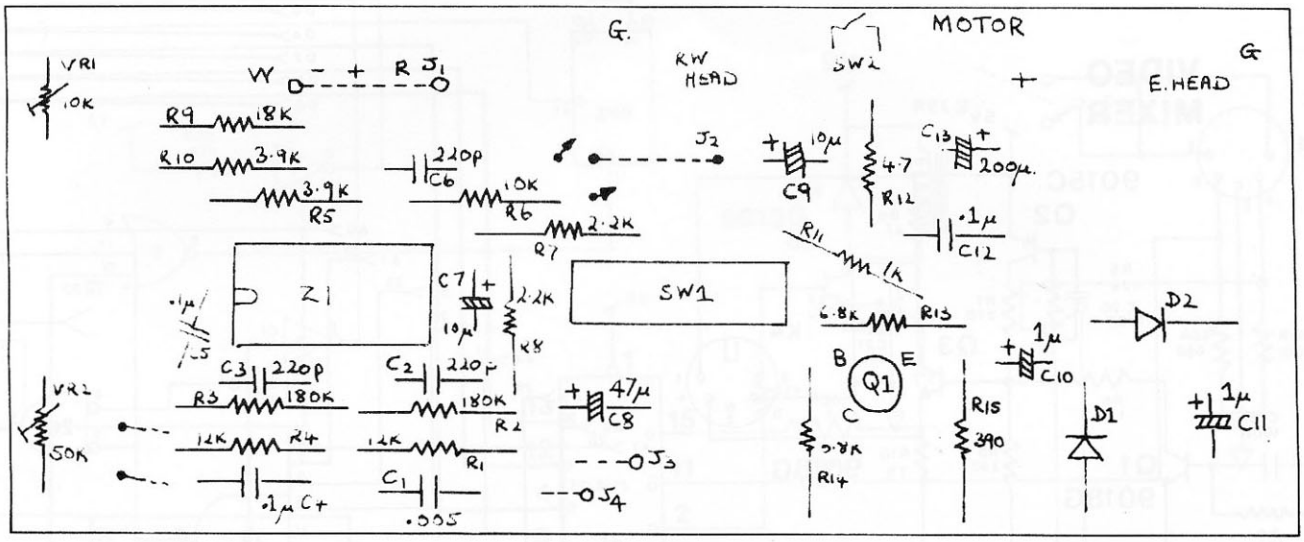
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.6	**CASSETTE INTERFACE** (Mk I) Note early models are not fitted with speaker and associated components



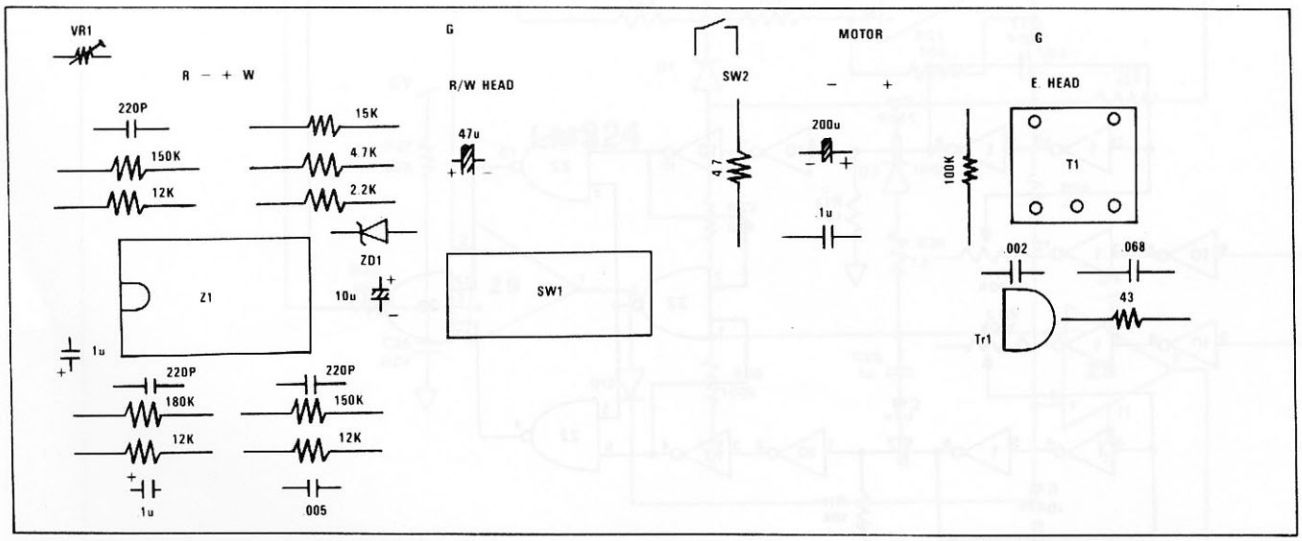
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.7	**CASSETTE INTERFACE** (Mk II) Note Blue Label models are fitted with speaker and associated components shown on preceding drawing (4.6)



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.8	CASSETTE RECORDER



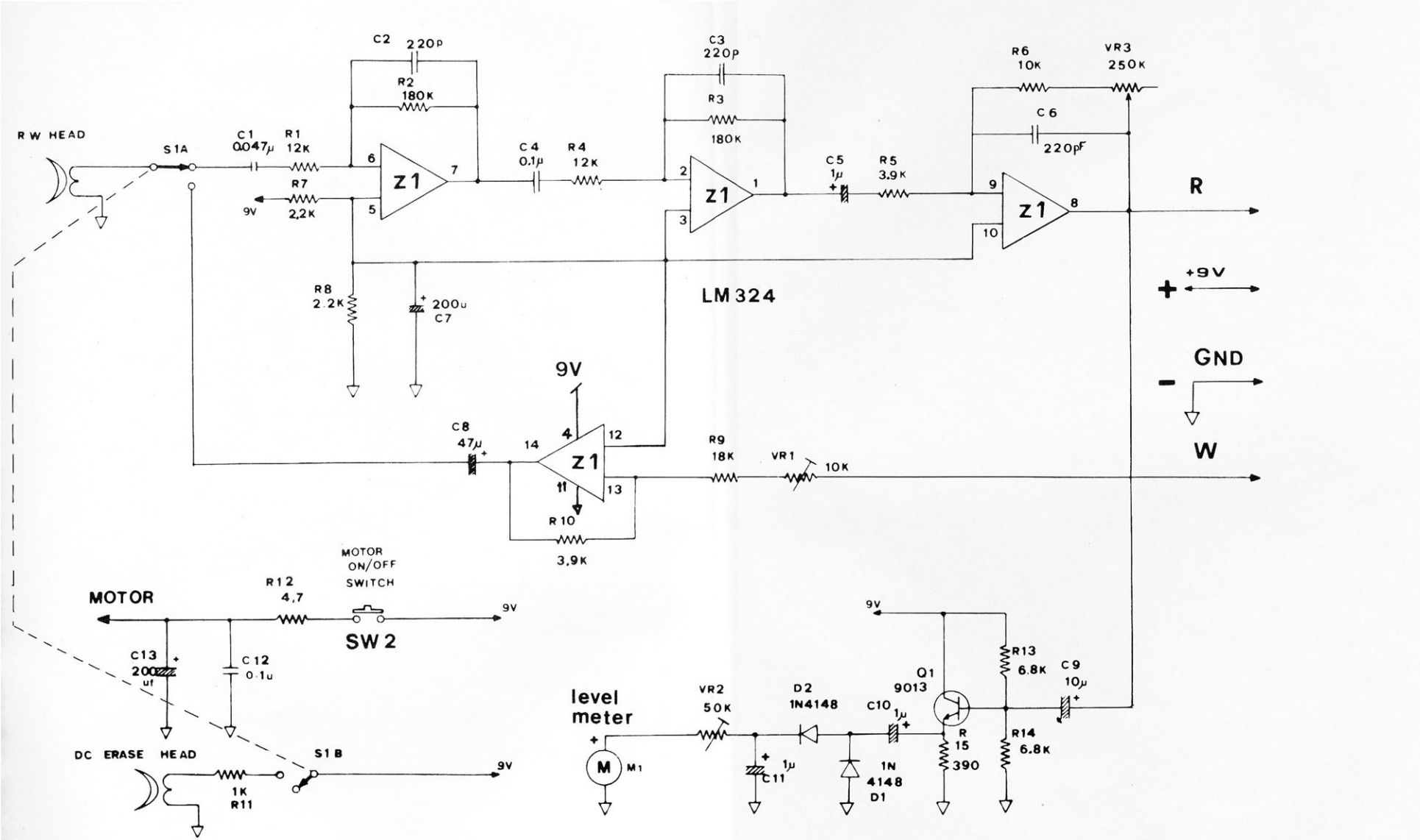
CASSETTE AMPLIFIER BOARD
(DC ERASE)



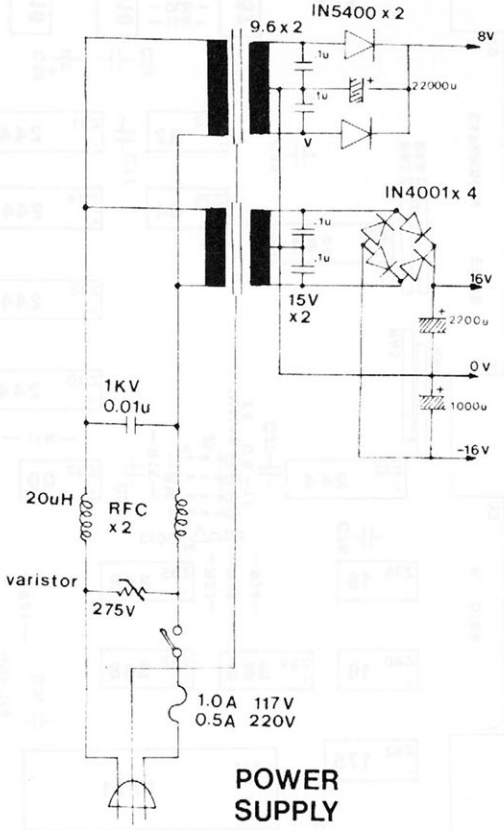
COMPONENT LAYOUT OF EACA P102 REV B

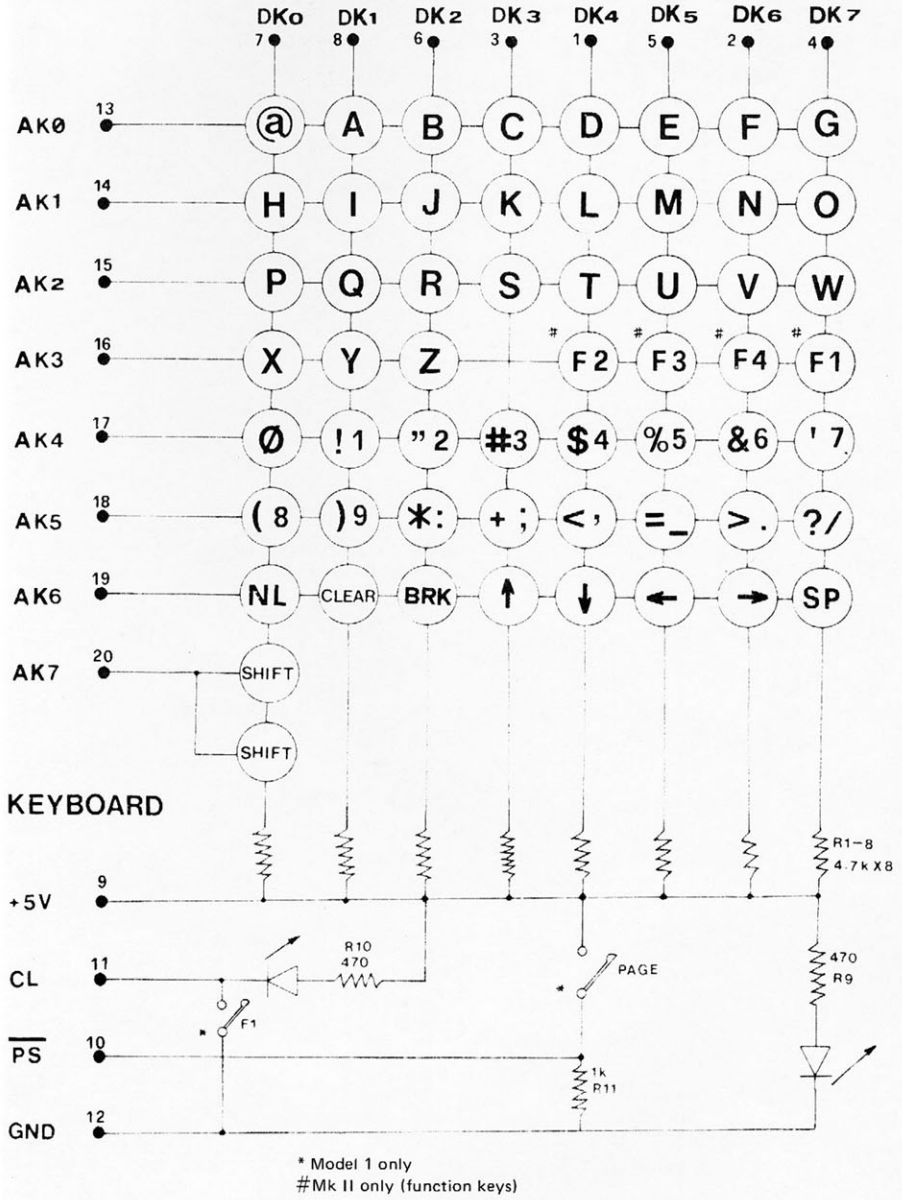
CASSETTE AMPLIFIER BOARD
(AC ERASE)

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.8	CASSETTE RECORDER



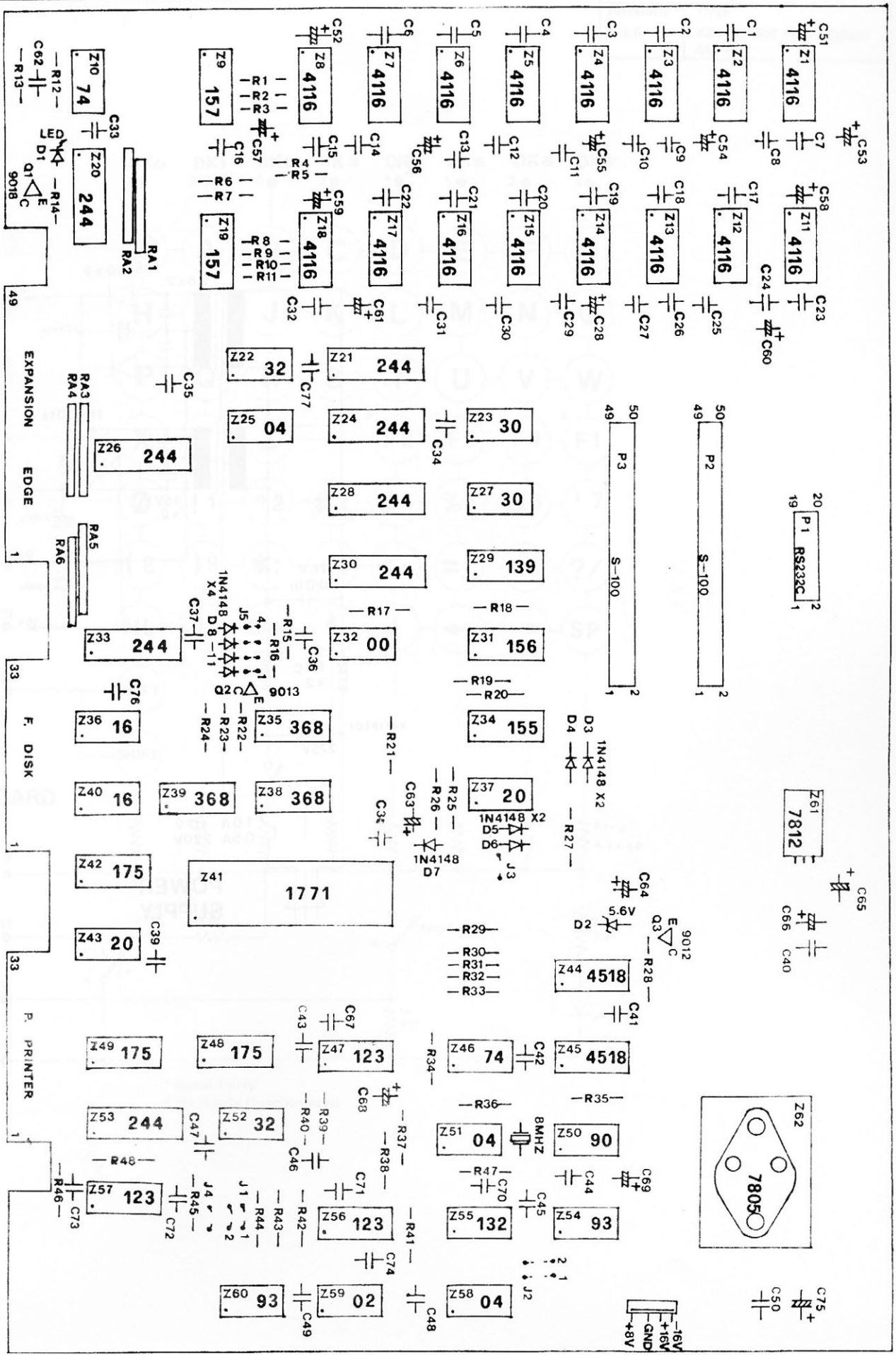
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.9	KEYBOARD AND POWER SUPPLY



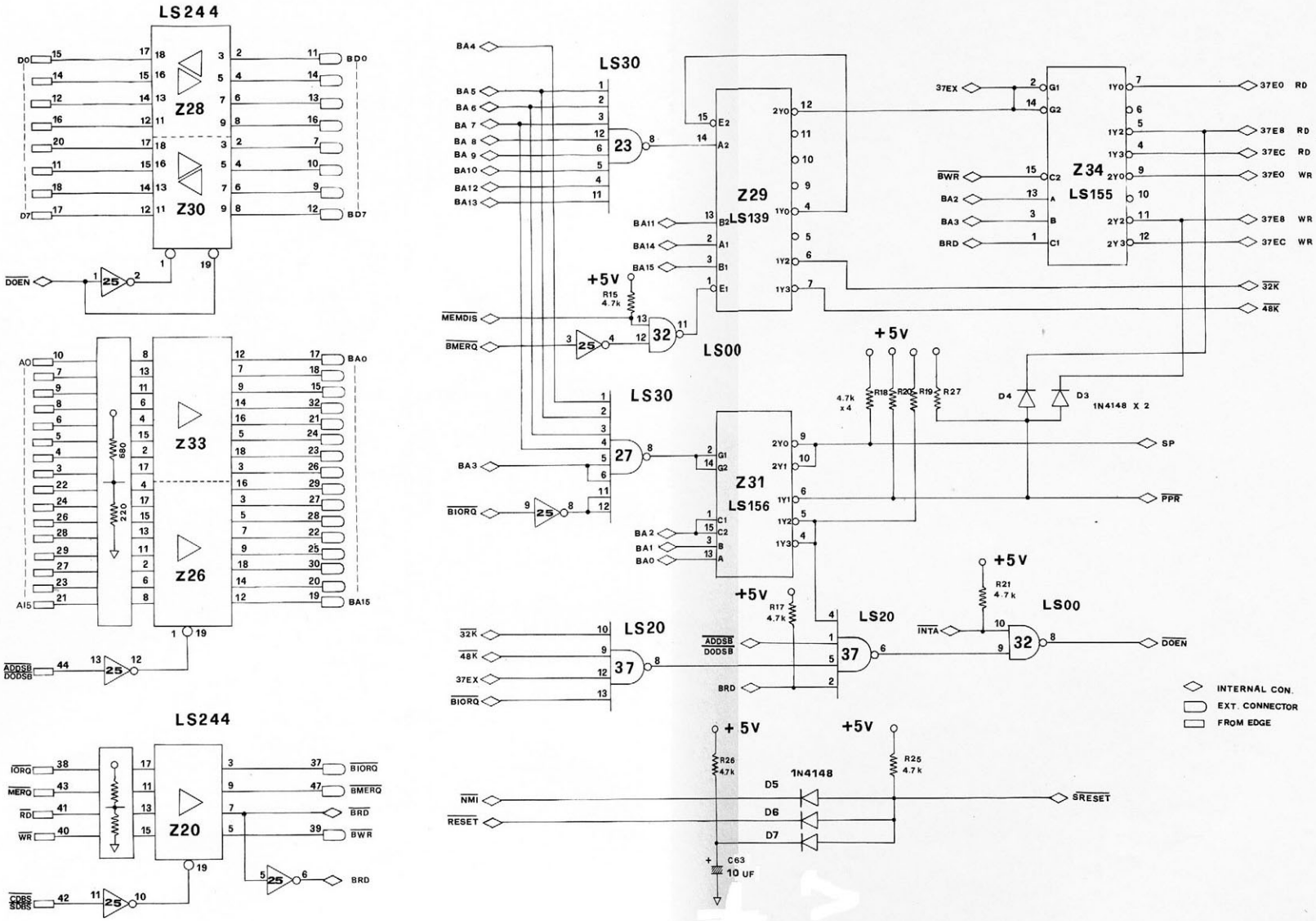


* Model 1 only
#Mk II only (function keys)

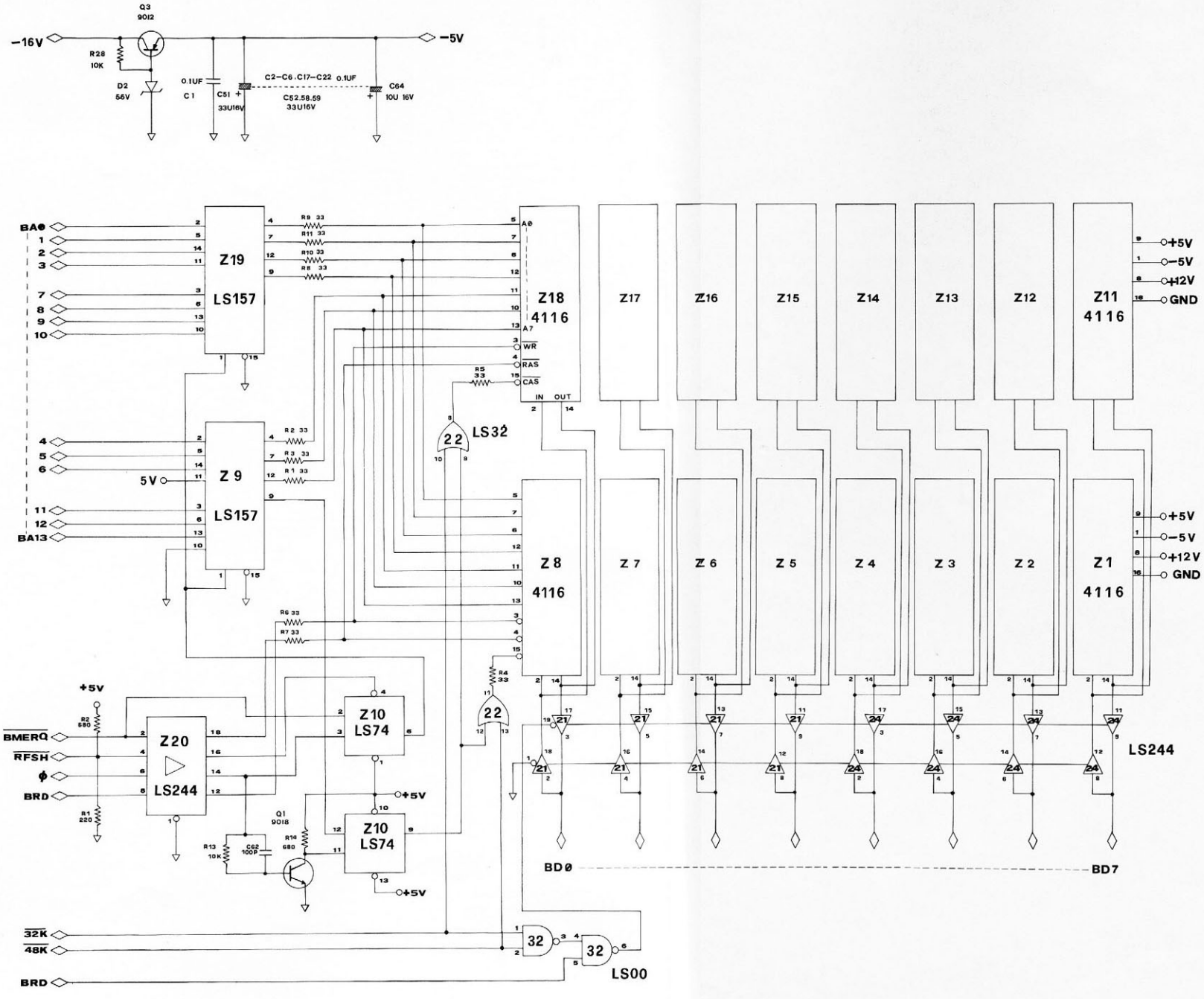
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.10	X-4020 EXPANDER



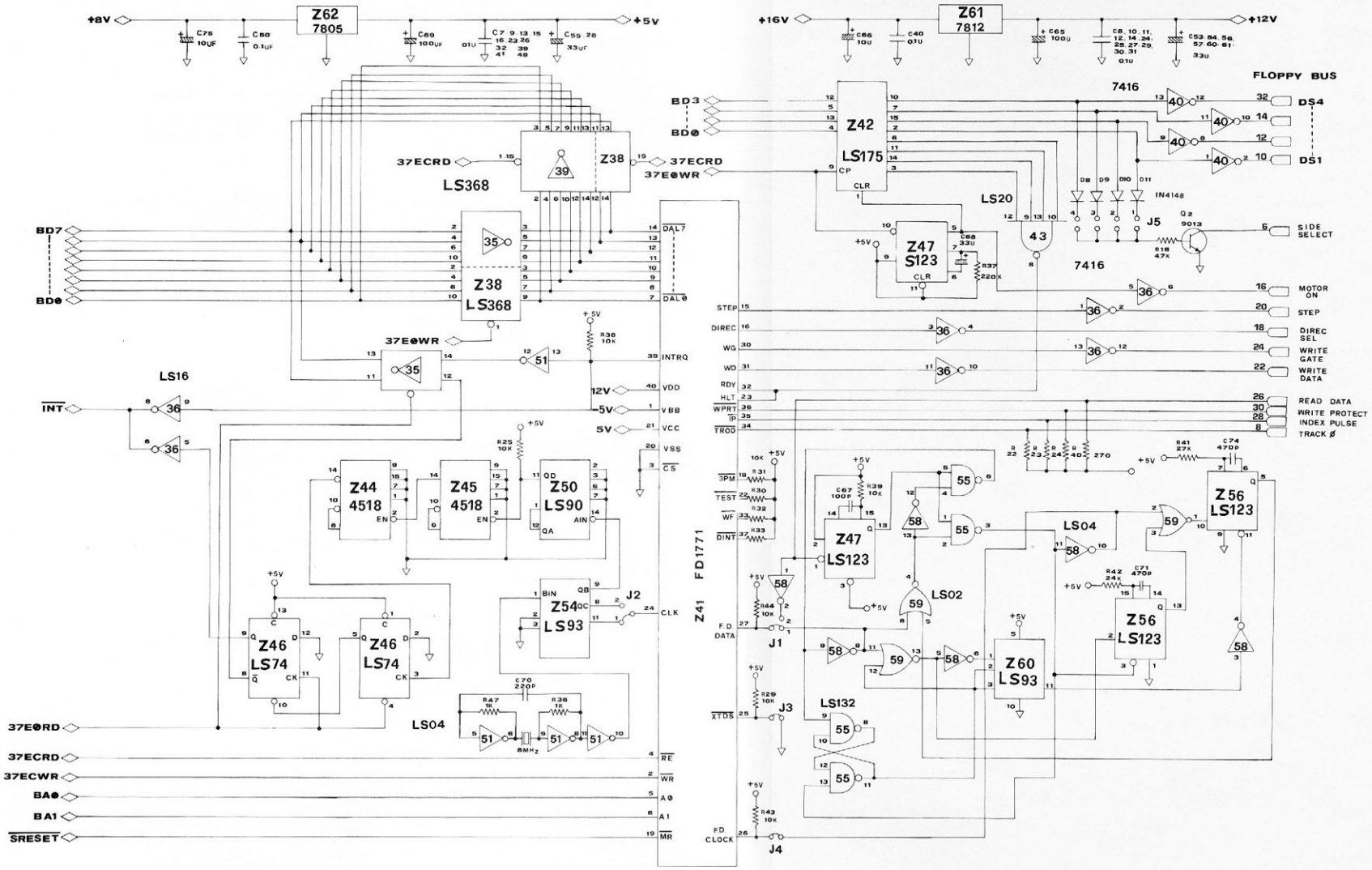
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.10	X-4020 EXPANDER Sheet 1



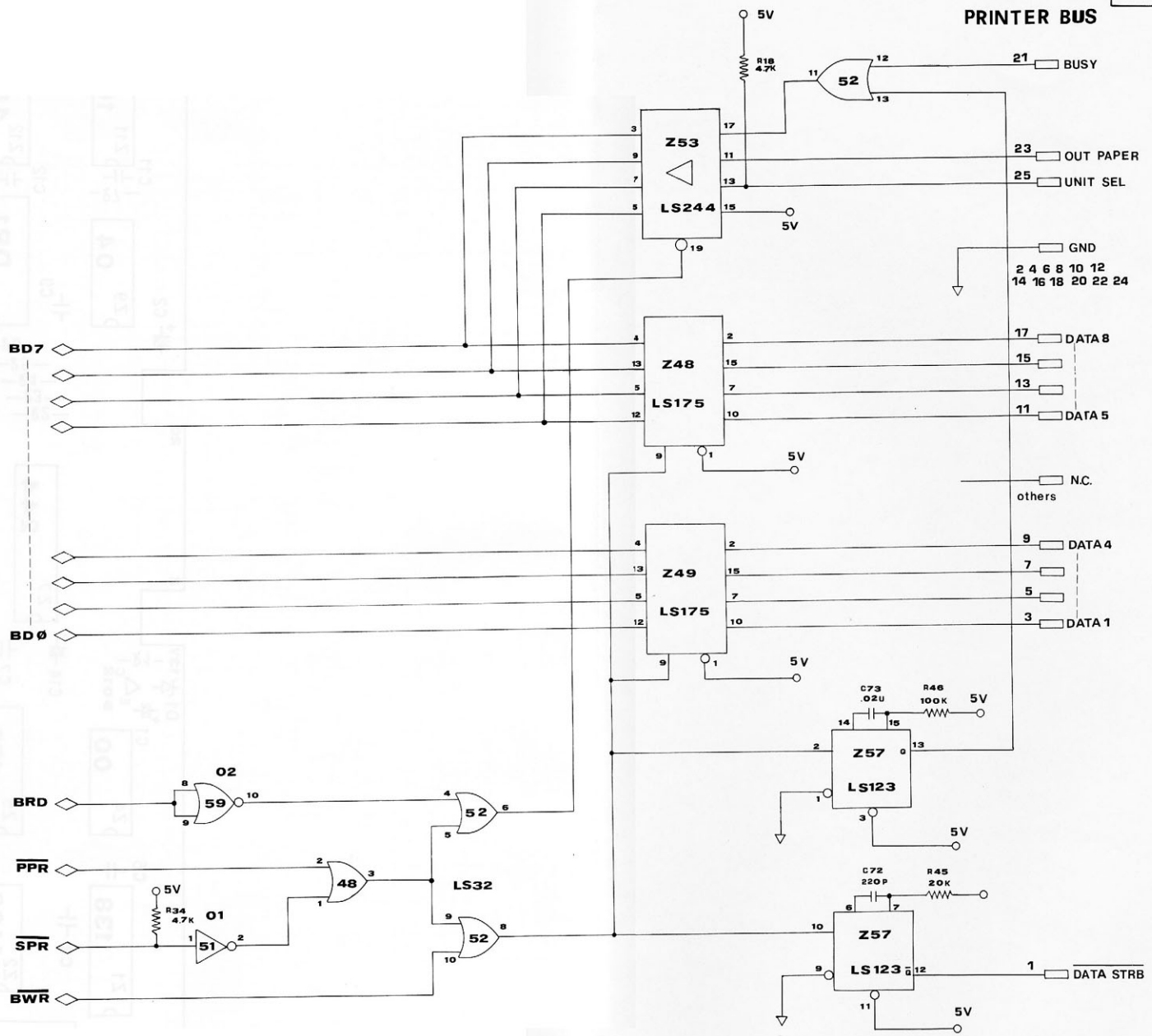
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.11	X-4020 EXPANDER Sheet 2



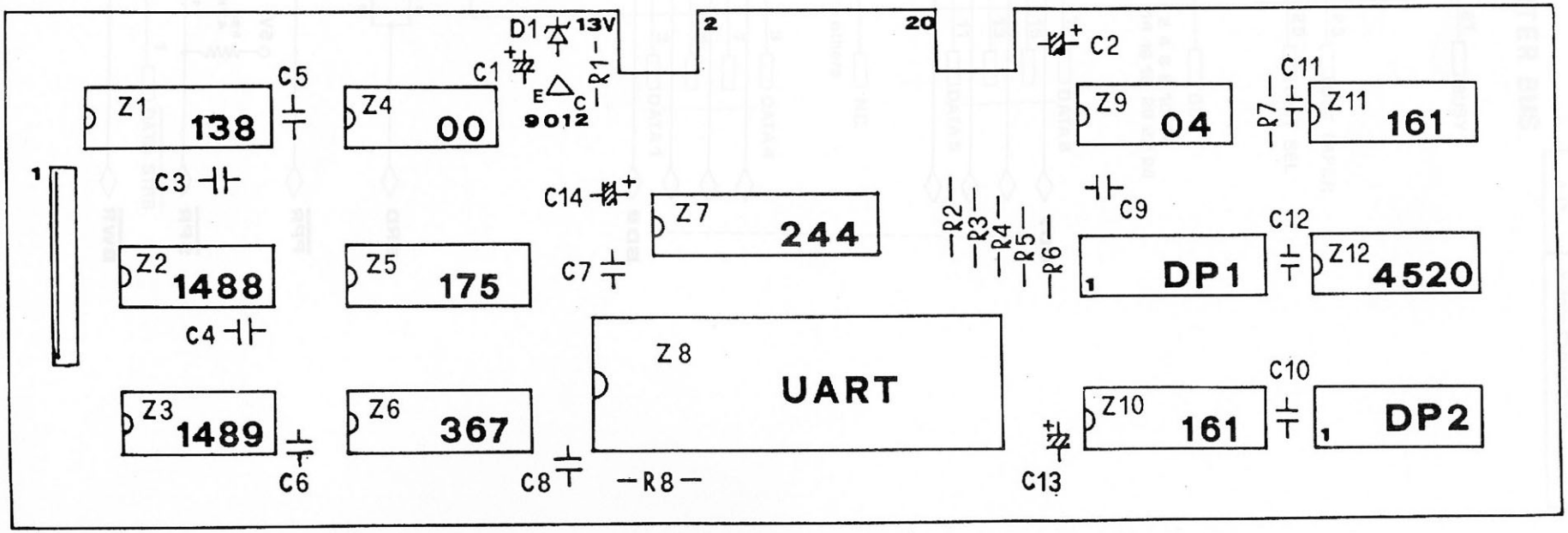
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.12	X-4020 EXPANDER Sheet 3



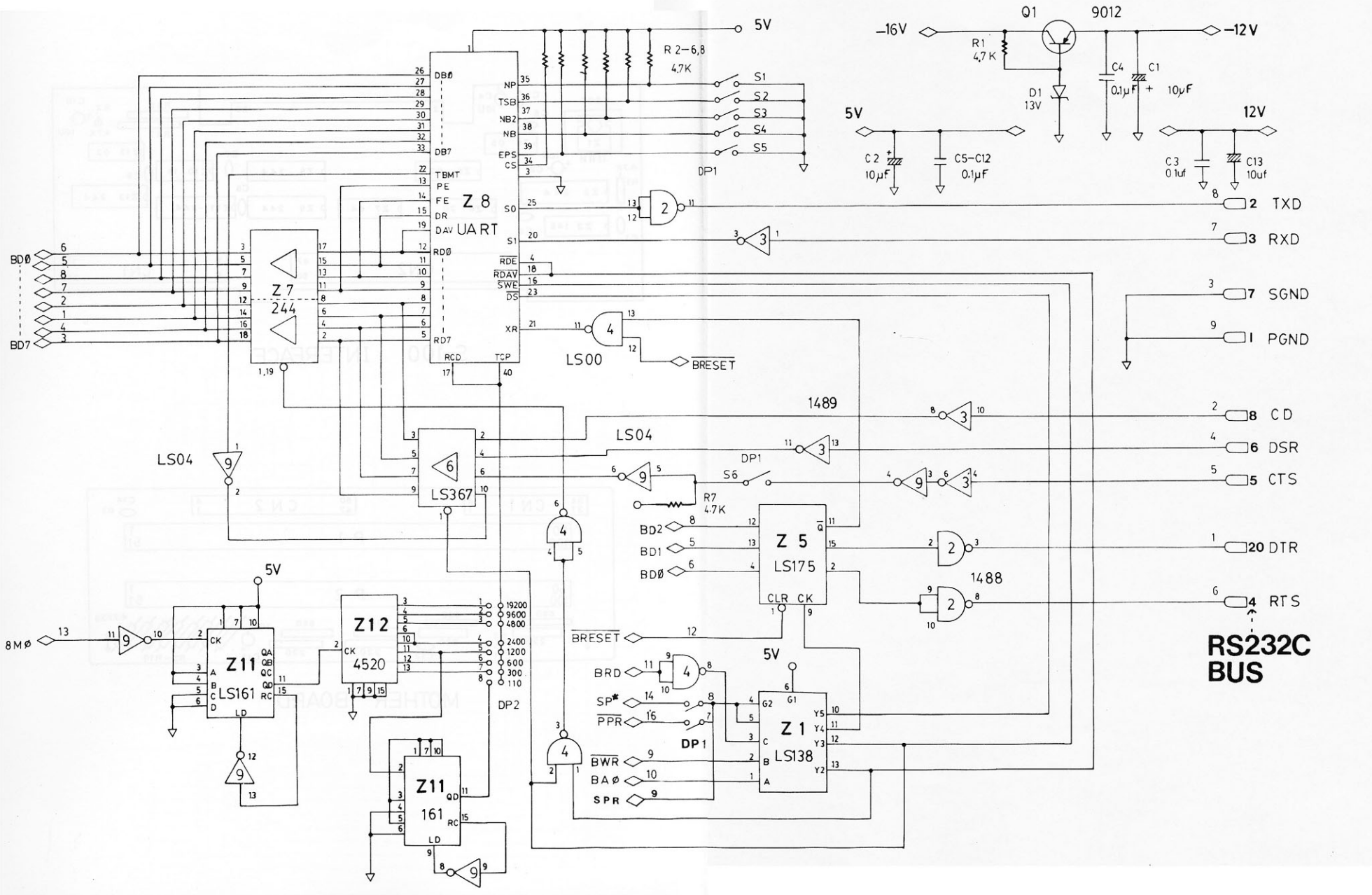
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.13	X-4020 EXPANDER Sheet 4



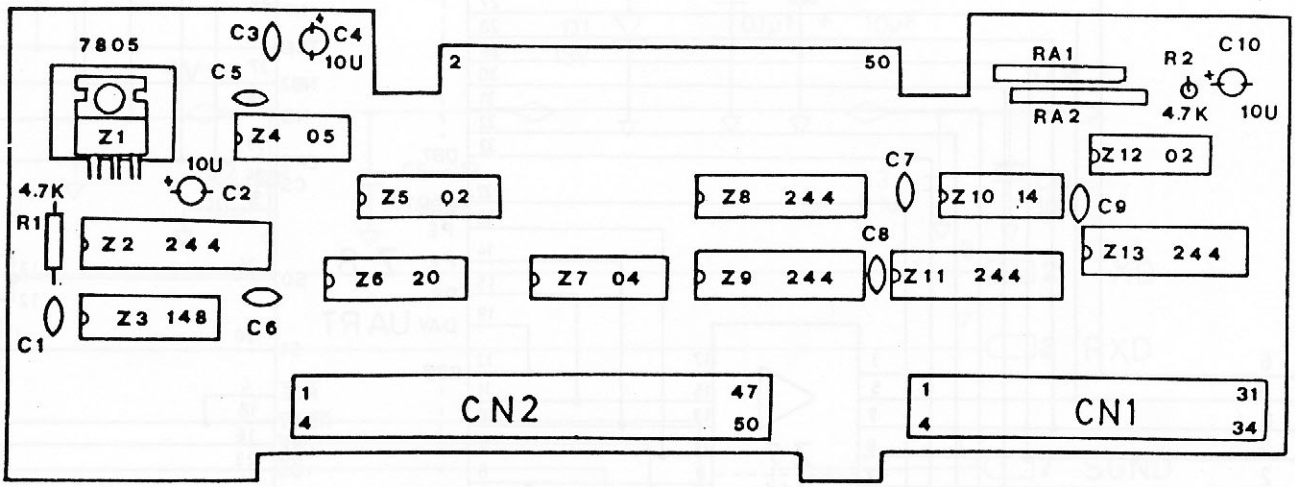
DICK SMITH SYSTEM 80	
DRAWING 4.14	TITLE X-4022 RS-232C COMMUNICATIONS PORT



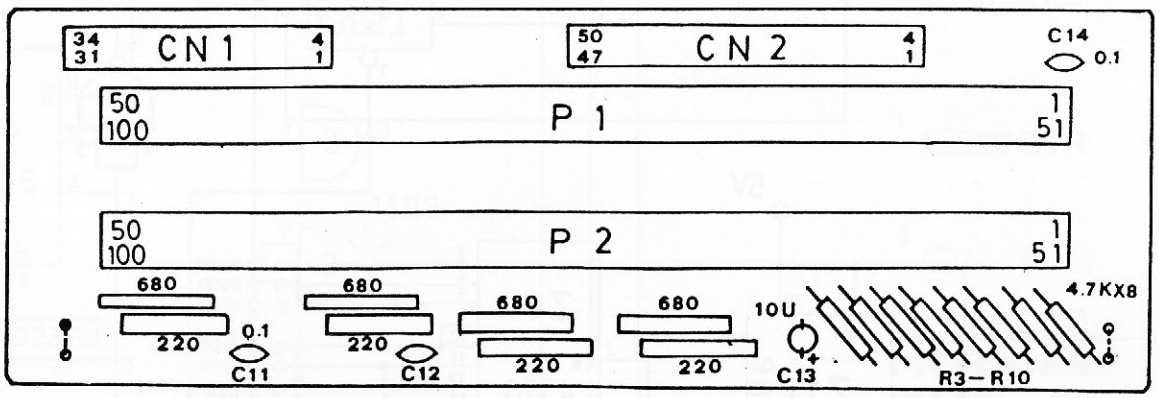
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.14	X-4022 RS-232C COMMUNICATIONS PORT



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.15	X-4024 S-100 INTERFACE

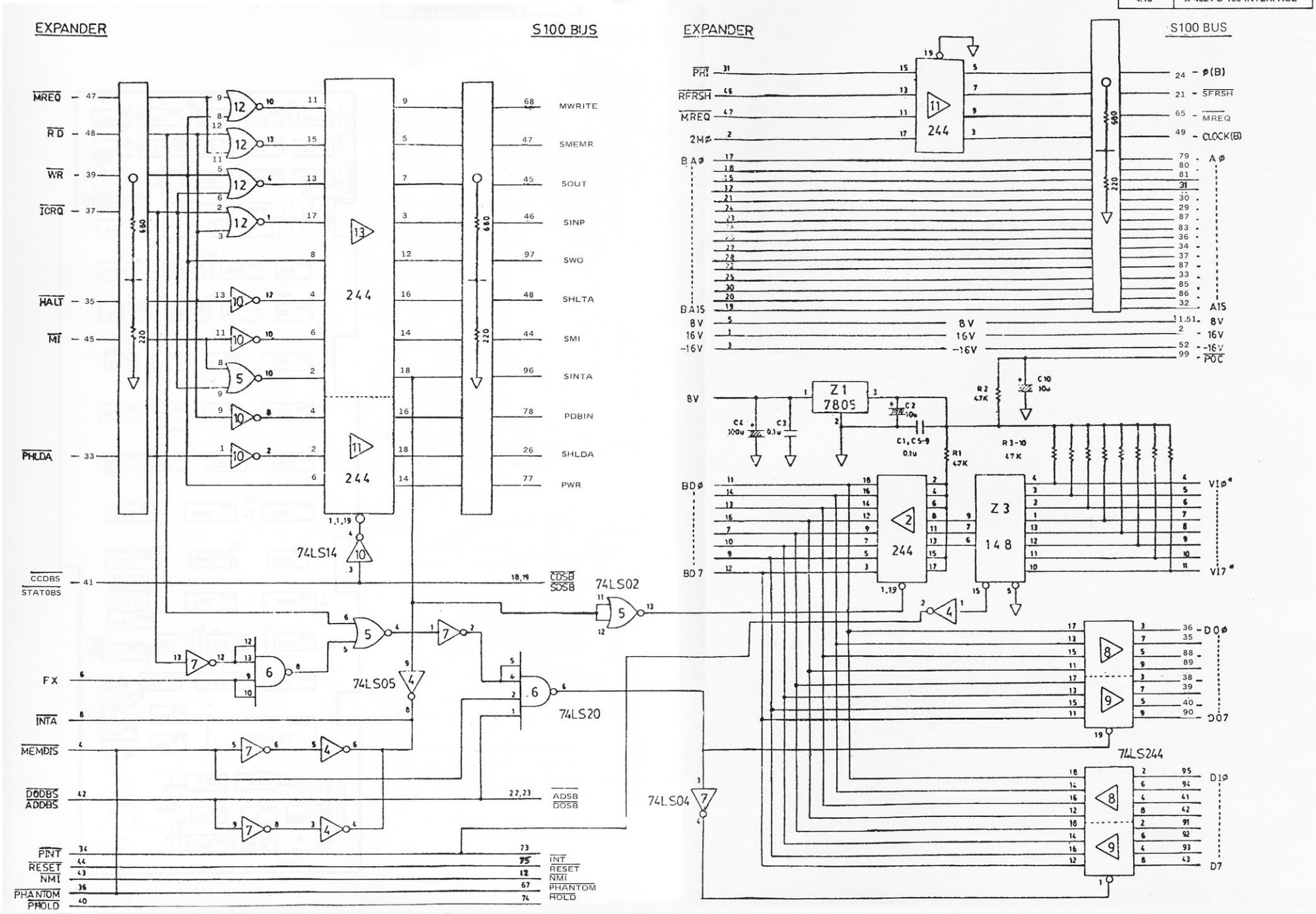


S-100 INTERFACE

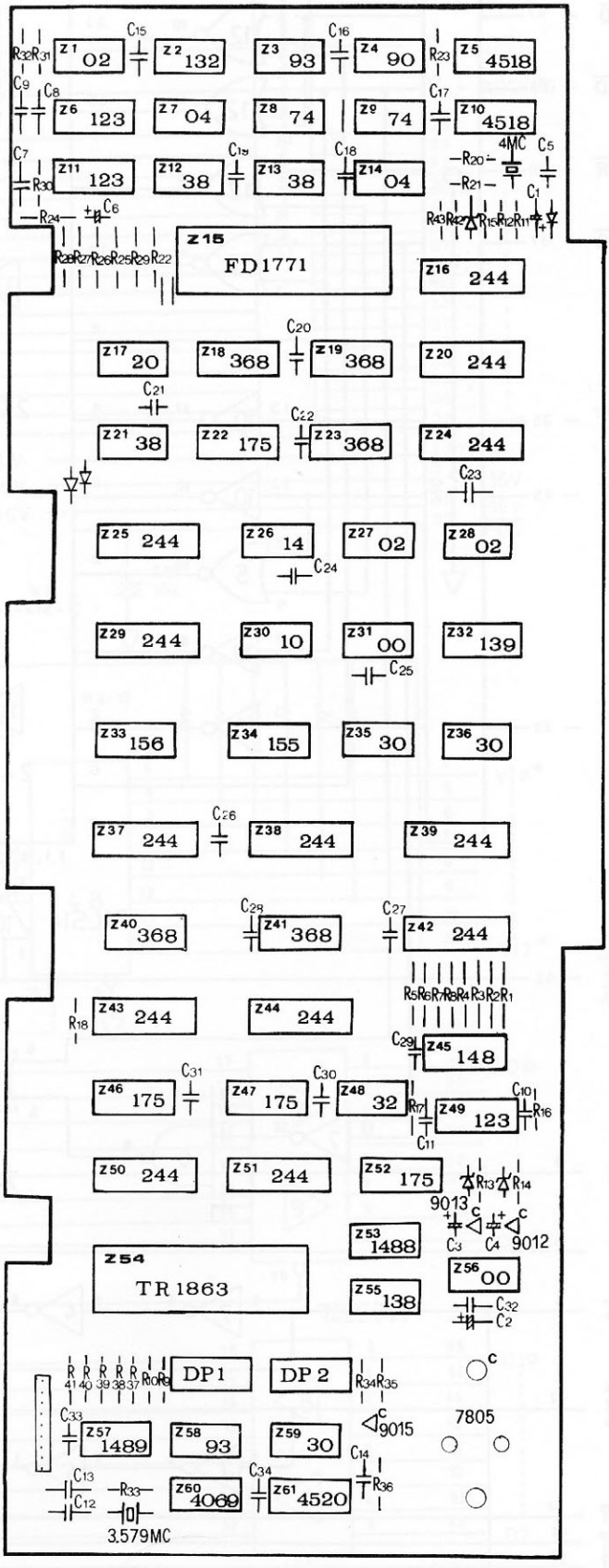


MOTHER BOARD

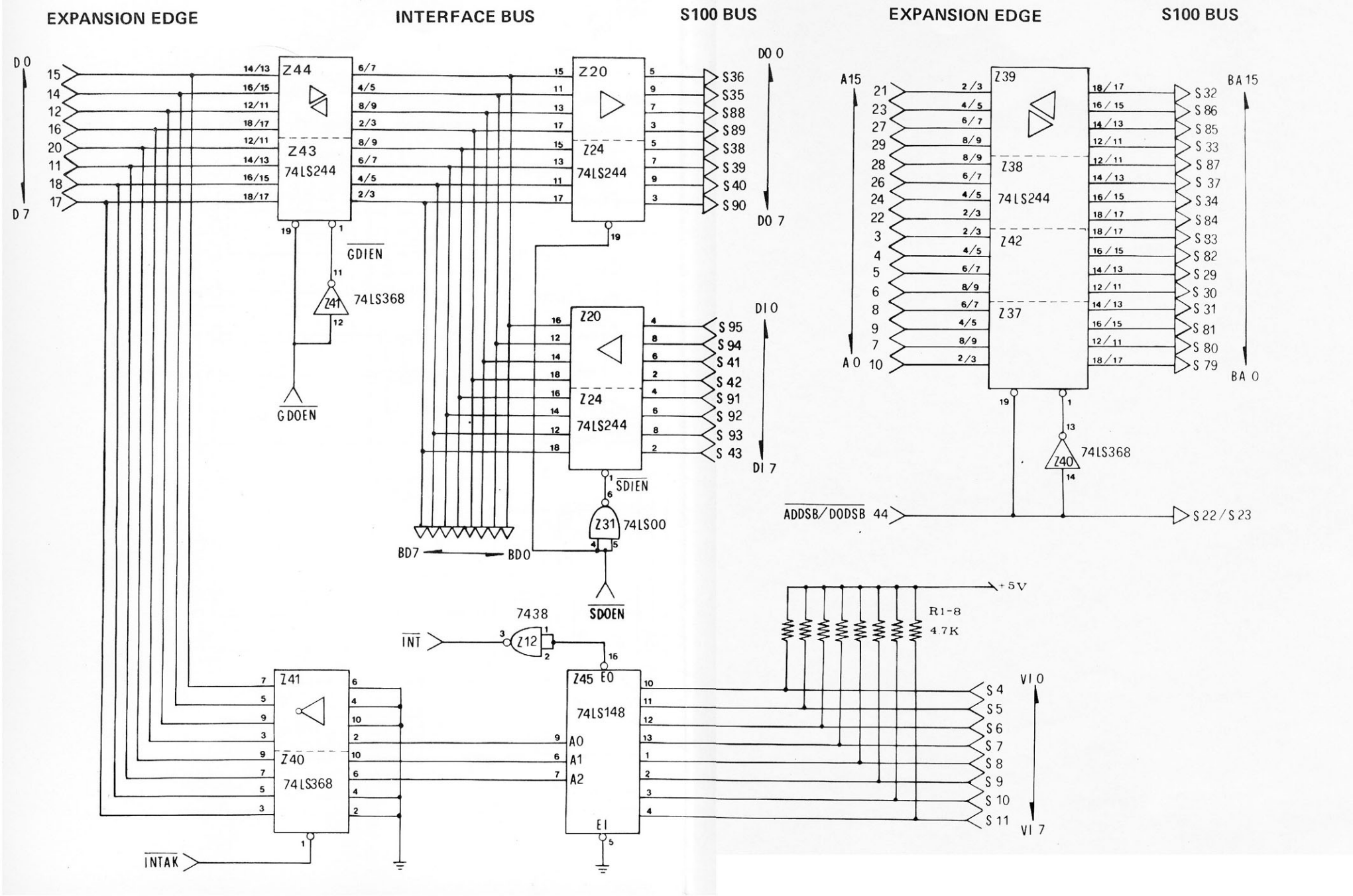
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.15	X-4024 S-100 INTERFACE



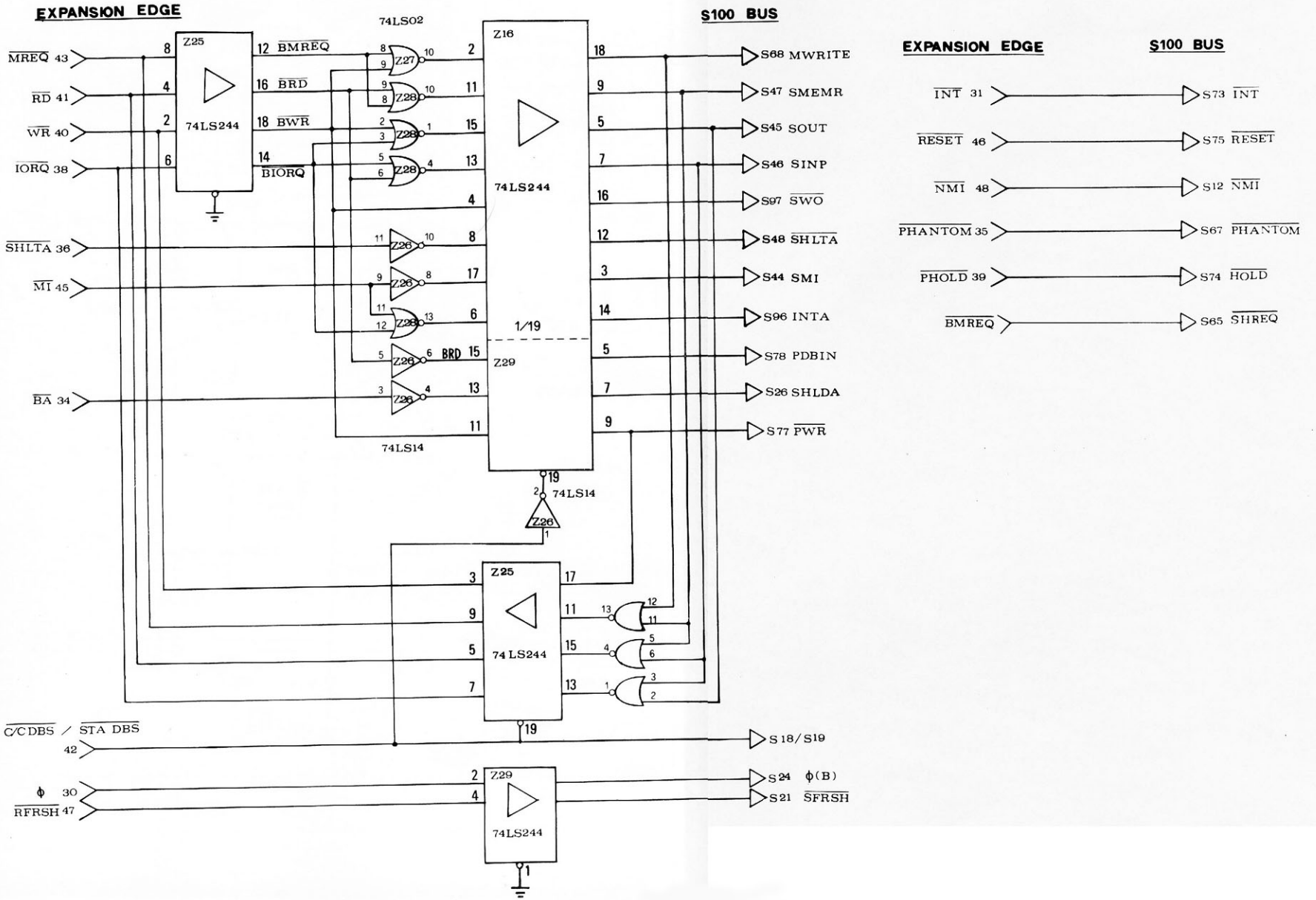
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.16	X-4010 EXPANSION UNIT INTERFACE BUFFERS



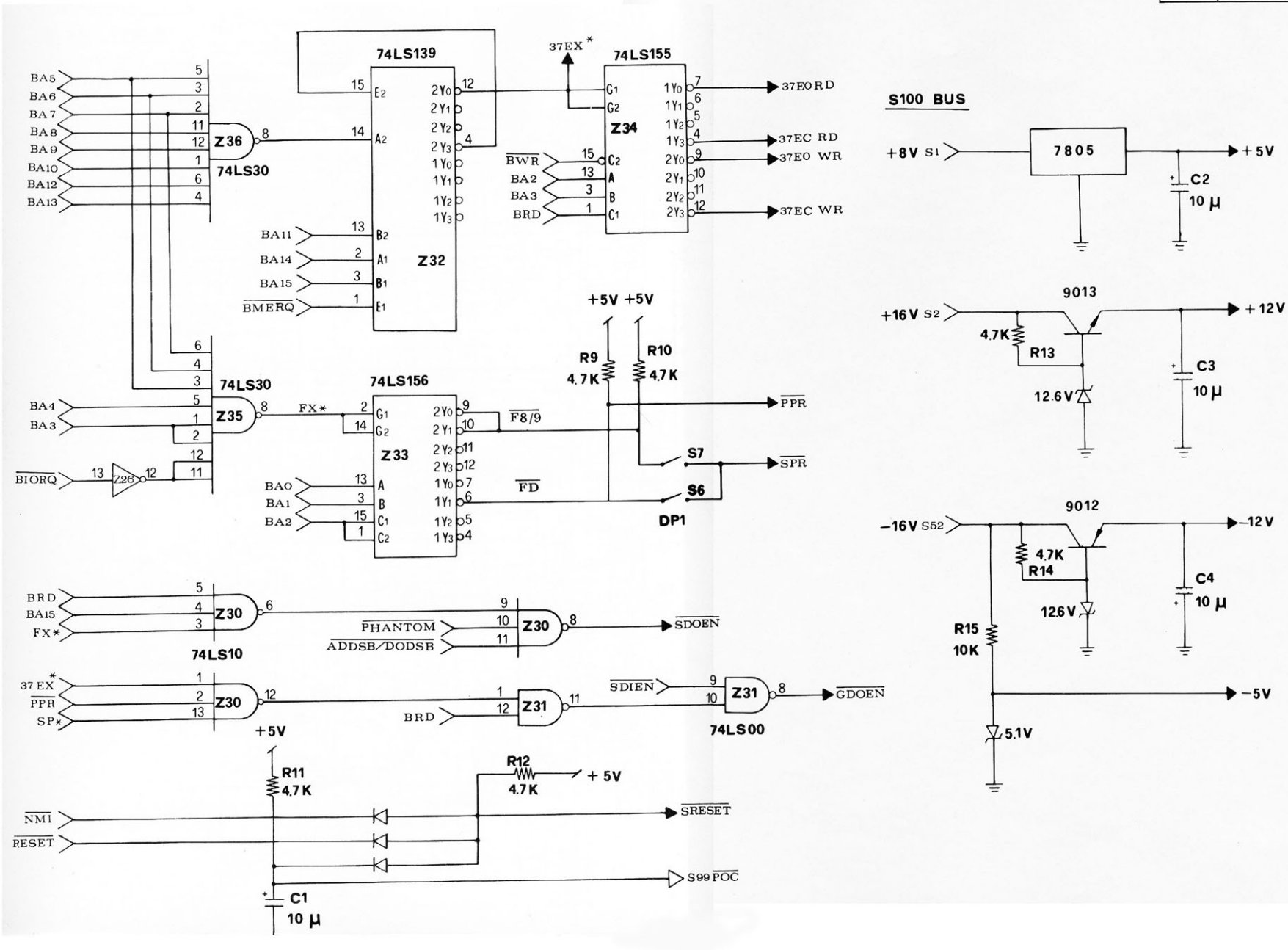
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.16	X-4010 EXPANSION UNIT INTERFACE BUFFERS



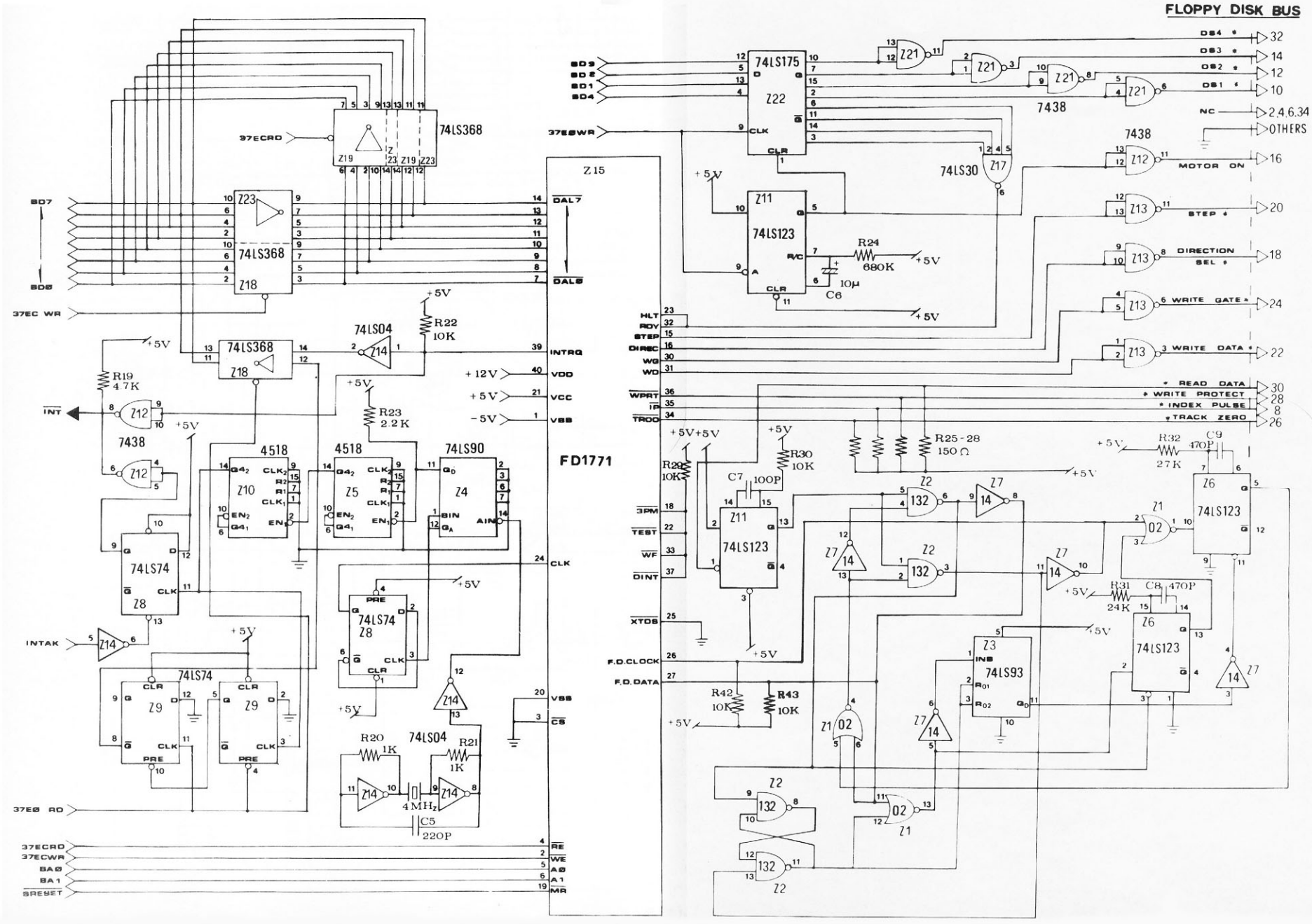
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.17	X-4010 EXPANSION UNIT S100 INTERFACE



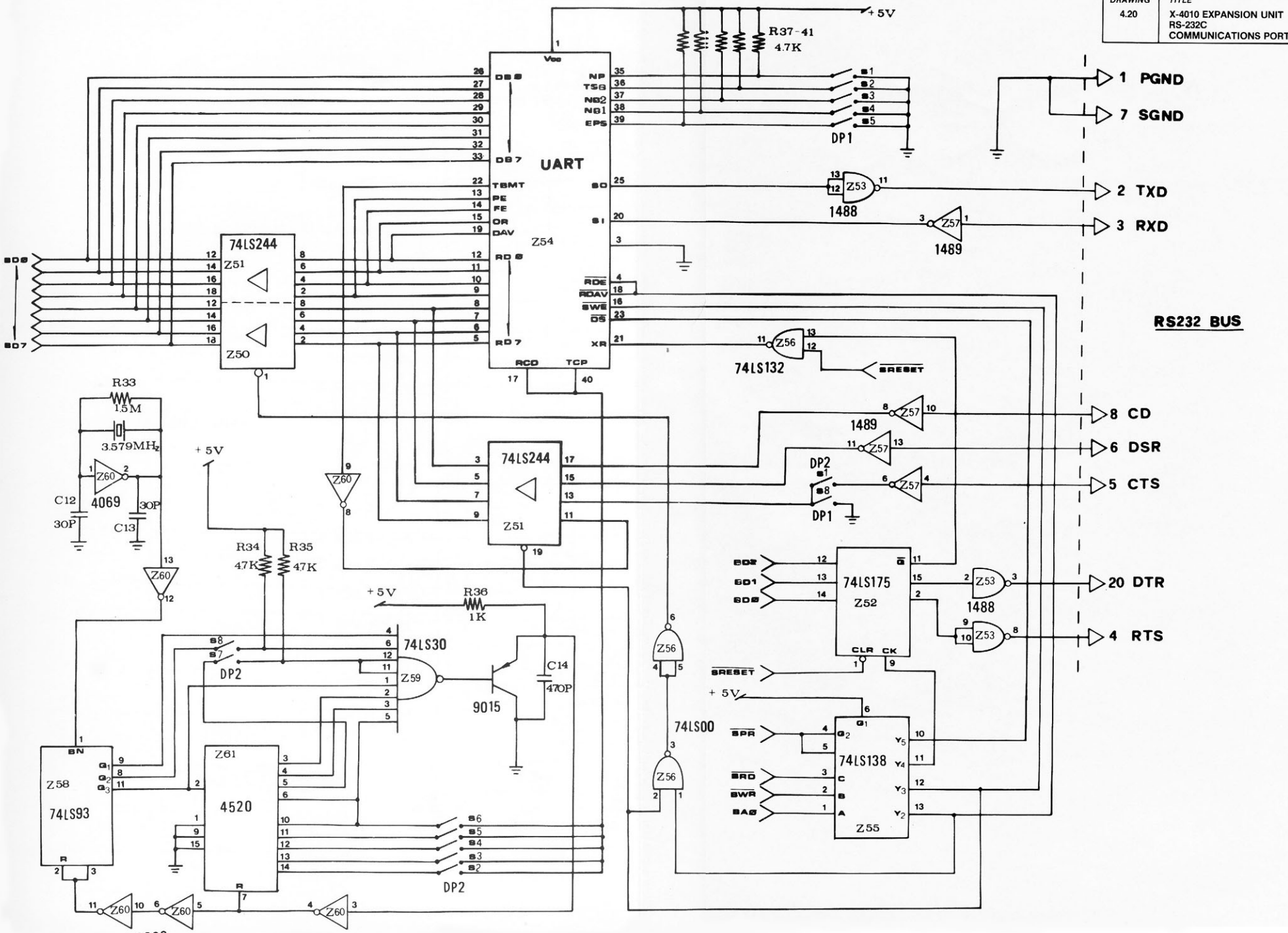
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.18	X-4010 EXPANSION UNIT ADDRESS DECODING



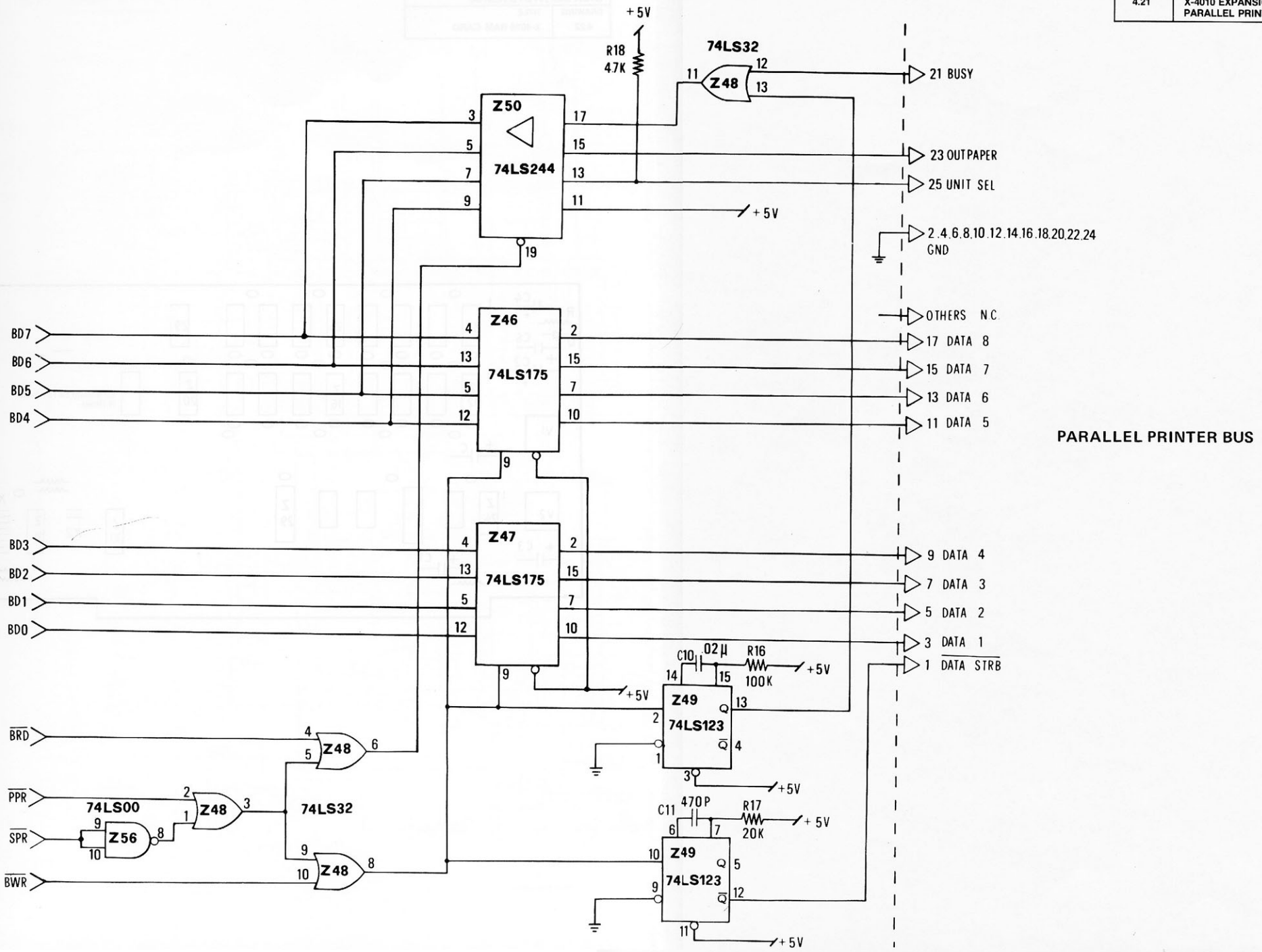
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.19	X-4010 EXPANSION UNIT FLOPPY DISK CONTROLLER



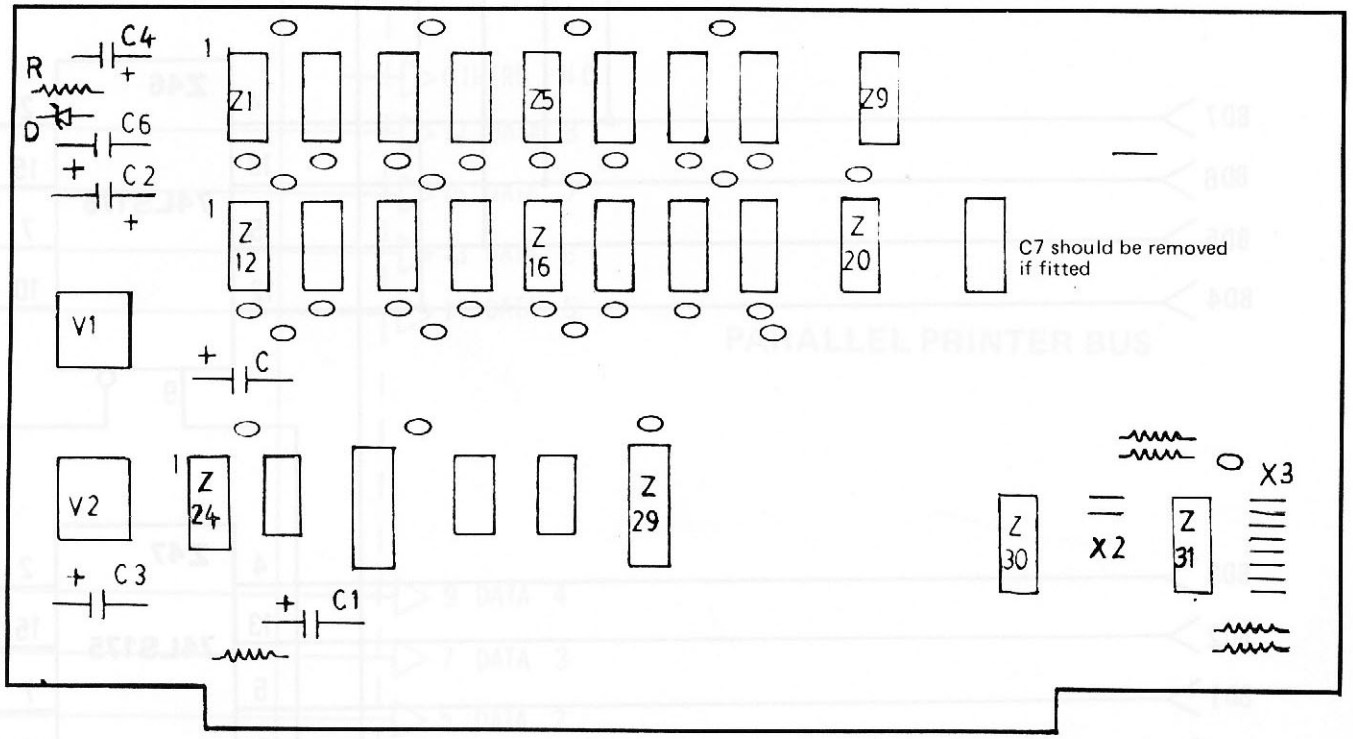
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.20	X-4010 EXPANSION UNIT RS-232C COMMUNICATIONS PORT



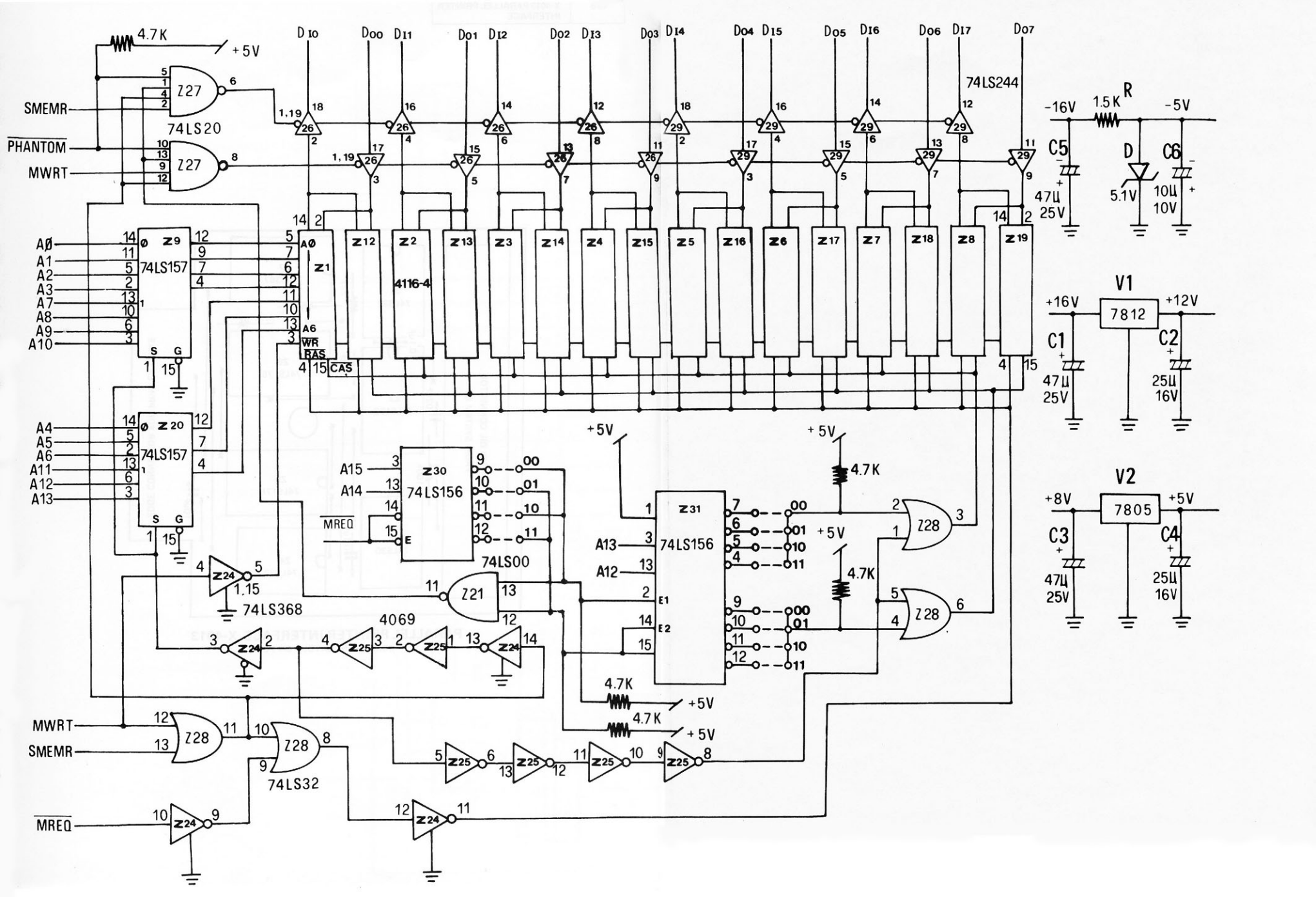
DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.21	X-4010 EXPANSION UNIT PARALLEL PRINTER PORT



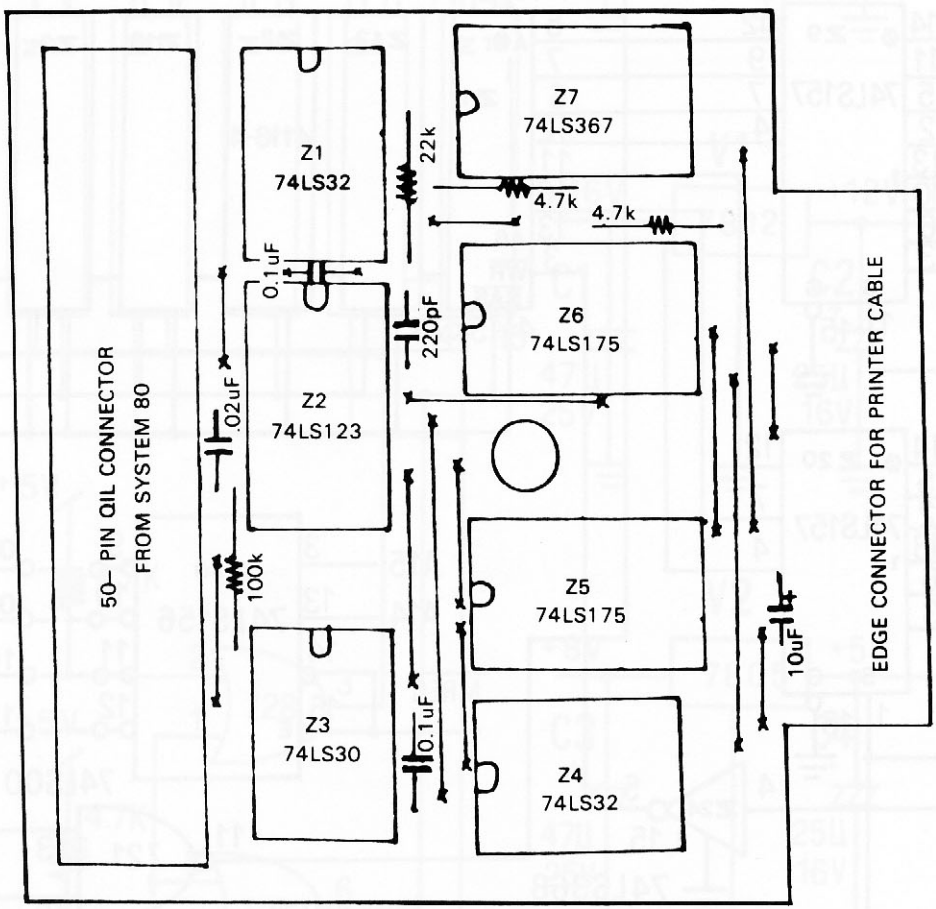
DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.22	X-4016 RAM CARD



DICK SMITH SYSTEM 80	
DRAWING	TITLE
4.22	X-4016 RAM CARD



DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.23	X-4013 PARALLEL PRINTER INTERFACE



PARALLEL PRINTER INTERFACE X-4013

COMPONENT LAYOUT ON PCB

DICK SMITH SYSTEM 80	
DRAWING	*TITLE*
4.23	X-4013 PARALLEL PRINTER INTERFACE