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RC702 Microcomputer
Technical Manual

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Abstract:

This manual contains a technical description of the RC702 Microcomputer.

(122 printed pages)

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1. DESCRIPTION

1.

The RC702 Microcomputer is a selfcontained computer system, which together with keyboard, videomonitor, and zero, one, or two flexible disc drives make a complete computer system.

The keyboard used may be an RC721 or an RC722. The video monitor used may be an RC752. The flexible disc drive may be an RC761 or an RC762. All these units are described in their own manuals. Fig. 1.1 shows an example of how to connect these units.

The RC702 itself is built up by the following parts:

1. MIC702 Microcomputer board
2. ROAxxx Character generator
3. KBN702 Cabinet with cables, transformer, and rectifier unit
4. CBL921 Internal video cable
5. CBL903 Internal power cable
6. CBL928 Internal sync. cable
7. CBL440 External power cable
8. POW739 Power supply

Part 1 and 2 are described in chapter 2 of this manual. Part 3 to 7 are described in chapter 3 of this manual, and part 8 is described in chapter 4 of this manual.

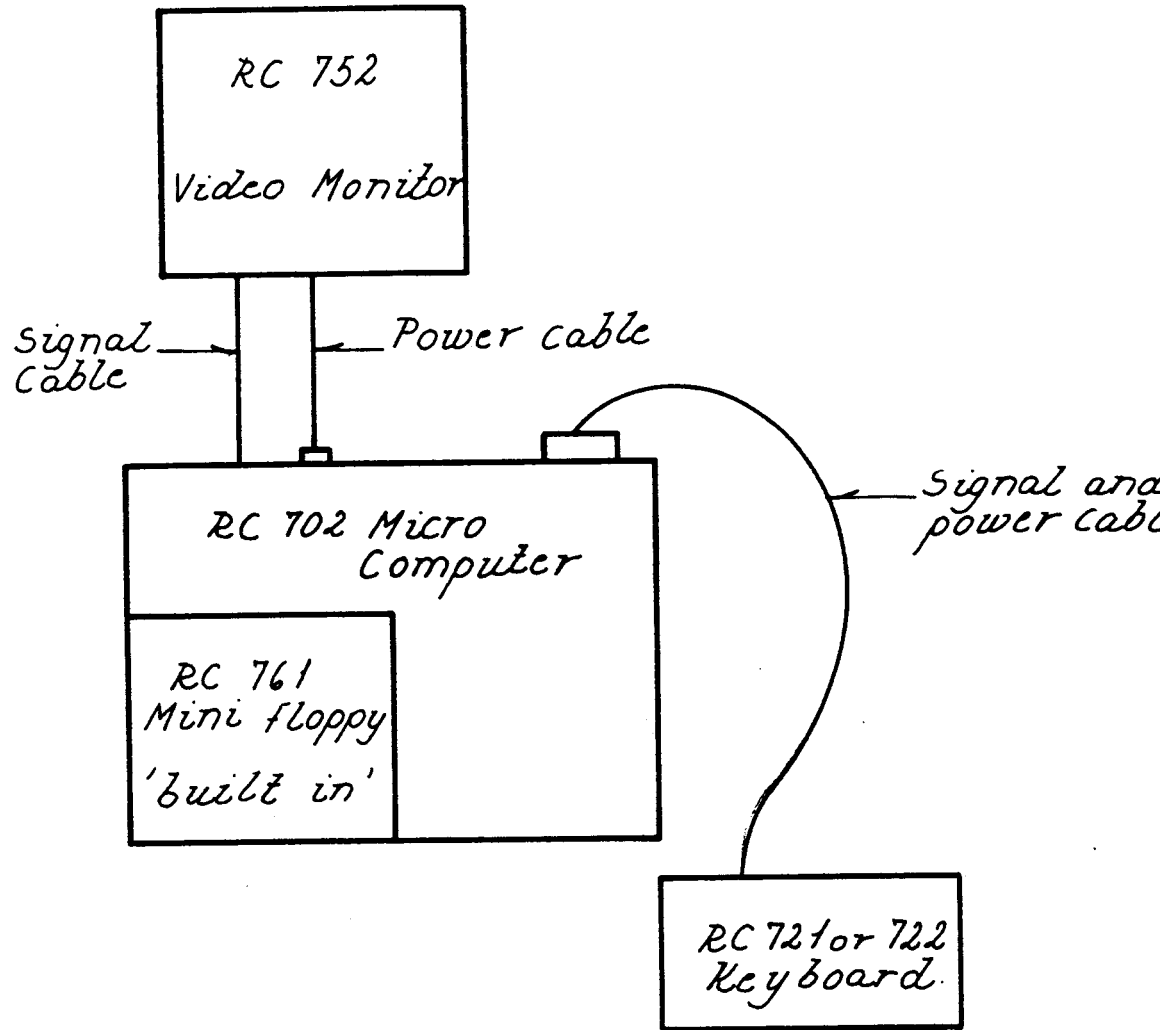


Fig. 1.1. Example of an RC 700 System made of an RC 702 Microcomputer, Video Monitor, Keyboard, and Mini floppy disk drive.

2. MIC702 MICROCOMPUTER AND CHARACTER GENERATOR 2.

2.1 General Description 2.1

The MIC 702 is built on a single circuit board. Power is supplied via a 4 pin connector, and MIC702 needs the following supply:

+5 V typical 2.5 Amp.

+12 V typical 0.1 Amp.

-12 V typical 0.1 Amp.

The board layout is shown in fig. 2.1 which also shows the input/output connections.

2.2 Block Diagram 2.2

Fig. 2.2 shows a block diagram of MIC702. In the diagram is shown where each block is found in the circuit diagrams.

2.3 Functional Description 2.3

The functional description follows the block diagram. This paper does not contain a full description of all the functions of the VLSI circuits used in MIC702. This kind of informations may be supplied by the manufactures of the VLSI circuits.

2.3.1 CPU Description 2.3.1

A block diagram of the architecture of the Z-80A CPU is shown in fig. 2.3.1. The diagram shows all the major elements in the CPU and it should be referred to throughout the following description.

Z-80A CPU contains 208 bits of R/W memory that are accessible to the programmers. Fig. 2.3.2 illustrates how this memory is configured into eighteen 8-bit registers and four 16-bit registers.

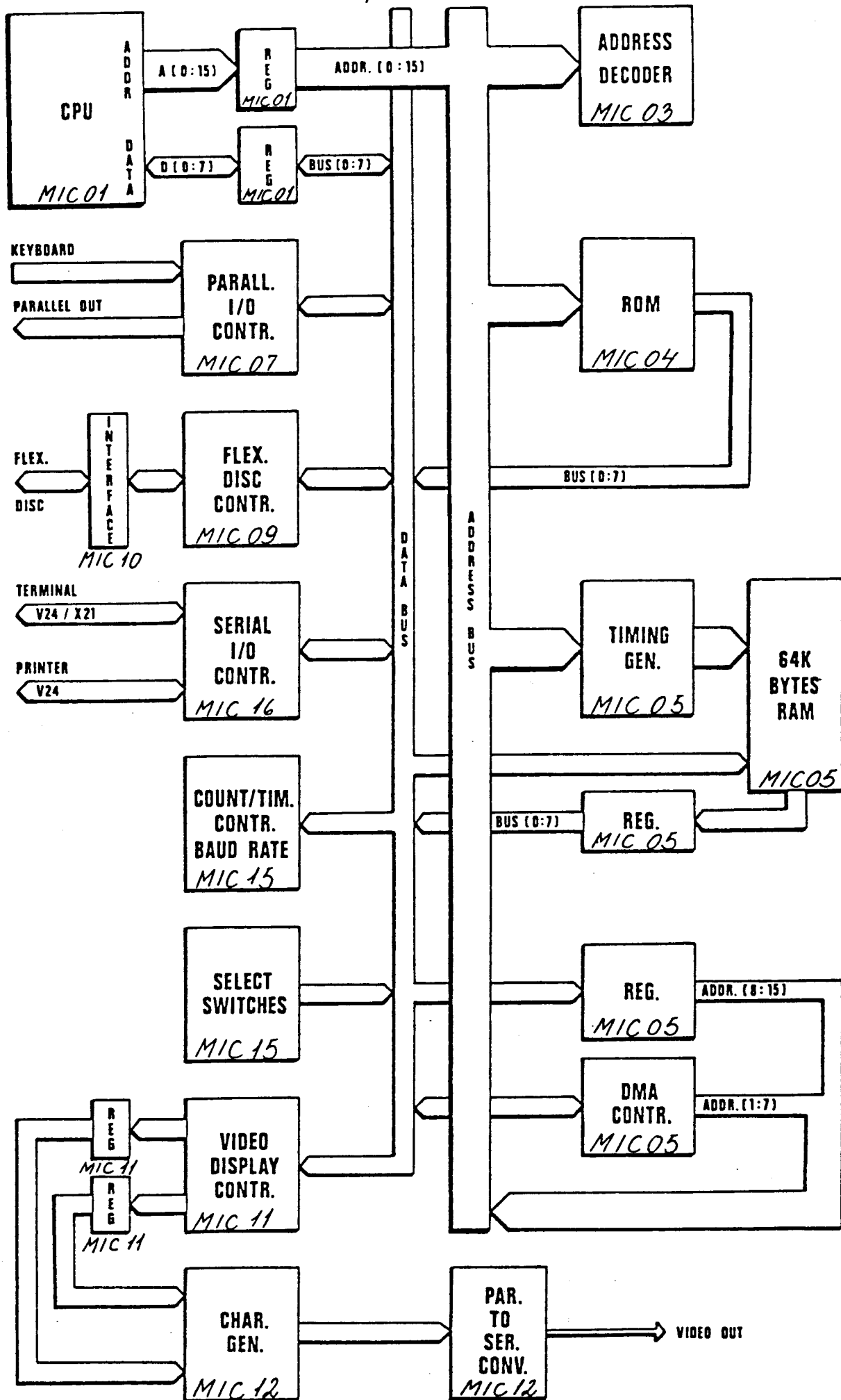


Fig. 2.2. Block Diagram RC 702.

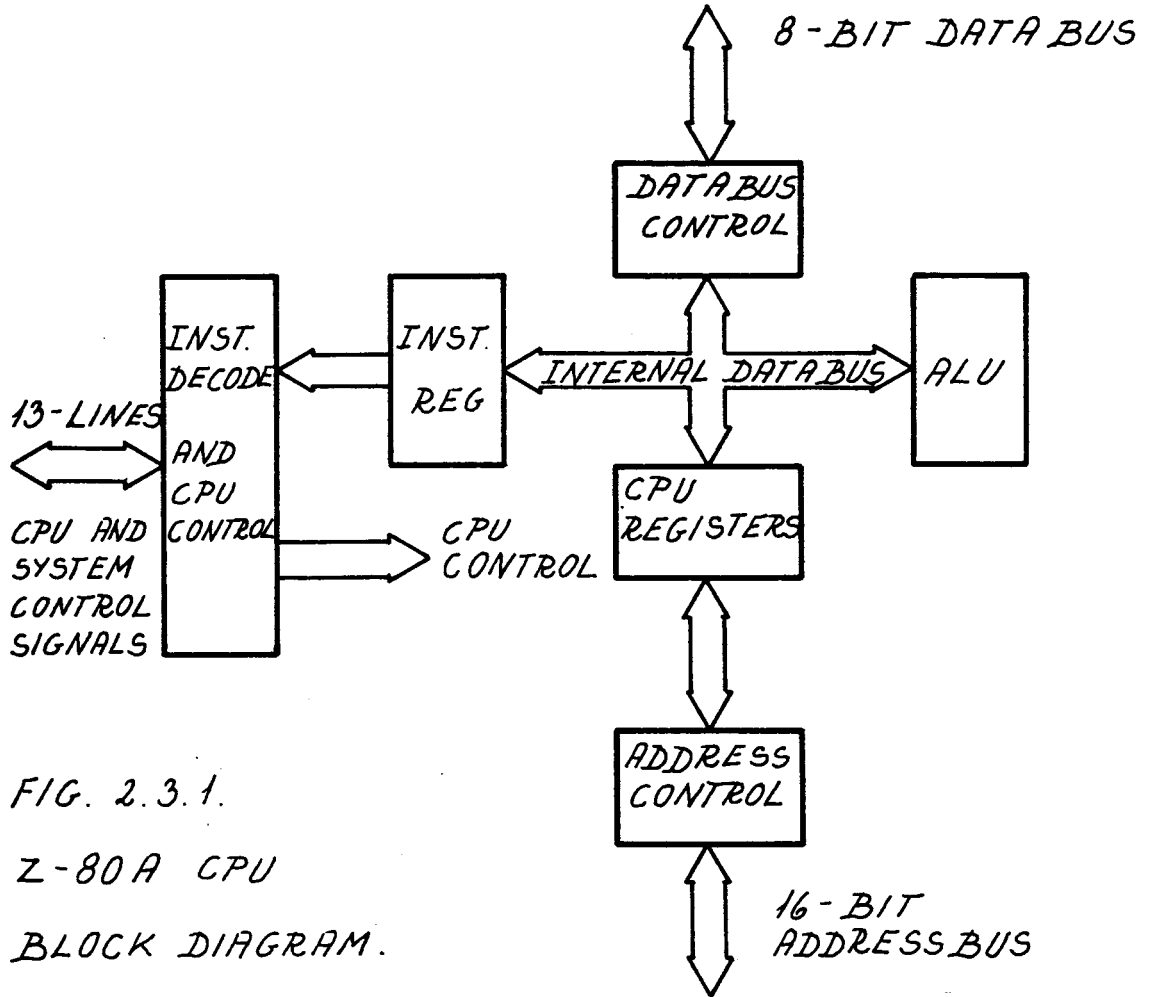


FIG. 2.3.1.
Z-80A CPU
BLOCK DIAGRAM.

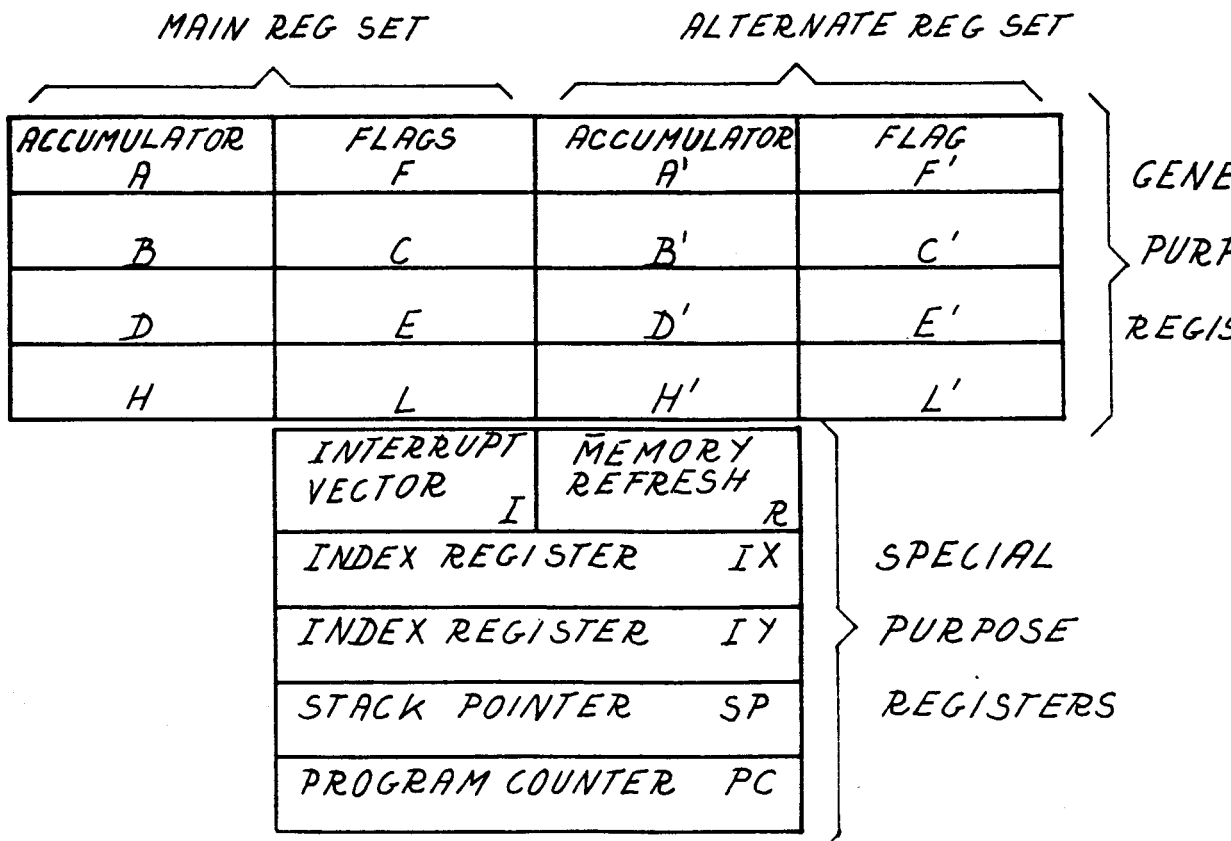


FIG. 2.3.2. Z-80A CPU REGISTERS

All Z-80A registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulators and flag registers.

CPU timing can be broken down into a few very simple timing diagrams. The diagrams show basic operations with one wait state (the wait state is added to synchronize the CPU to the RAM memory). Figs. 2.3.3 to 2.3.5 show the CPU timing.

The Z80A CPU can execute 158 different instruction types including all 78 of the 8.080A CPU. A description of this may be obtained from Zilog Z80A CPU Technical Manual.

2.3.2 Address Decoder

2.3.2

The addressing of devices is made very simple with the circuit shown in diagram page MIC03. Each device uses 4 addresses except the DMA controller which uses 16 addresses. This is shown in fig. 2.3.6.

Addressing of dynamic RAM and ROM is made using the PROM in Pos. 55. Most significant bit in the PROM is controlled by the flip-flop in Pos. 42. The flip-flop is reset by the RESET signal and set by the program using the following instruction:

```
OUT (18 Hex), A
```

The resulting addressing is shown in fig. 2.3.7.

This circuit makes it possible for the program to disconnect the program stored in PROM 0 and in PROM 1.

2.3.3 Parallel I/O Controller

2.3.3

The Z-80A parallel I/O (PIO) interface controller is a program-

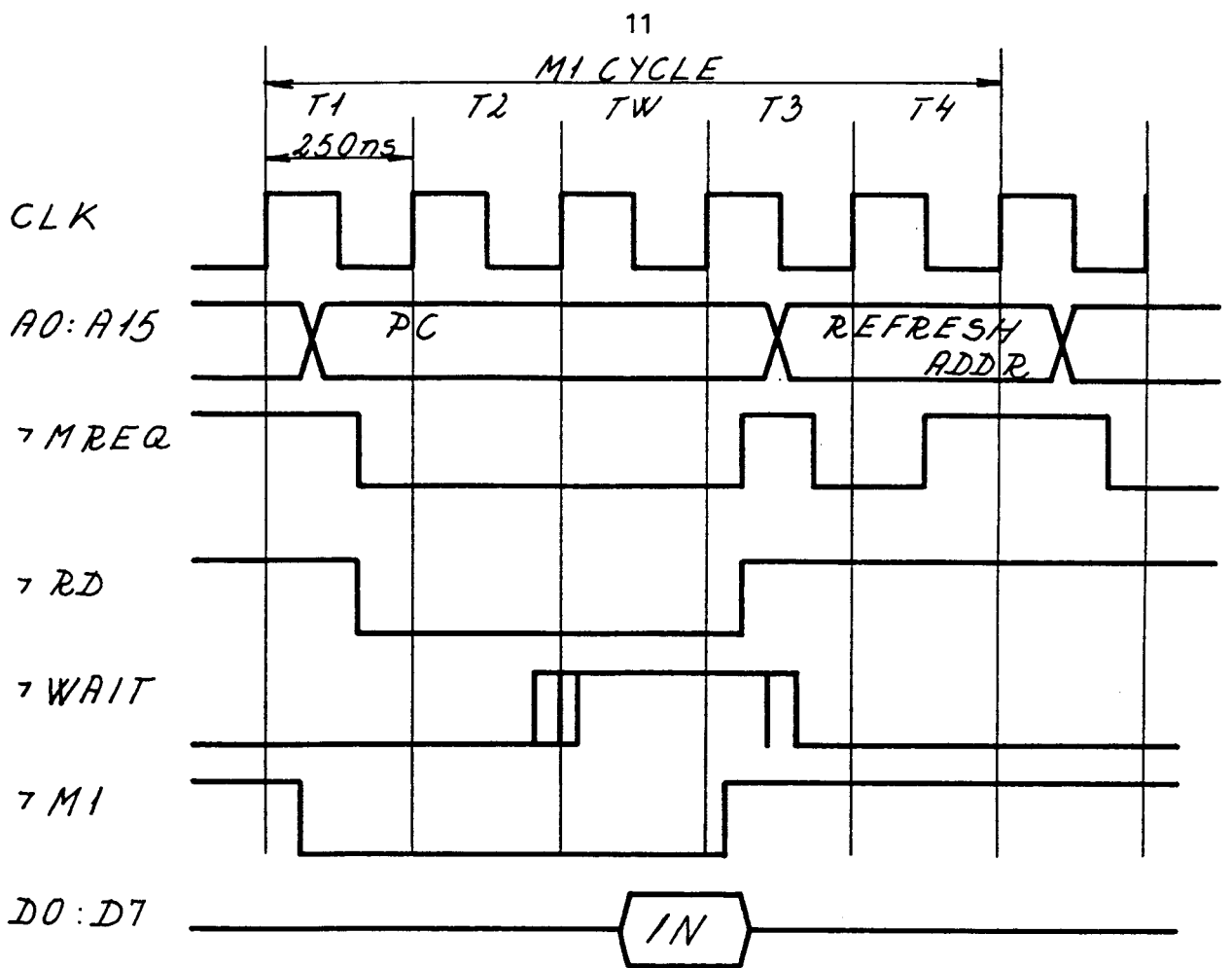


Fig. 2.3.3. INSTRUCTION OP CODE FETCH.

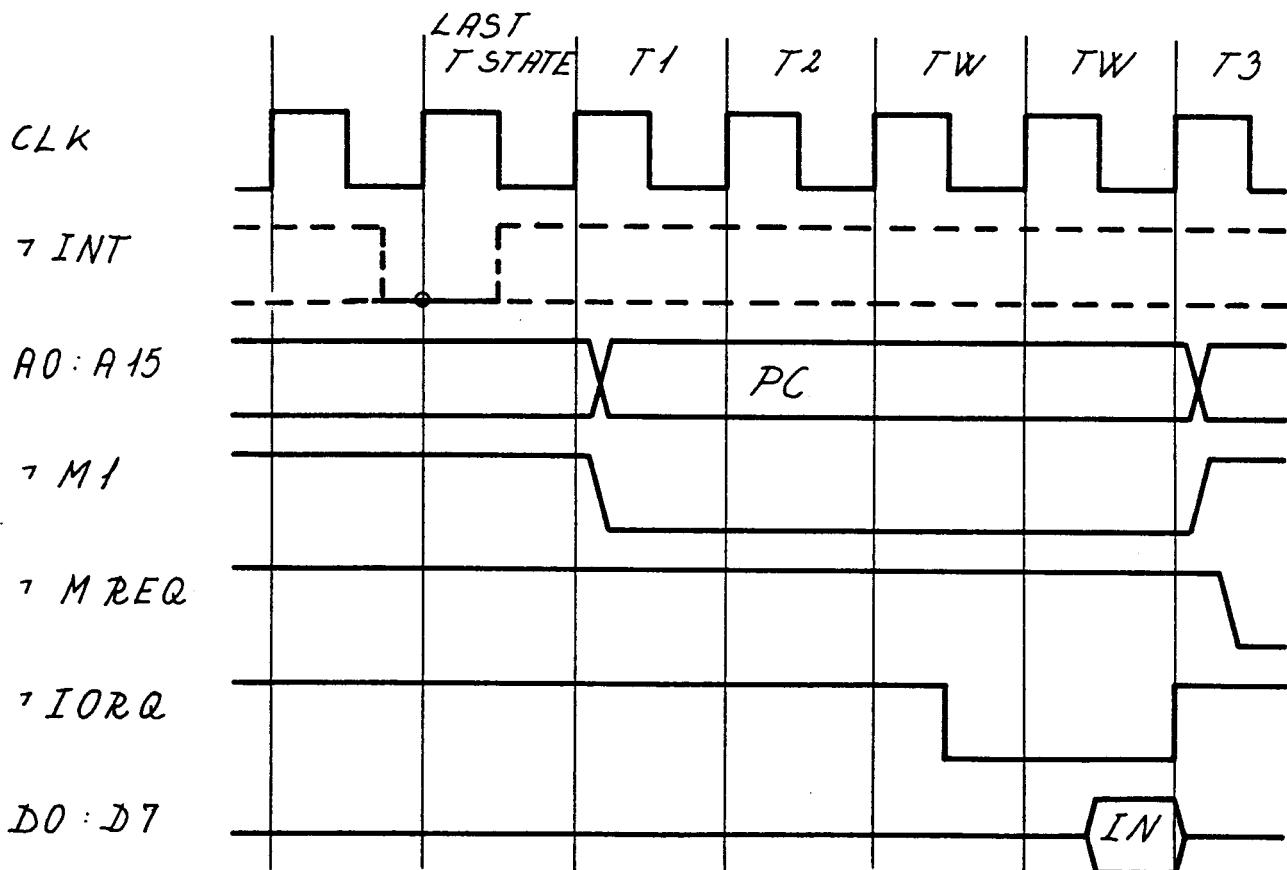


Fig. 2.3.4. INTERRUPT REQUEST/ACKNOWLEDGE.

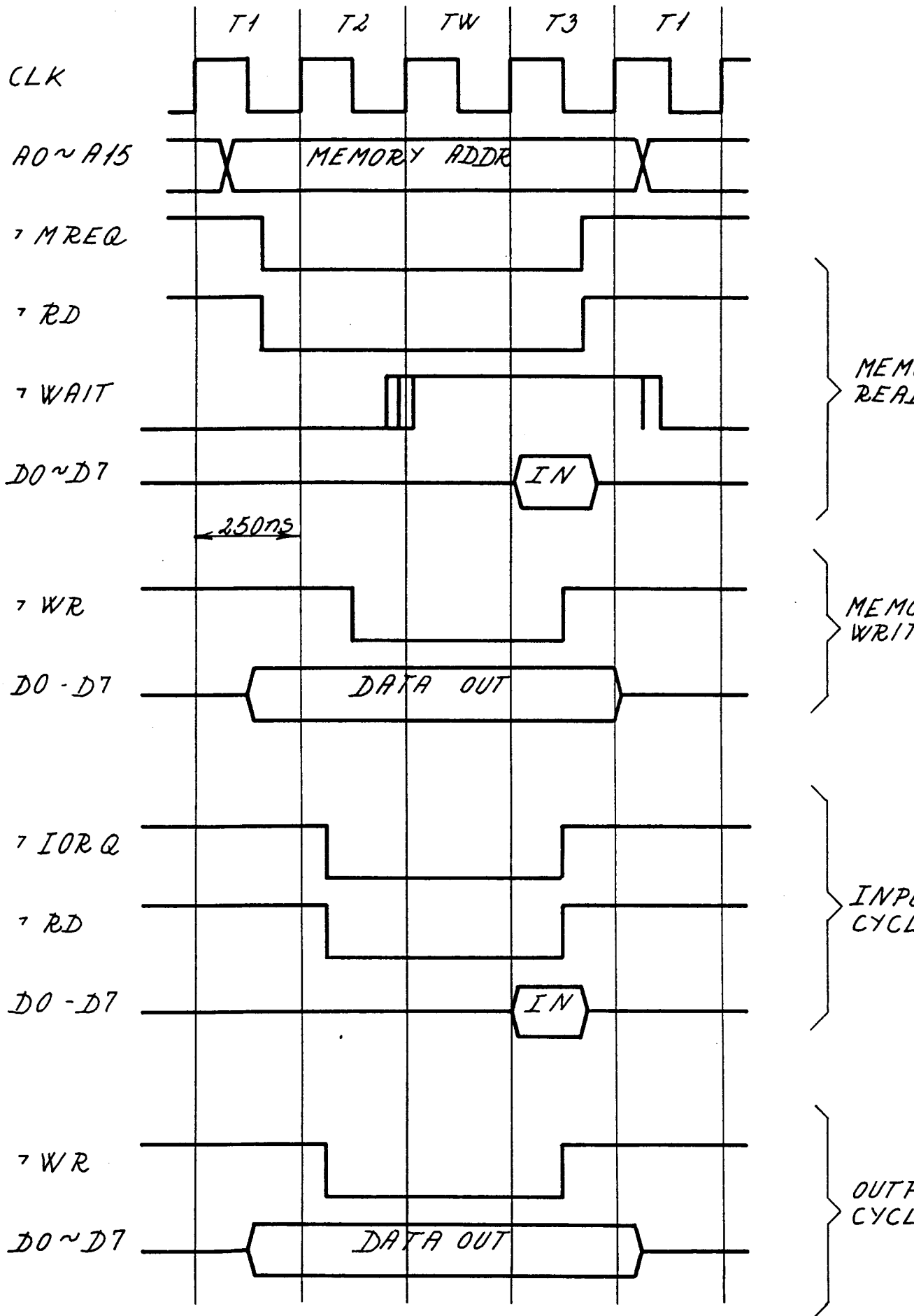


Fig. 2.3.5 TIMING WAVEFORM FOR Z-80A DIAGRAM

Address No.	Name	IC type	Comments
00	DISP	I 8275	PARAMETER PORT
01	-		COMMAND PORT
02	-		
03	-		
04	FLOP	μ PD 765	MAIN STATUS REG
05	-		DATA REG
06	-	or I 8272	
07	-		
08	SIO	Z 80A - SIO2	DATA CHANNEL A
09	-		DATA CHANNEL B
0A	-		CONTROL CHANNEL A
0B	-		CONTROL CHANNEL B
0C	CTC	Z 80A - CTC	CHANNEL 0 to SIOA
0D	-		CHANNEL 1 to SIO.B
0E	-		CHANNEL 2 INT DISP
0F	-		CHANNEL 3 INT FLOP
10	PIO	Z 80A - PIO	DATA KEYBOARD
11	-		DATA PARALLEL I/O
12	-		CONTROL KEYBOARD
13	-		CONTROL PARALLEL I/O
14	SWITCH		INPUT: 8 bit from switch
15	-		
16	-		OUTPUT: Enable Motor
17	-		to FLOP
18	DIS PROM		
19	-		
1A	-		
1B	-		
1C	SOUND		
1D	-		
1E	-		
1F	-		
20			
21			
EE			
EF			
F0	DMA	AM 9517A-4	Use of the 16 Registers
...	-	or	is described in the
...	-	I 8237-2	MANUFACTURER'S MANUAL
...	-		
...	-		
...	-		
FF	-		

Fig. 2.3.6. ADDRESS DECODING

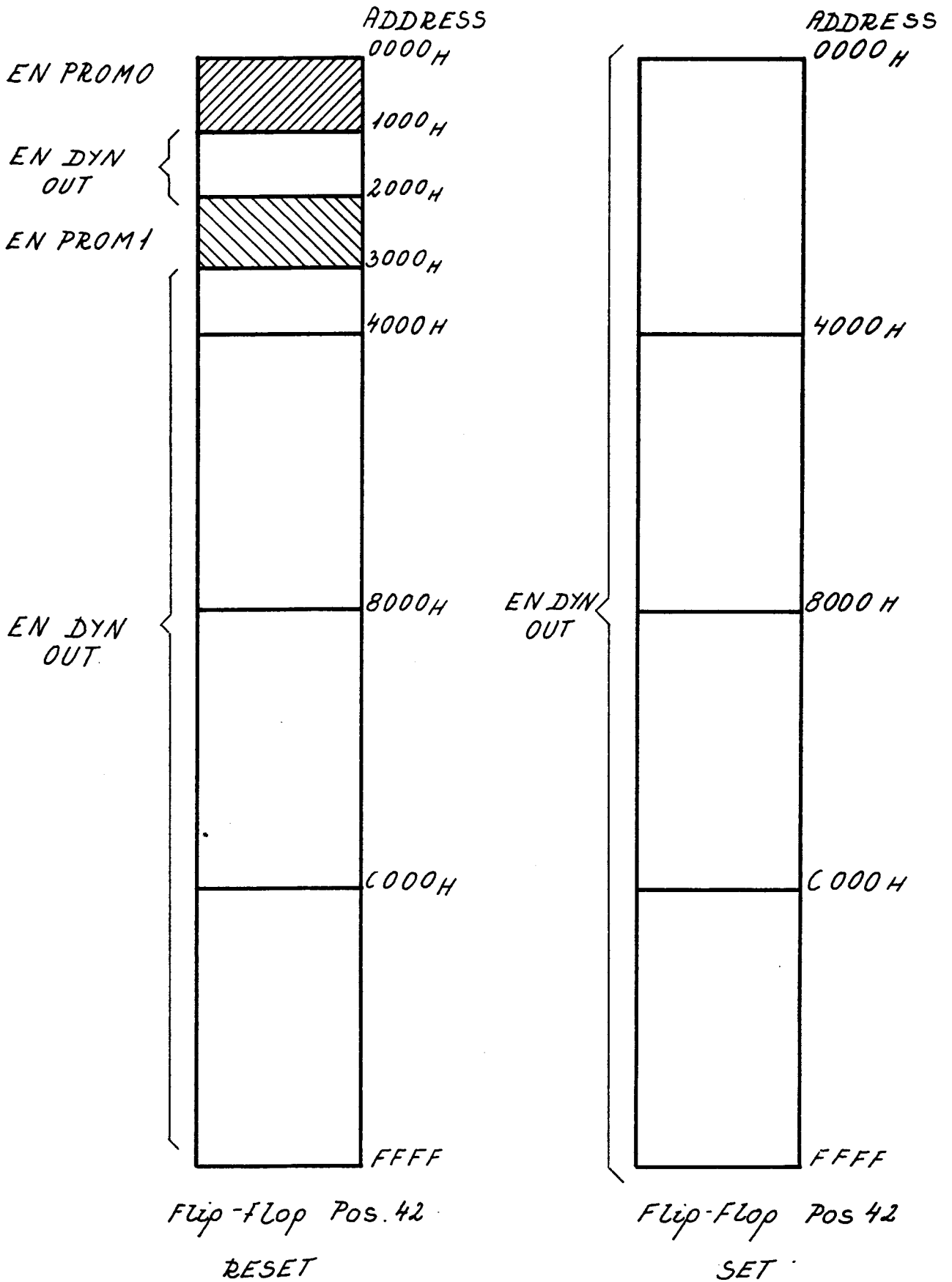


Fig 2.3.7. ADDRESS SPACE IN MIC 702.

mable, two port device which provides interface between the CPU and the two connectors for keyboard and for parallel I/O. The diagram is shown on page MIC07. The block diagram is shown in fig. 2.3.8. The internal structure of the Z80A-PIO consists of a bus interface, internal control logic, port A I/O logic, port B I/O logic, and interrupt control logic.

Each of the two port I/O logic is composed of 6 registers. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit moderegister, an 8-bit mask register, an 8-bit input/output select register, and a 2-bit mask control register.

Before using the PIO it has to be programmed to the wanted Interrupt Vector and operating mode. This is described in manuals from Zilog.

The timing diagram in fig. 2.3.9 shows input from keyboard. The interrupt system is described in subsection 2.3.7.

2.3.4 Serial Input/Output Controller

2.3.4

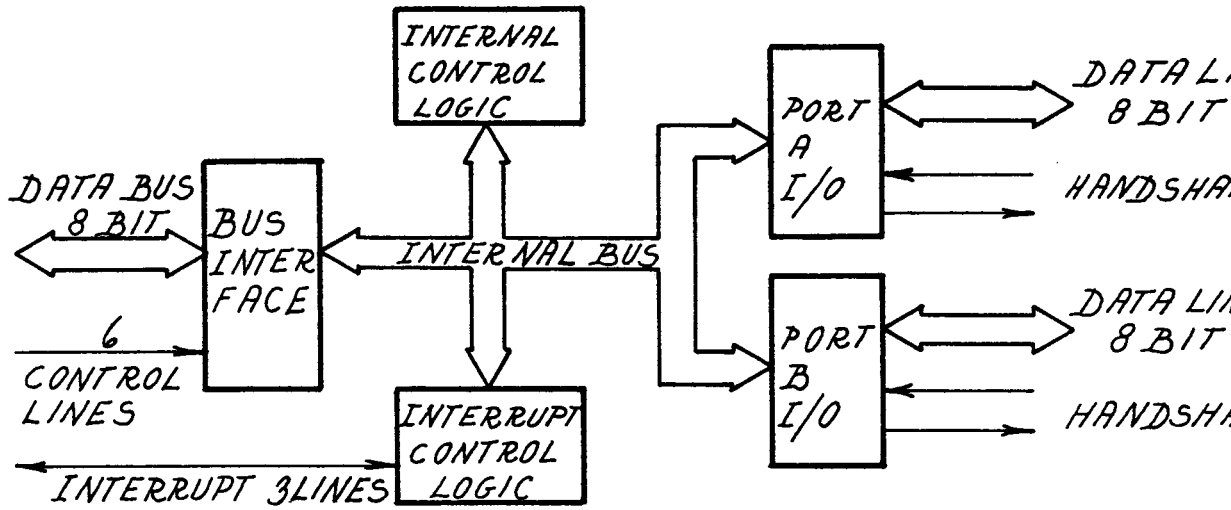
The Z80-SIO/2 (Serial Input/Output) is a dual-channel multi-function peripheral component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but - within that role - it is configurable by system software so its "personality" can be optimized for a given serial data communications application.

The Z80-SIO/2 is in RC702 capable of handling asynchronous formats.

The Z80-SIO/2 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. Block diagram for the Z80-SIO/2 is shown in fig.

2.3.10.

The internal structure includes Z80A CPU interface, internal con-



* HANDSHAKE not used to KEYBOARD

Fig. 2.3.8. BLOCK DIAGRAM Z-80A PIO

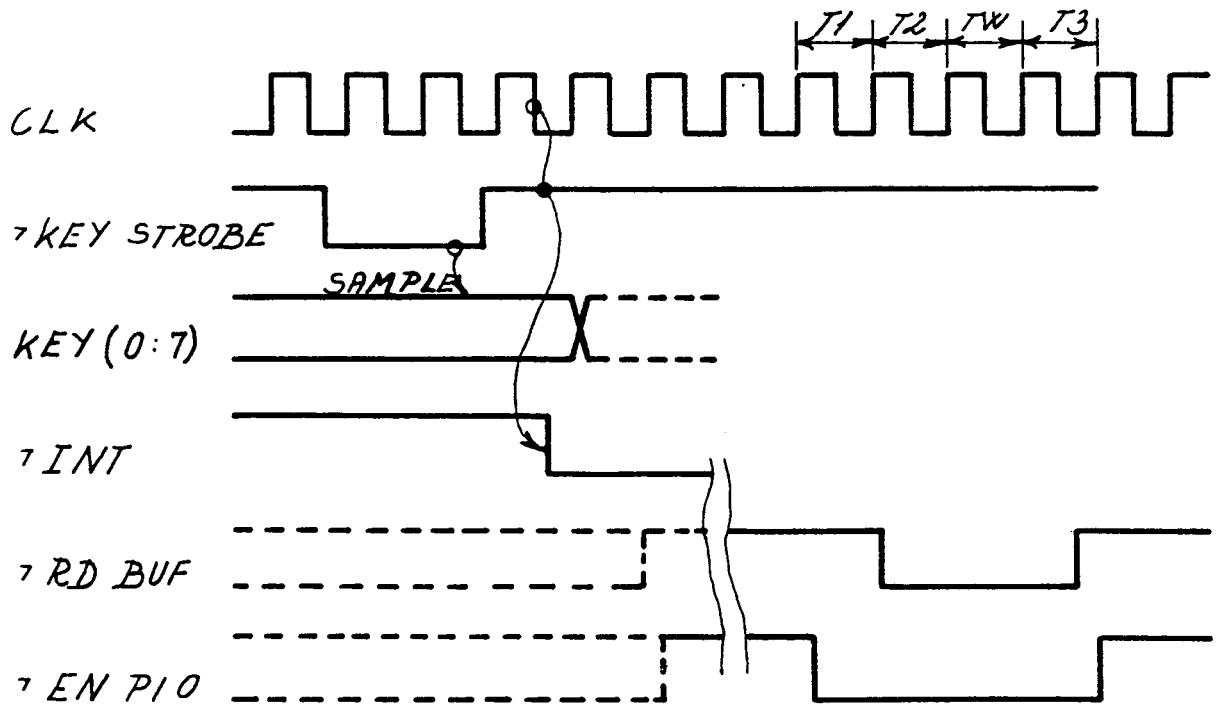


FIG. 2.3.9. TIMING DIAGRAM SHOWING INPUT FROM KEYBOARD

trol and interrupt logic, and two full duplex channels. Each channel contains read and write registers, and discreet control and status logic that provides interface to modems.

The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs, Clear to Send (CTS) and Data Carrier Detect (DCD) are monitored by the discreet control logic under program control. All the modem control signals are general purpose in nature.

The programming for the SIO/2 is very complex and is described in manuals from Zilog.

2.3.5 Counter Timer Controller

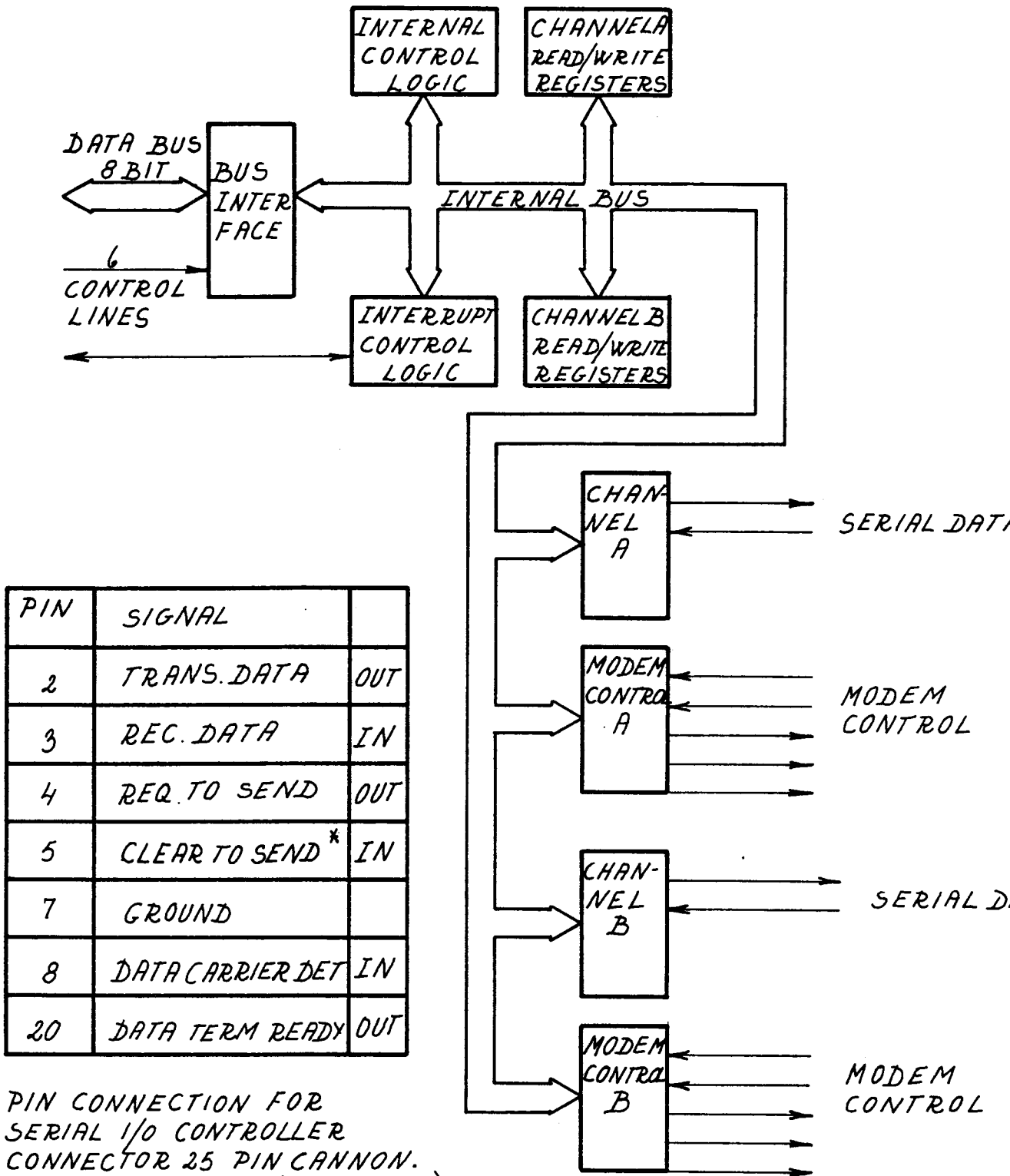
2.3.5

The Z80A Counter Timer Controller (CTC) is a programmable four channel device that provides counting and timing functions for the system. The diagram is shown in page MIC15 and the block diagram is shown in fig. 2.3.11.

The internal structure of the Z80-CTC consists of a Z80 CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel 0 having the highest priority.

The channel logic is composed of 2 registers, 2 counters, and control logic as shown in fig. 2.3.12. The registers include an 8-bit constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

Channel 0 and 1 are used to generate the clock to channel A and B in the Z80A-SIO/2. The clock delivered to the SIO is again divided in the SIO to make the baudrate for the terminal and printer connections. Input to these two channels is a clock of



PIN	SIGNAL	
2	TRANS. DATA	OUT
3	REC. DATA	IN
4	REQ. TO SEND	OUT
5	CLEAR TO SEND *	IN
7	GROUND	
8	DATA CARRIER DET	IN
20	DATA TERM READY	OUT

PIN CONNECTION FOR SERIAL I/O CONTROLLER
 CONNECTOR 25 PIN CANNON.
 CHANNEL A TO J1 (TERMINAL)
 CHANNEL B TO J2 (PRINTER)
 * IF PRINTER CONNECTOR TO 7 BUSY.

Fig. 2.3.10. BLOCK DIAGRAM FOR Z-80A SIO/2
 AND SIGNAL CONNECTION TO J1 AND J2.

0.614 MHz. How the clock is divided in the SIO is shown in fig. 2.3.13.

Channel 2 and 3 are initiated in counter mode with interrupt enabled and with a time constant of 1. This means that for every clock input an interrupt is sent to the CPU. Channel 2 is connected to the display controller and channel 3 is connected to the floppy controller, and in this way their interrupt is connected to the CPU.

2.3.6 Interrupt System

2.3.6

The CPU has two interrupt inputs, a software maskable interrupt and a non-maskable interrupt. The non-maskable interrupt (NMI) cannot be disabled by the program and is not used in MIC702. The CPU can be programmed to respond to maskable interrupts in one of three modes. In MIC702 mode 2 is selected. In this mode a single 8-bit byte from the controller (the interrupt vector) is used to make an indirect call instruction.

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted a special M1 cycle (INTA) is generated. During this M1 cycle IORQ becomes active (instead of MREQ) indicating the INTA cycle. The Z80 peripherals have an interrupt enable input (IEI) and an interrupt enable output (IEO) and are connected in daisy chain. The peripheral with IEI high and IEO low, will during INTA place the preprogrammed 8-bit interrupt vector on the data bus.

IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the peripheral for this purpose.

Fig. 2.3.14 shows the daisy chain interrupt system in MIC702.

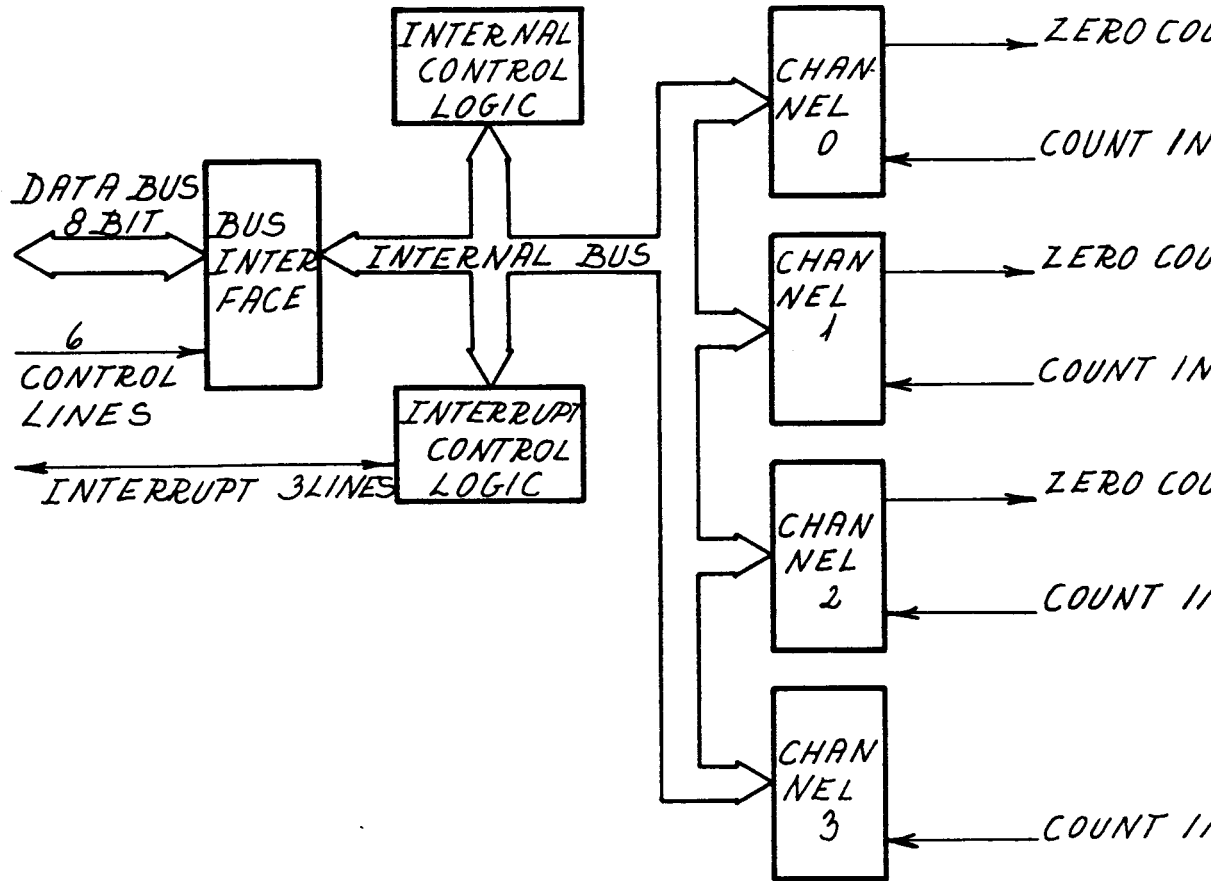


Fig. 2.3.11. BLOCK DIAGRAM FOR Z-80A CTC.

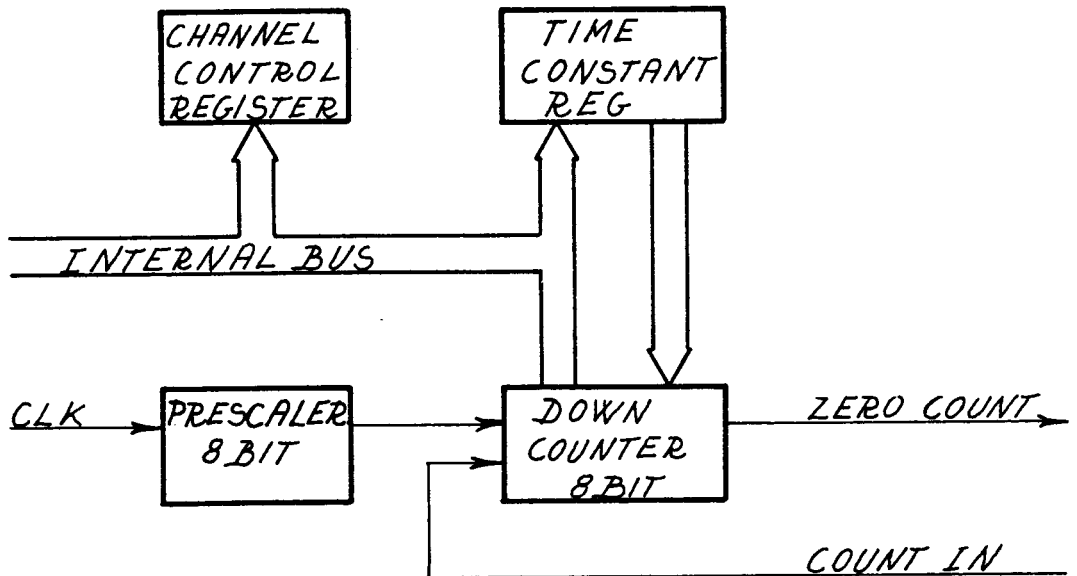
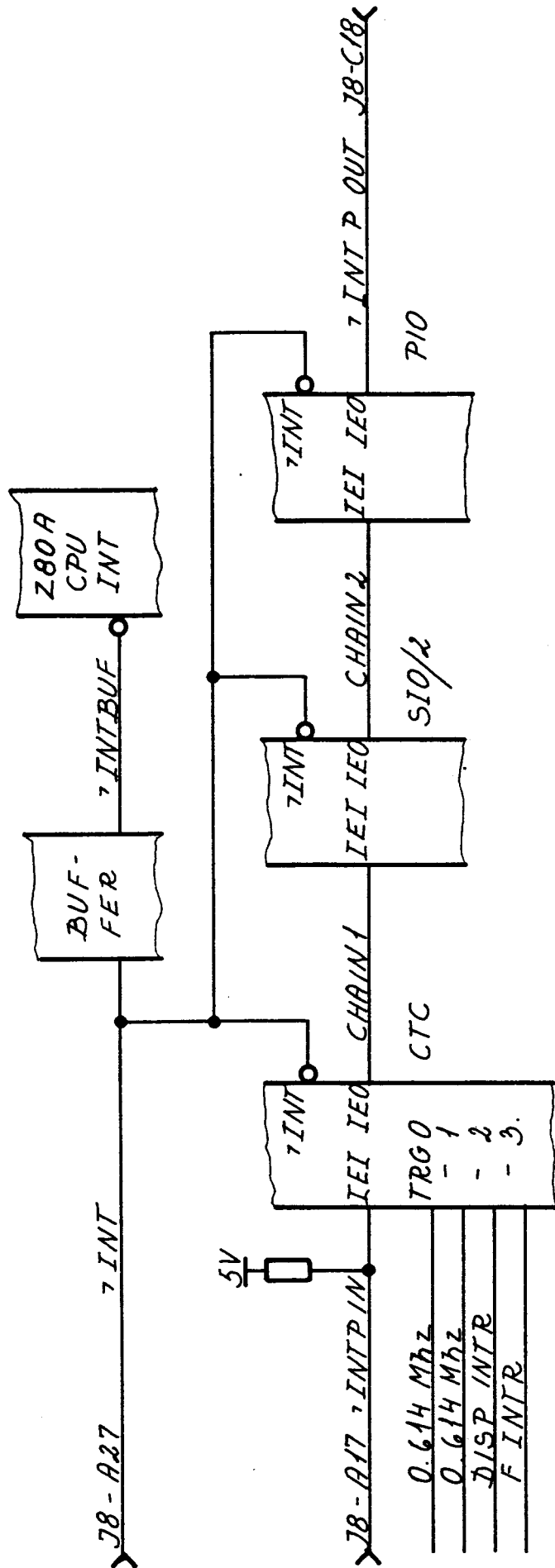


Fig. 2.3.12. BLOCK DIAGRAM for ONE CHANNEL in Z-80A CTC.

CTC INPUT	CLOCK Divided by	CTC OUTPUT	SIO Divided by	SIO Periodic time	SIO BAUDRATE
T in μsec	decimal	T in μsec	decimal	μsec	
0.614	193	314	64	19.970	50
0.614	128	208	64	13.310	75
0.614	88	144	64	9.222	110
0.614	64	104	64	6.667	150
0.614	32	52	64	3.333	300
0.614	64	104	16	1.667	600
0.614	32	52	16	833.3	1200
0.614	16	26	16	416.7	2400
0.614	8	13	16	208.3	4800
0.614	64	104	1	104.2	9600
0.614	32	52	1	52.1	19200

Fig. 2.3.13. GENERATING BAUDRATE in RC 702.



NAME	IC	COMMENT
BAUD RATE A	CTC	INT. NOT ENABLED
BAUD RATE B	CTC	-
DISPLAY CONTROLLER FLOPPY	CTC	-
SERIAL A	SIO/2	TERMINAL
SERIAL B	SIO/2	PRINTER
PARALLEL A	PIO	KEYBOARD
PARALLEL B	PIO	PARALLEL I/O

HIGHEST PRIORITY →

← LOWEST PRIORITY

Fig. 2.3.14. INTERRUPT PRIORITY IN RC702

2.3.7 ROM Memory

2.3.7

The ROM, Read Only Memory, contains the autoloader program. After a reset signal is generated, the CPU starts to execute the program stored in POS. 66. In subsection 2.3.3 is shown how this addressing is made. In a test situation both ROM POS. 66 and 65 may contain a ROM. The ROMs are normally 2 K bytes PROM.

2.3.8 RAM Memory

2.3.8

The RAM, Random Access Memory, is shown in 3 blocks in the block diagram: the TIMING GEN block, the 64 K BYTES RAM block, and the REG. block. This subsection describes these 3 blocks. The circuit diagram is on page MIC05. The timing generator is made using the IC I8202. This circuit makes all the signals which the RAM circuits need. Fig. 2.3.15 shows the block diagram for the I8202 and the timing diagram for the whole RAM circuit is shown in fig. 2.3.16.

2.3.9 DMA Controller

2.3.9

The DMA controller to MIC702 is based on the Am9517A-4 from Advance Micro Devices or an 8237-2 from Intel. The IC is designed to be used in conjunction with an external 8-bit address register made by an 74LS373. The circuit diagram is shown in MIC06. The Am9517A-4 contains 4 channels which have full 64 K address and word count capability.

The four channels are in MIC702 used in the following way:

- channel 0 : External debugger
- channel 1 : Floppy disk controller
- channel 2 : Visual display controller
- channel 3 : Visual display controller.

The block diagram for Am9517A-4 is shown in fig. 2.3.17.

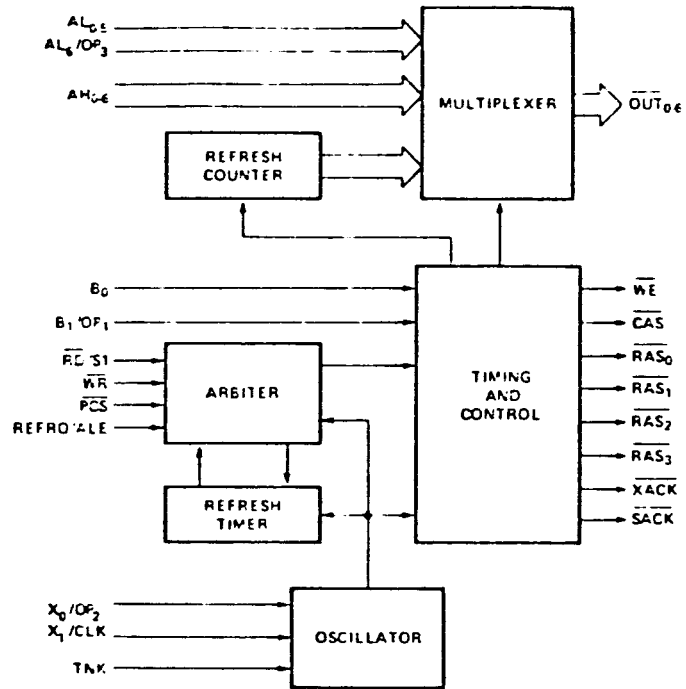


Fig. 2.3.15 Block Diagram for I 8202
RAM Controller

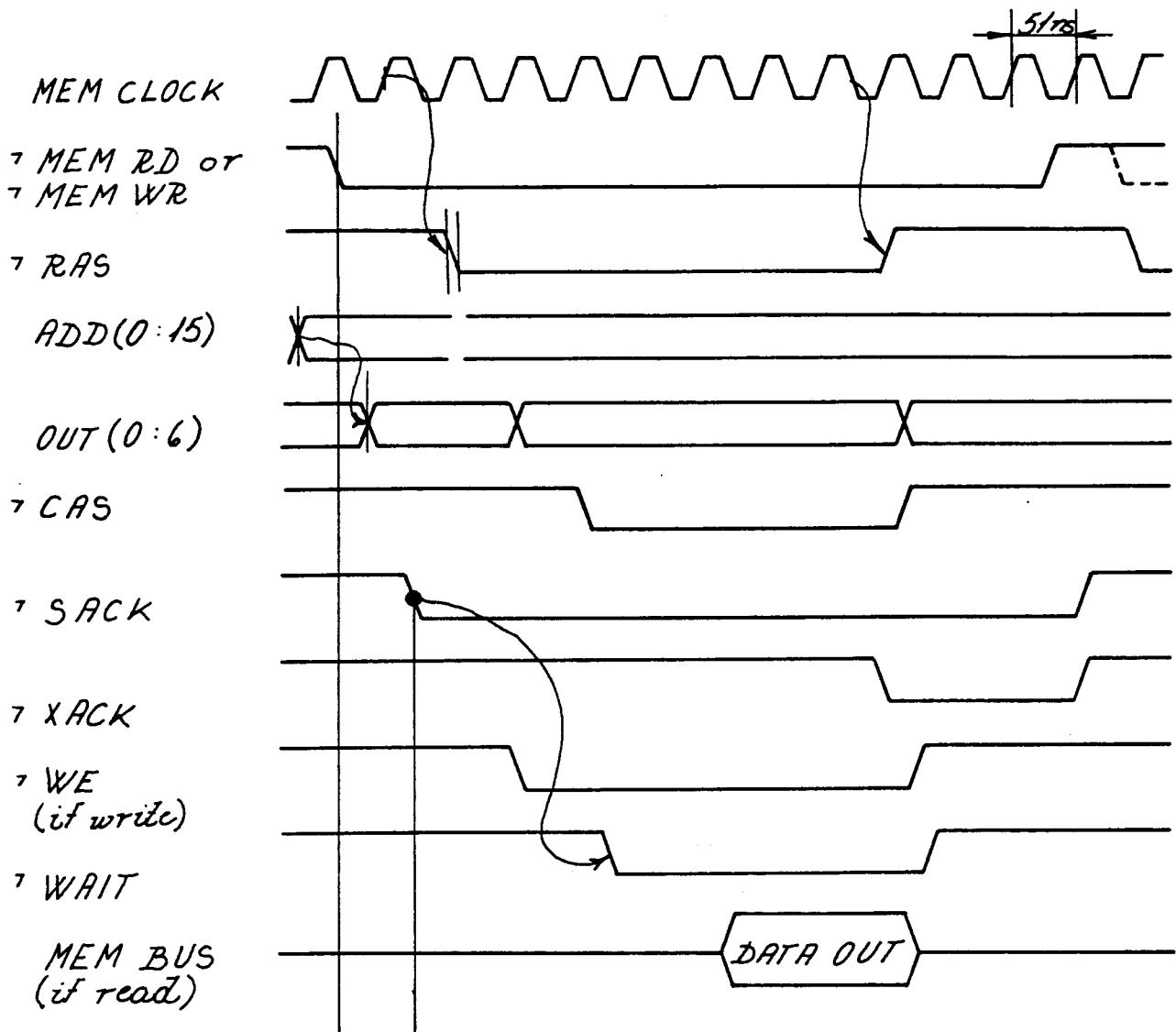


Fig. 2.3.16. TIMING DIAGRAM for RAM SYSTEM

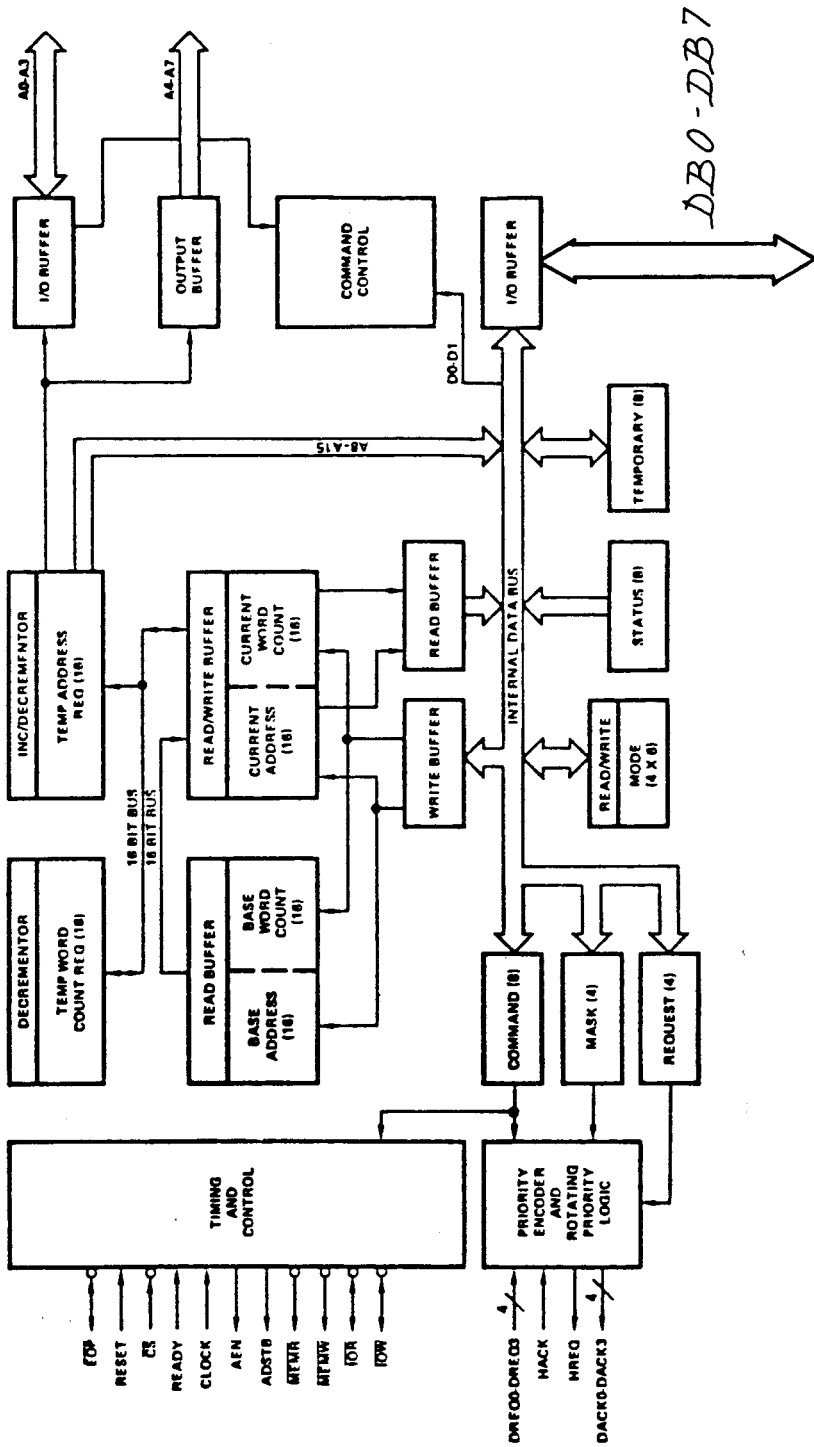
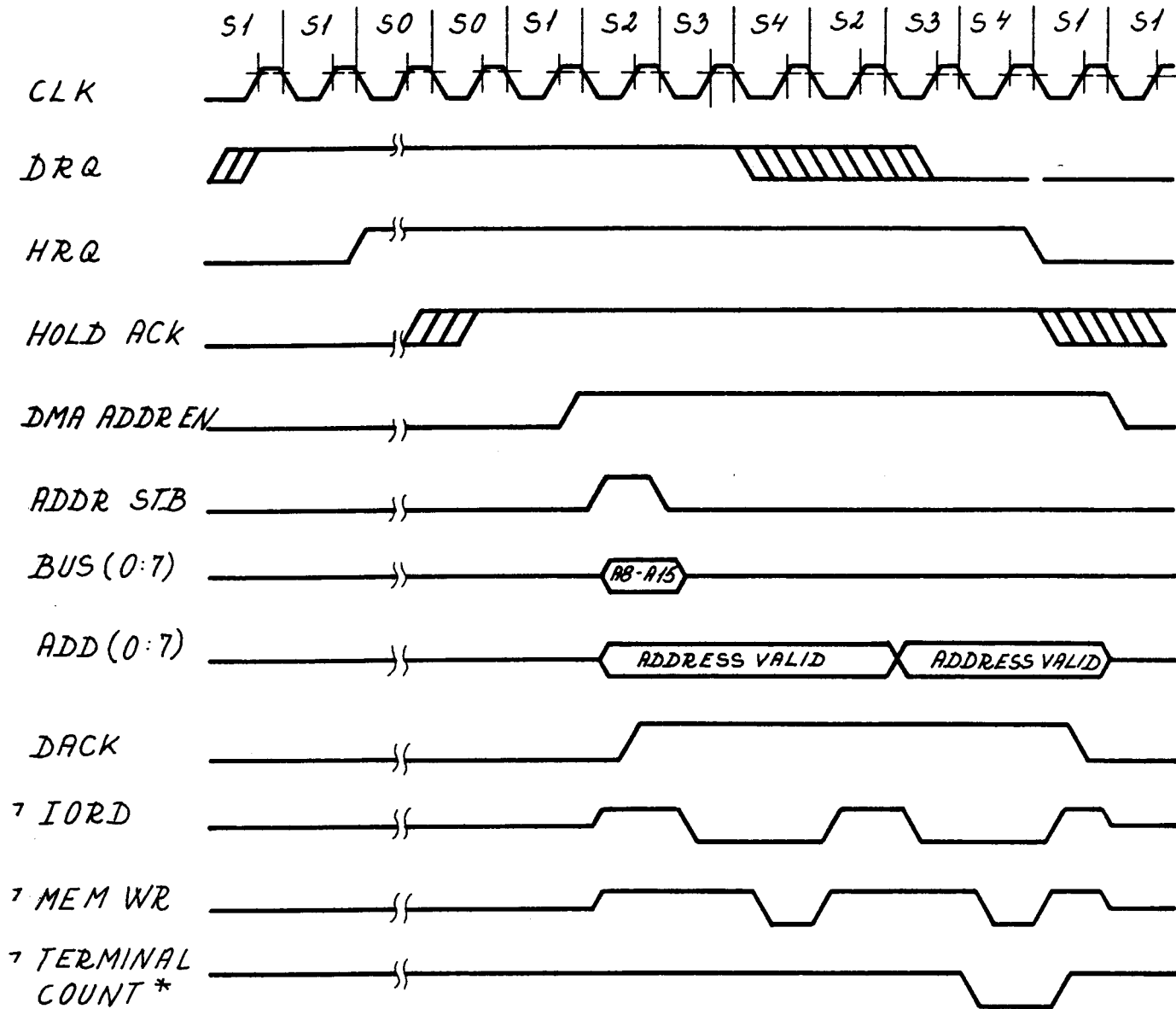


Fig. 2.3.17. Block Diagram for Am 9517A-4.



* Only if last byte in the block.

Fig. 2.3.18. TIMING DIAGRAM for Am 9517A-4
DMA-CONTROLLER.

Fig. 2.3.18 shows the timing diagram for a normal operation of Am9517A-4.

More specific description of the units. may be obtained from one of the two manufacturers.

2.3.10 Select Switches

2.3.10

8 switches are situated on the board. Their position may be sensed by the program. The switches are mainly used when the ROM is replaced with a testprogram ROM. One switch (BUS 7) is used to switch between Mini and Maxi floppy. The circuit may be seen in diagram MIC15.

2.3.11 Video Display Controller

2.3.11

The video display controller is based on the 8275 programmable CRT controller from Intel. The device interfaces the CRT raster scan display with the system. The controller refreshes the display by buffering the information from the memory and it keeps track of the display position of the screen. Fig. 2.3.19 shows a block diagram for the 8275 controller. The program initiates the controller to make the wanted picture. The initiations needed may be seen in the description from Intel.

The initiation made in MIC702 is listed in fig. 2.3.20.

The video display controller needs a number of registers, etc. to support it. This circuits are shown in diagram pages MIC11 to MIC14. Fig. 2.3.21 shows a block diagram with this circuit.

The output from the video display controller system is made with comp. sync and with normal TTL signal output. In RC702 the comp. sync. is used and fig. 2.3.22 shows the timing of this signal.

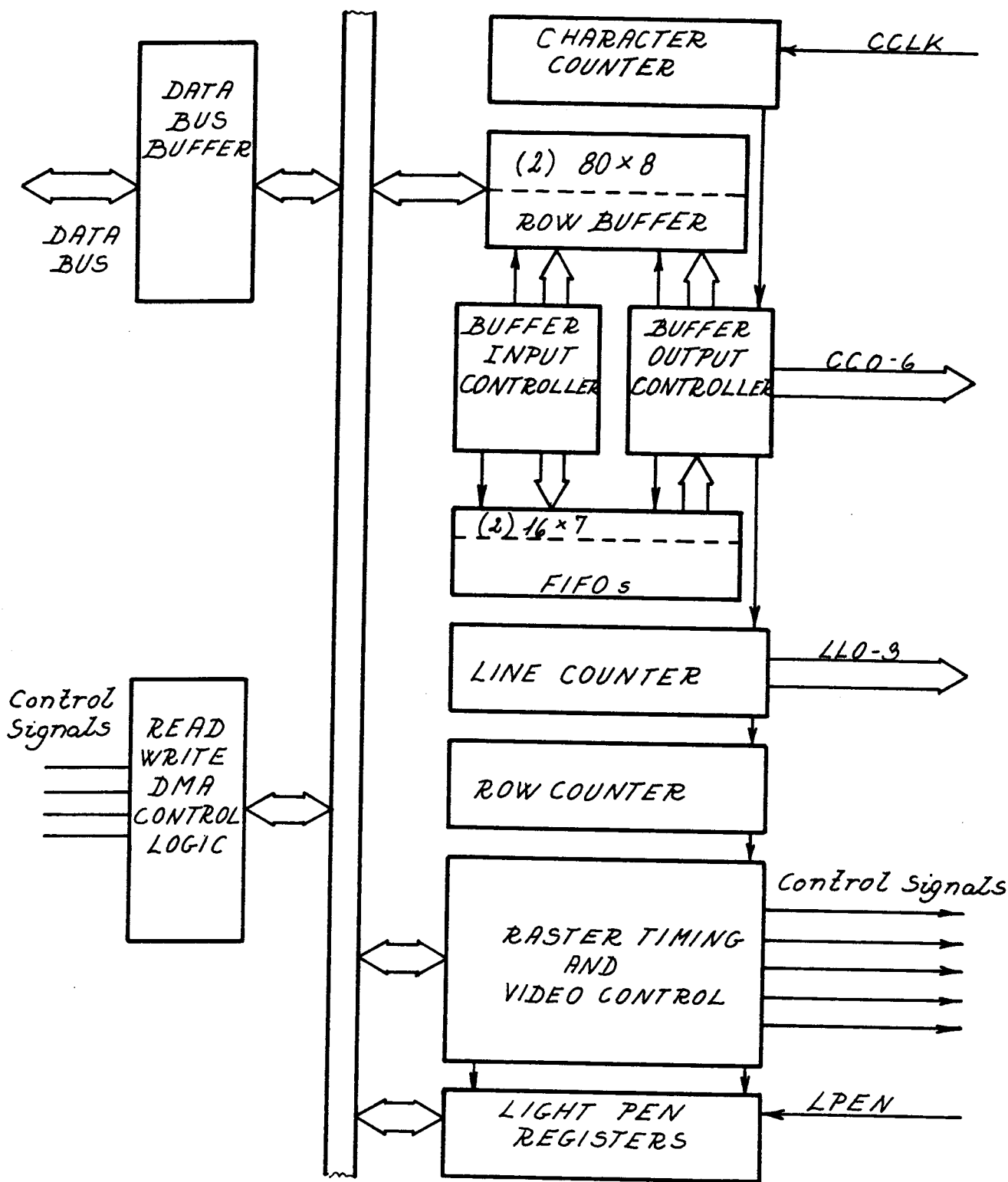


Fig. 2.3.19 BLOCK DIAGRAM FOR 8275.

Initiation of 8275 makes the following picture on the monitor used.

		Comments
80	Chars pr. row	
25	Rows of characters	
5	Char. Dot matrix width	Made in Char. generator
9	- - - height	- - - -
7	Char cell width	
11	- - height	
50 Hz	frame frequency	sync. with mains freq.
275	active scan lines	
33	vertical blanking intervals	
308	Total scan lines	
15.4 kHz	line frequency	
65 μ sec	line period time	
150 μ sec	vertical sync time	Made with monostable
28	char. time for horz. blank	
108	char. time each line	
0.601 μ sec	char time	
86 nsec	DOT time	
11.64 MHz	DOT frequency	
4.5 μ sec	Horizontal sync width	Made with monostable
5, 8 μ sec	- - - delay	- - -
	Blinking field cursor	

Fig. 2.3.20. INITIATION of 8275 in MIC 702.

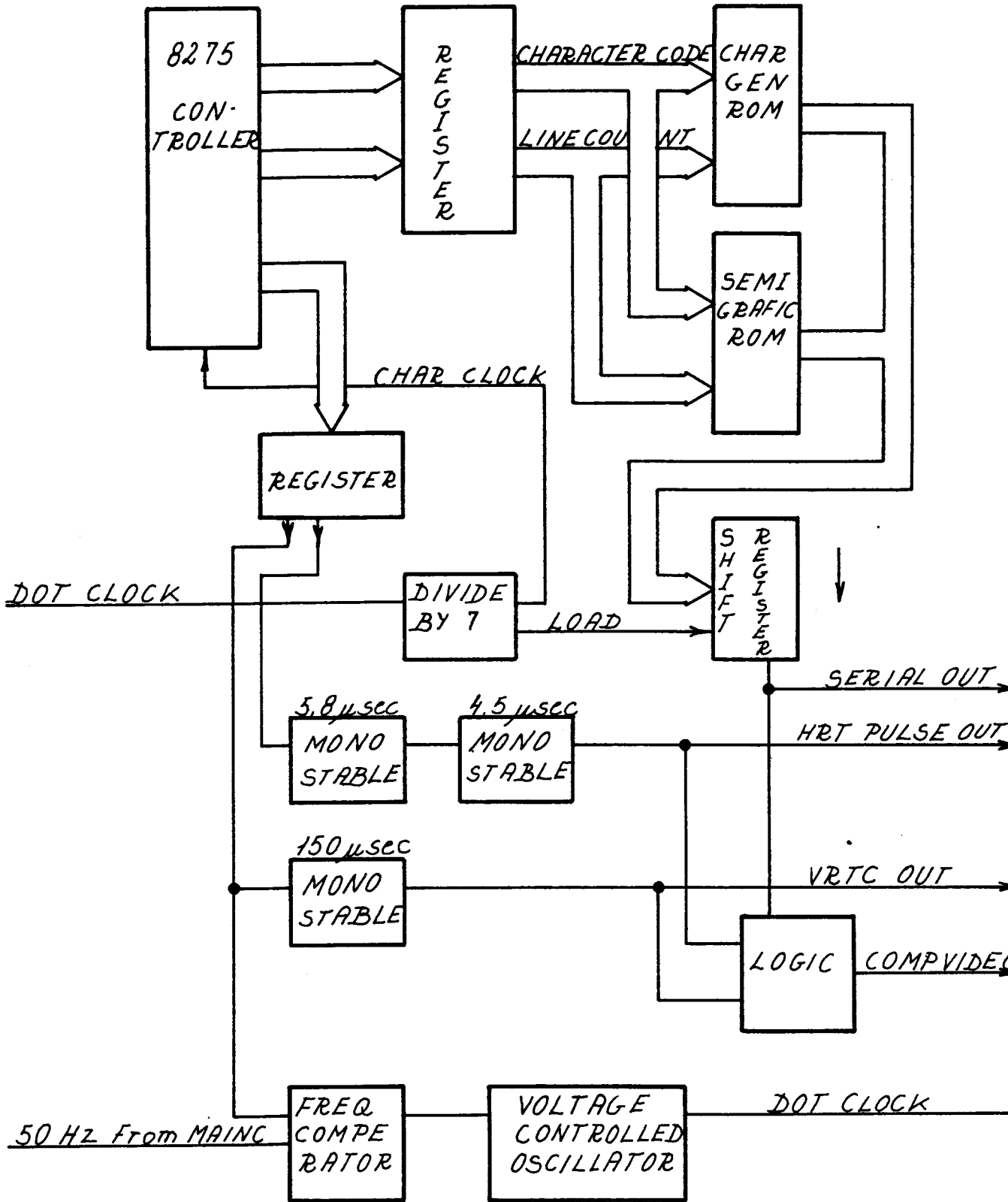
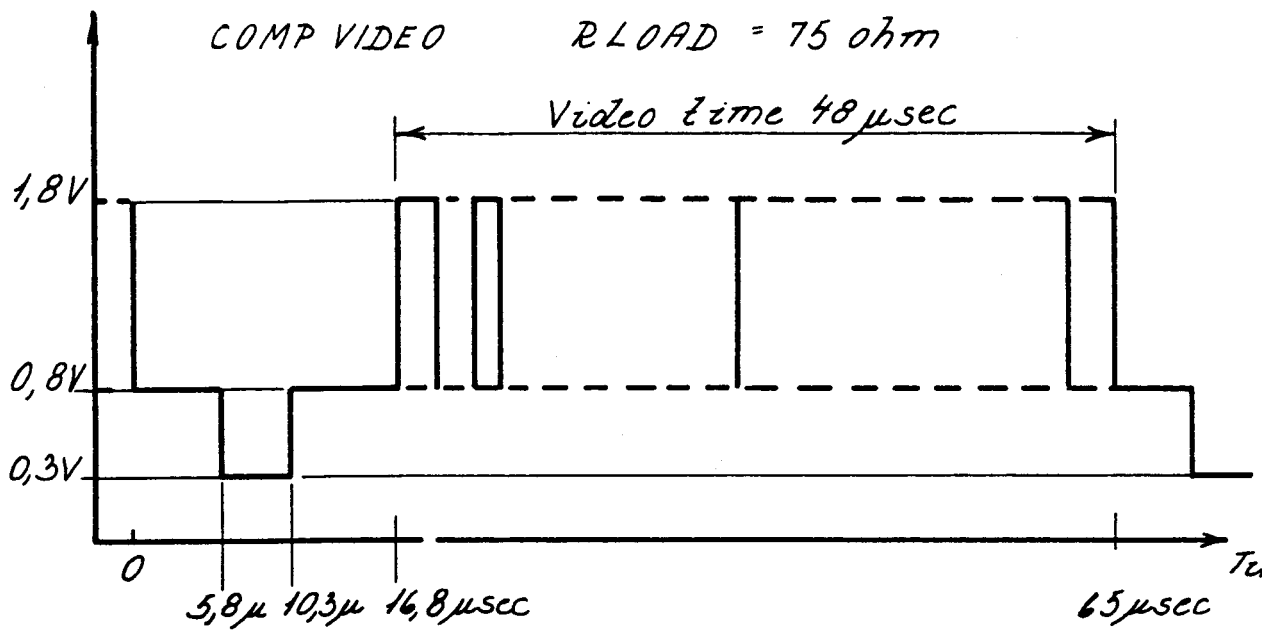
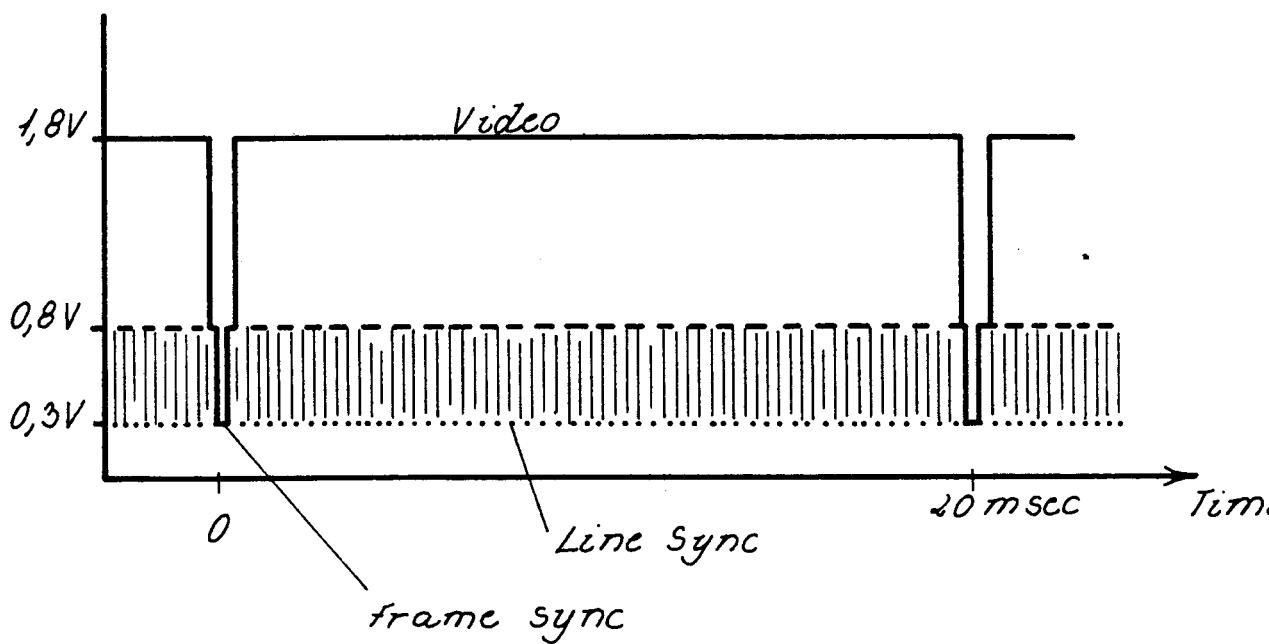


Fig. 2.3.21. BLOCK DIAGRAM FOR VIDEO DISPLAY SYSTEM
NOTE ONLY COMP SYNC IS USED I MIC 702.



Comp. Sync signal for one Line.



Comp. Sync signal for one frame.

Fig. 2.3.22. TIMING DIAGRAM COMP. SYNC SIGNAL
TO RC 702.

The floppy disk controller to MIC702 is based on the FDC chip uPD765 from NEC or 8272 from Intel. The chip contains the circuitry and control functions for interfacing the processor to 4 floppy disk drives. It supports both IBM3740 single density format (FM) and IBM system 34 double density format including double sided recording.

Fig. 2.3.23 shows a block diagram for the controller chip.

The uPD765 contains two registers which may be accessed by the program. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consists of several registers in stack with only one register present to the bus at a time), which stores data, commands, parameters, and floppy disk drive information. Fig. 2.3.24 shows the information stored in the status register.

Fig. 2.3.25 shows the information delivered to and from the data register during a read or write instruction to the controller. The programming of uPD765 is very complex and is described by the manufacturer. The controller interfaced to both Maxi- and Mini disk drives. The circuits on diagrams MIC09 and MIC10 show this.

Fig. 2.3.26 shows the data media floppy diskette. The diskette contains a number of tracks which again are divided into a number of sectors as shown in fig. 2.3.26. The controller is able to format, read, or write the diskette. Information about the actual formats used is available in the software manuals. Fig. 2.3.28 shows the two recording methods used.

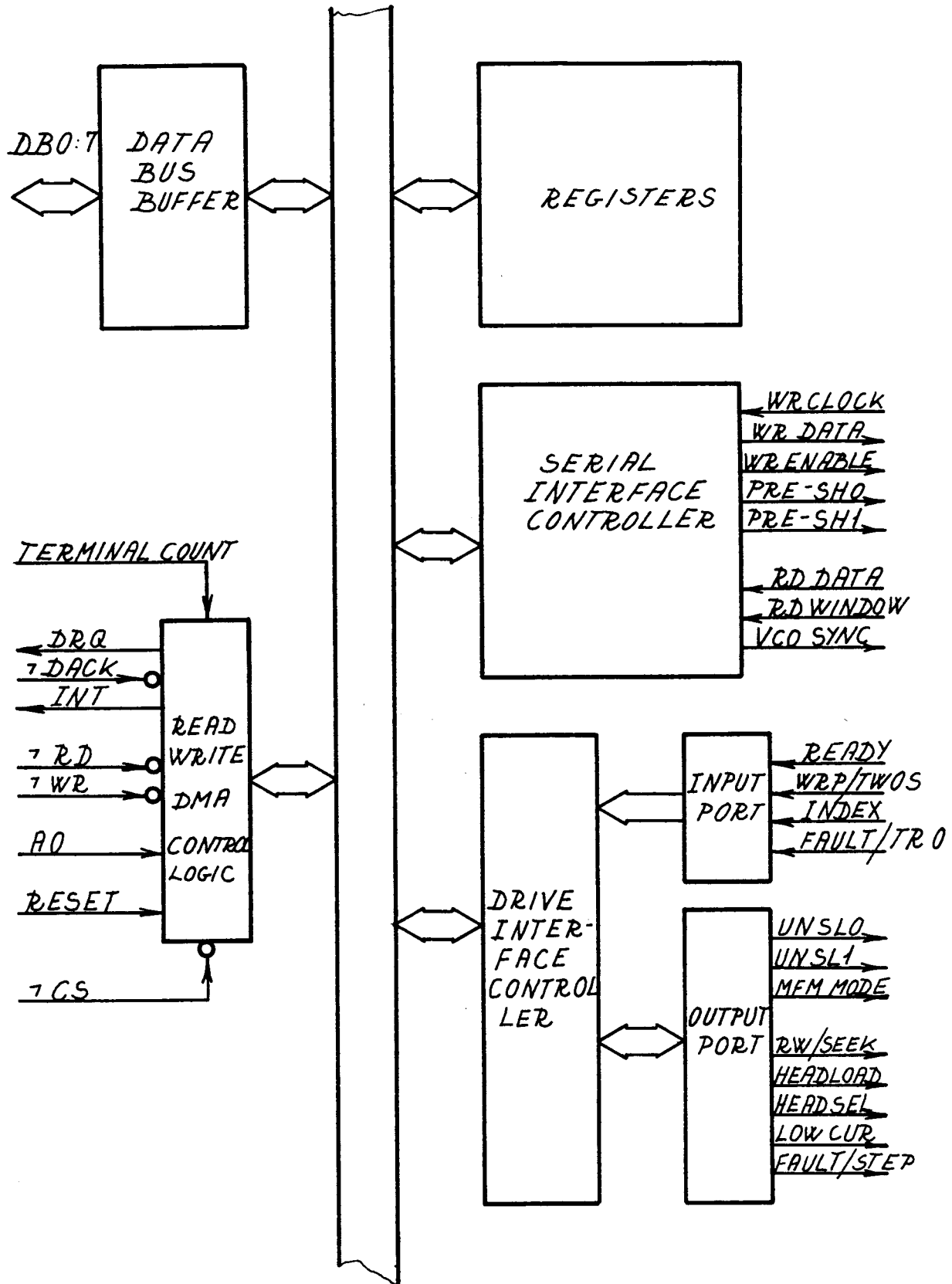
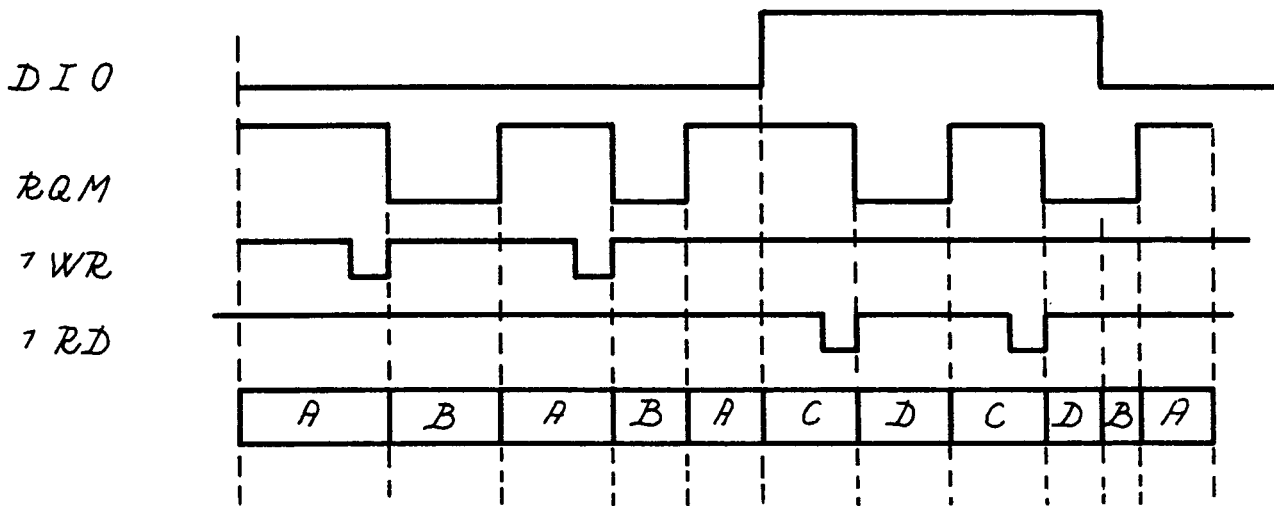
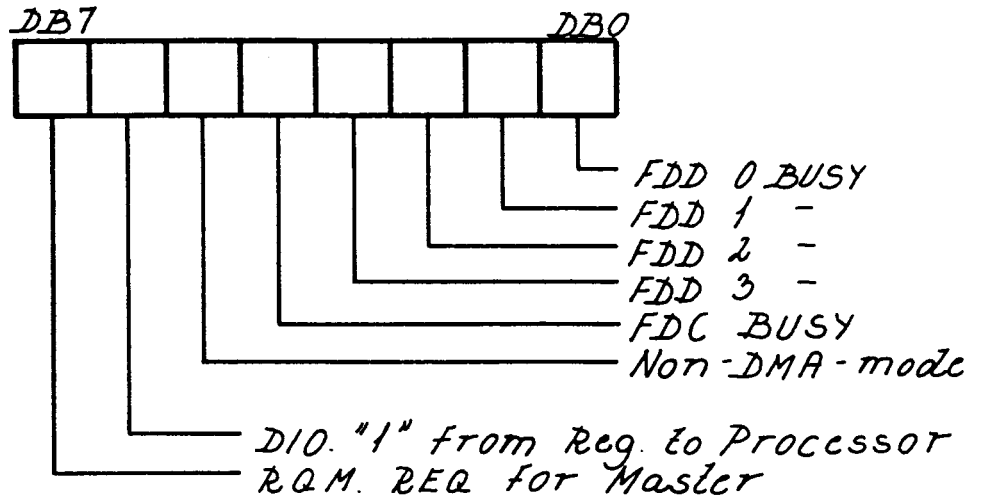


Fig. 2.3.23. BLOCK DIAGRAM FOR μ PD 765
FLOPPY DISK CONTROLLER CHIP.

STATUS REGISTER (MAIN STATUS REGISTER)

One 8-bit byte with inf. of the controller.



- A Data register ready to be written into by C
- B - - not ready - - - - -
- C - - ready for next byte to be read
- D - - not ready - - - - -

Fig. 2.3.24. STATUS REGISTER IN μ PD 765.

49

Data Register of 8-bit bytes
(Several registers in a stack)

All commands contains a command phase, an execution phase and a result phase.

PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	
	W	X	X	X	X	X	HD	US1	US0	
	W	Cylinder number (current)								
	W	Head address								
	W	Record (sector number)								
	W	Number (of data bytes/sector)								
	W	End of track								
	W	Gap Length								
	W	Data Length								
Execute Result	R	Status 0								
	R	-	1							
	R	-	2							
	R	Cylinder number (current)								
	R	Head address								
	R	Record (sector number)								
	R	Number (of data bytes/sector)								

Fig. 2.3.25. INFORMATION SUPPLIED TO AND FROM DATA REGISTER IN μ PD 765 DURING READ OR WRITE.

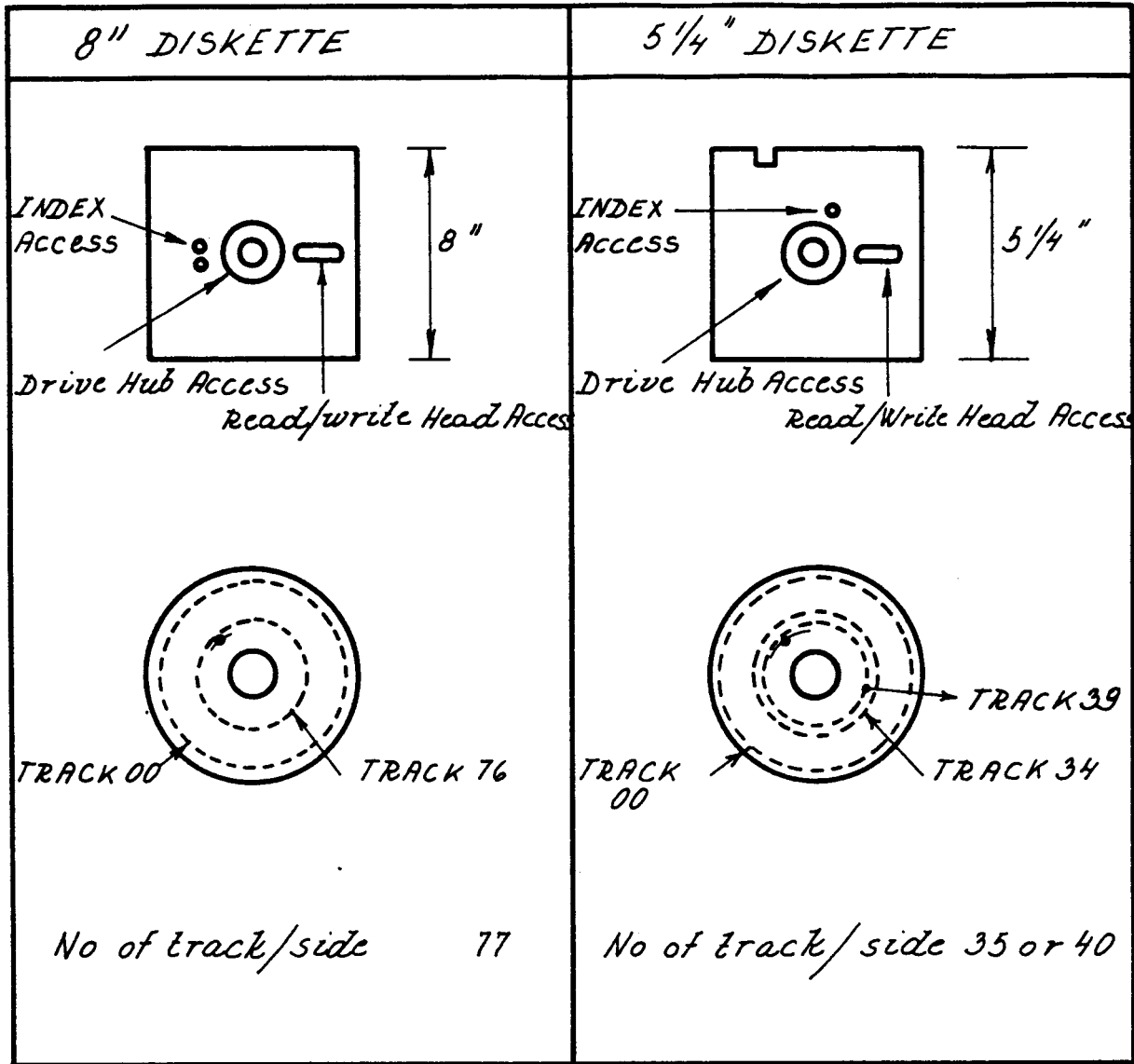
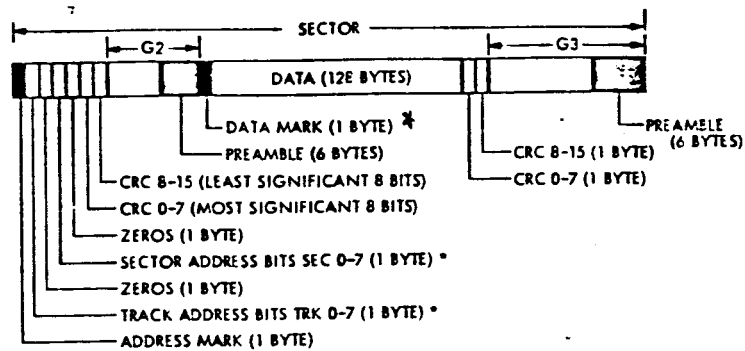
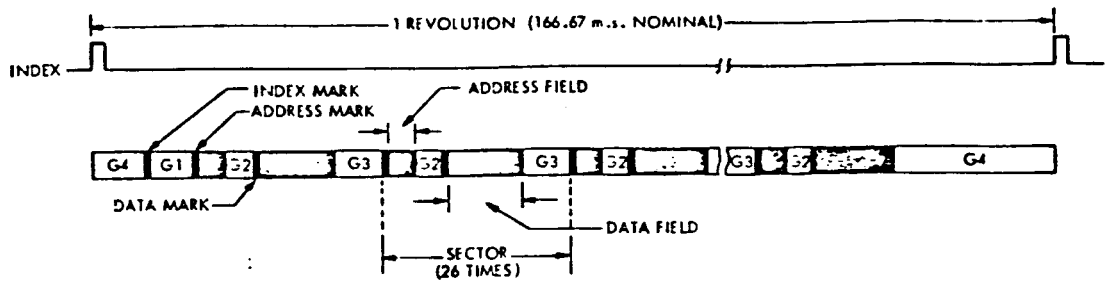


FIG. 2.3.26. FLOPPY DISK DATA MEDIA.



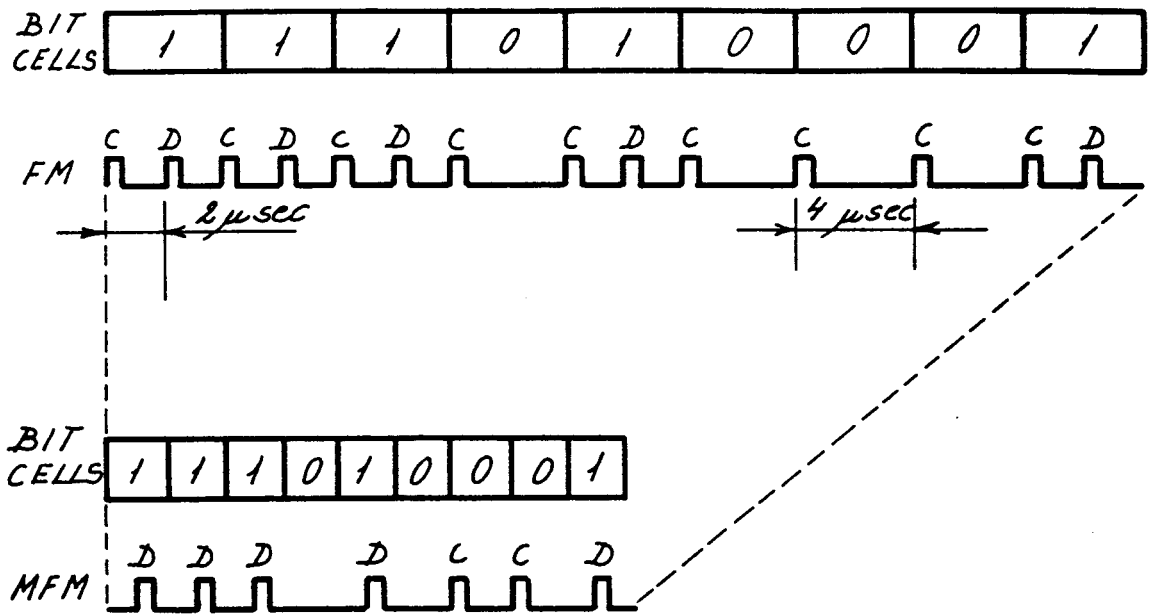
* BIT 0 IS THE MOST SIGNIFICANT BIT

GAP FIELDS

G1 = 26 BYTES HEX FF
6 BYTES HEX 00
G2 = 11 BYTES HEX FF
6 BYTES HEX 00
G3 = 27 BYTES HEX FF
6 BYTES HEX 00
G4 = 314 BYTES HEX FF
6 BYTES HEX 00

* DATA MARK is also called 'Data Address Mark'

Fig. 2.3.27 Information stored on one Track of a Diskette. The Example here shows a 8" Diskette.



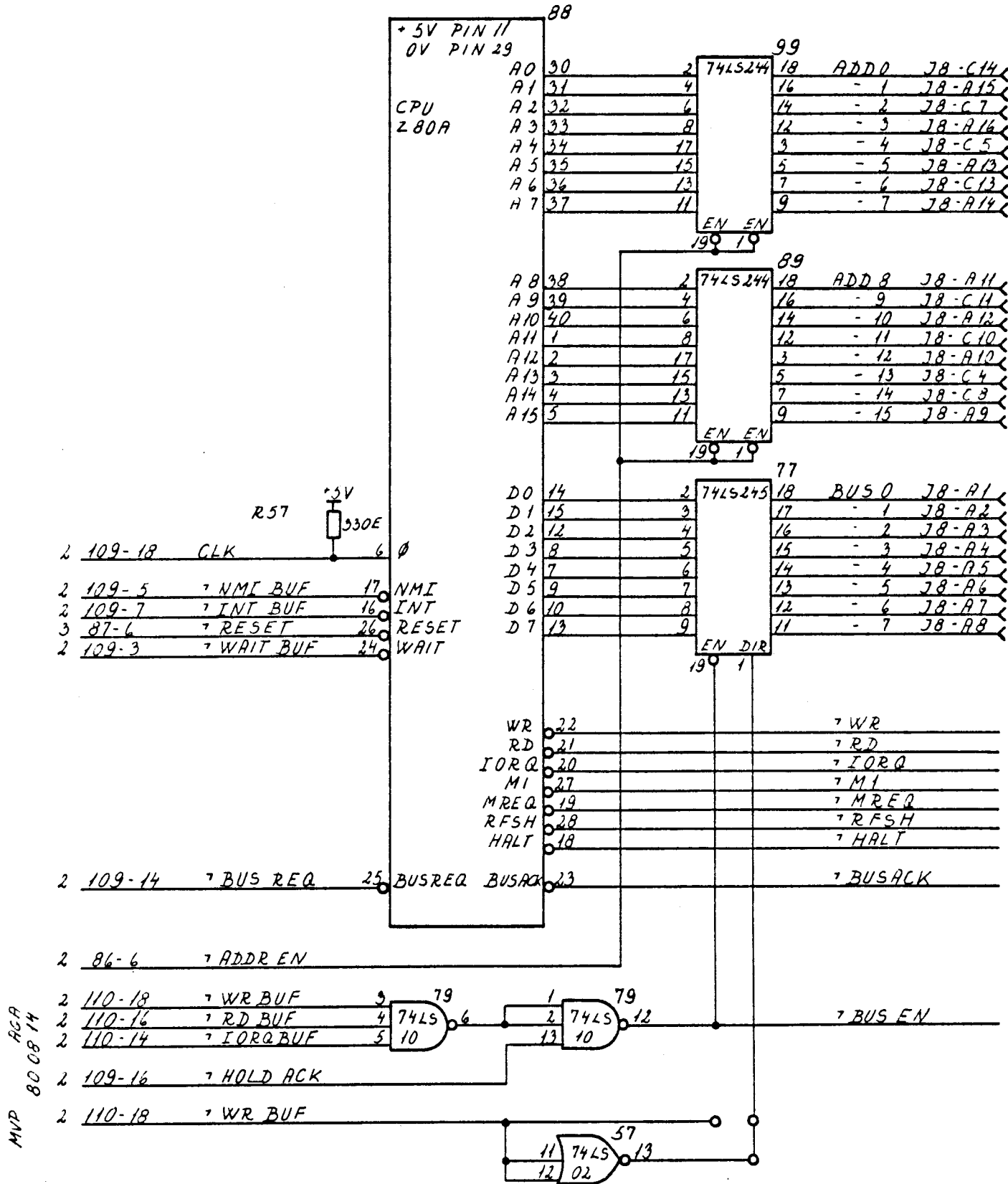
D ~ Data Pulse
 C ~ Clock

FM is also called single Density.
 MFM - - - double

	8" DISK		5 1/4" DISK	
	FM	MFM	FM	MFM
Bit Cell	4 μs	2 μs	8 μs	4 μsec
Flux Changes/Cell	2	1	2	1
- - /Inch	6536	6536	2728	5456
Kilo Bits/sec	250	500	125	250
Frequency Ratios	2/1	2/1	2/1	2/1
Bit to Bit spacing	2 μs 4 μs	2 μs 3 μs 4 μs	4 μs 8 μs	4 μs 6 μs 8 μs

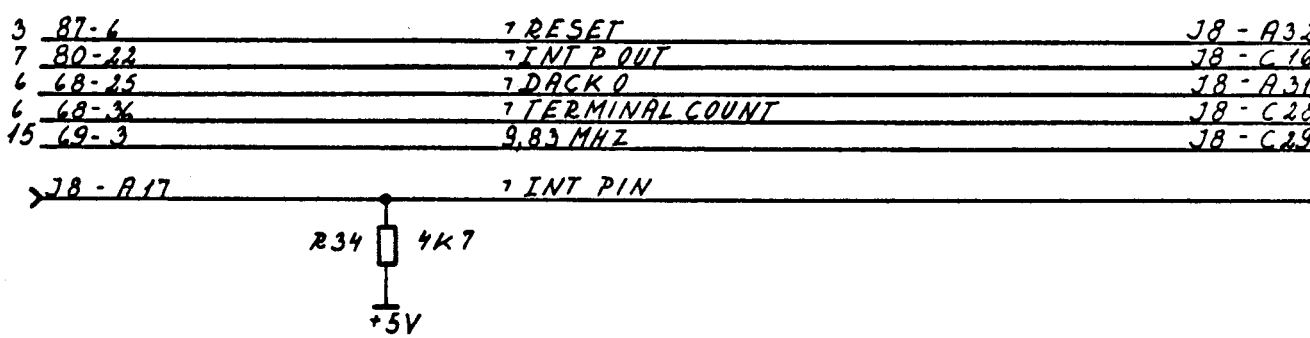
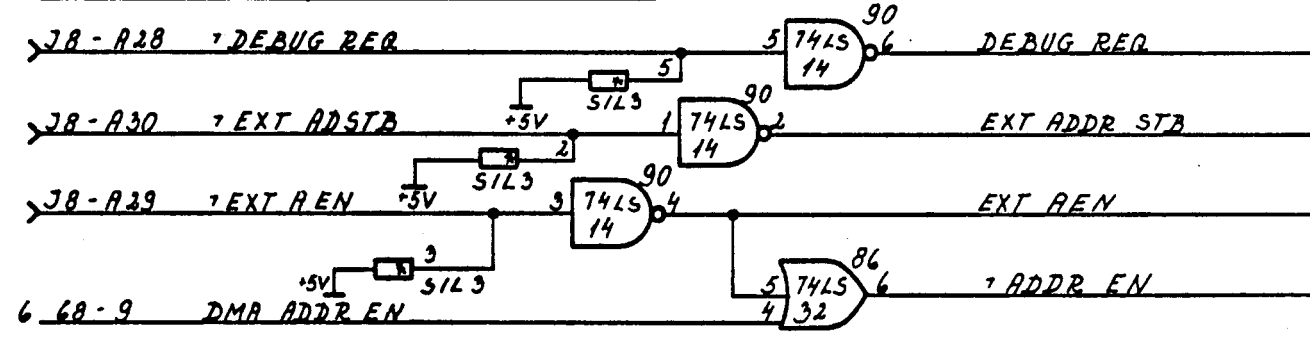
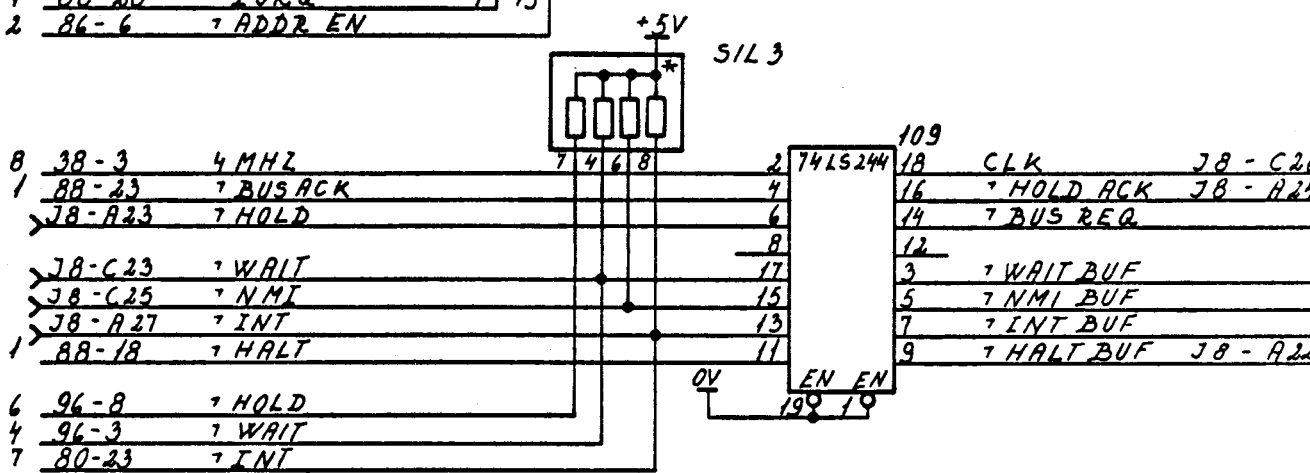
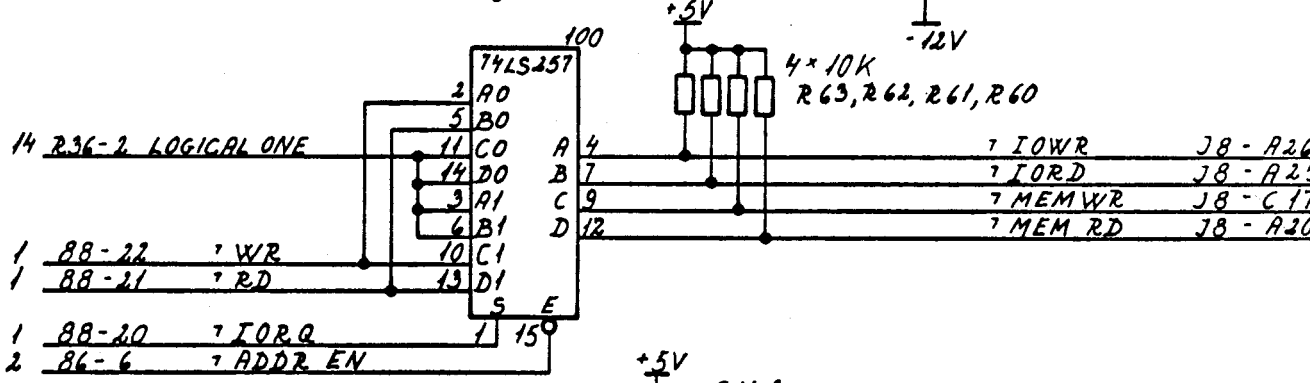
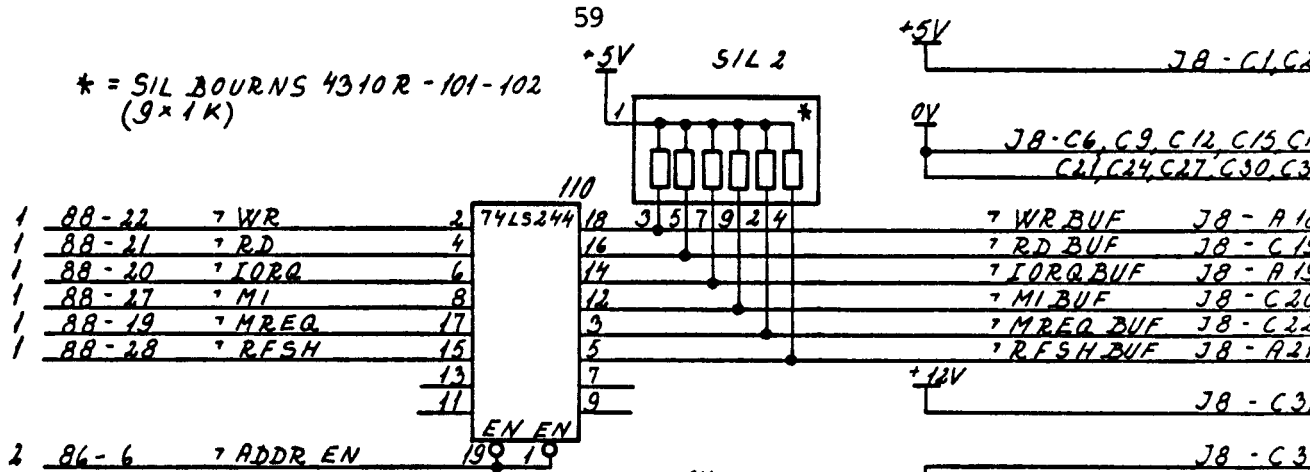
Fig. 2.3.28. RECORDING METHODS OF FLOPPY DISKS.

Signal	Destination MIC No.	Description
ADD(0:15)	3, 4, 5, 6, 7, 9, 11, 15, 16	The address bus is the TRI-state bus supplying address information to all the controllers.
BUS(0:7)	3, 5, 6, 7, 9	The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WR	2	WRITE output from the CPU.
RD	2	READ - - - -
IORQ	2	INPUT OUTPUT REQUEST, when active the WR or RD pulse is addressing a controller and not the memory.
M1	2	MACHINE CYCLE ONE, indicates the op code fetch cycle of the CPU.
MREQ	2	MEMORY REQUEST, indicates a read or write memory cycle.
REFSH	2	REFRESH, indicates a refresh cycle by the CPU, the signal is not used in MIC702.
HALT		HALT indicates that the CPU is executing a halt instruction. An error situation.
BUS ACK	2	BUS ACKNOWLEDGE, the CPU has received a BUS REQ and lets the DMA use the BUS.
BUS EN	1	BUS ENABLE for the CPU.



Signal	Destination MIC No.	Description
WR BUF	1	* WRITE output pulse from the CPU
RD BUF	1, 7, 15, 16	* READ - - - - -
IORQ BUF	1, 7, 15, 16	* IORQ - - - - -
M1 BUF	7, 15, 16	* M1 - - - - -
M REQ BUF	4	* M REQ - - - - -
RFSH BUF		* RFSH - - - - -
IOWR	3, 6, 7, 9	** INPUT/OUTPUT WRITE, write pulse to controllers which are not of the Zilog type.
IORD	6, 9, 11, 15	** INPUT/OUTPUT READ, read pulse to controllers which are not of the Zilog type.
MEM WR	4, 5	** MEMORY WRITE pulse.
MEM RD	3, 4, 5	** MEMORY READ pulse.
CLK	1, 4, 6, 7, 15, 16	4 MHz symmetric clock to the system.
HOLD ACK	1, 6	BUS ACK signal through a buffer.
BUS REQ	1	The DMA controller or the tester demand control over the BUS.
WAIT BUF	1	This signal inserts at least one wait state in each CPU cycle.
NMI BUF	1	NON MASKABLE INTERRUPT, only used by a tester.
INT BUF	1	INTERRUPT REQUEST to CPU.
HALT BUF		HALT signal through a buffer.
DEBUG REQ	6	DMA REQUEST from a tester.
EXT ADDR STB	6	DMA REQUEST signal from a tester.
EXT AEN		- - - - -
ADDR EN	1, 2, 3, 4, 6	ADDRESS ENABLE when active the CPU controls the BUS system.
INT PIN	15	INT PIN may be used by a unit connected to J8 and is interrupt priority in.
		* signal is only active, when ADDR EN is active.
		** Signal may also be active when ADDR EN is active. The DMA also uses these signals, which are of the TRI-state type.

* = SIL BOURNS 4310R-101-102
(9x1K)



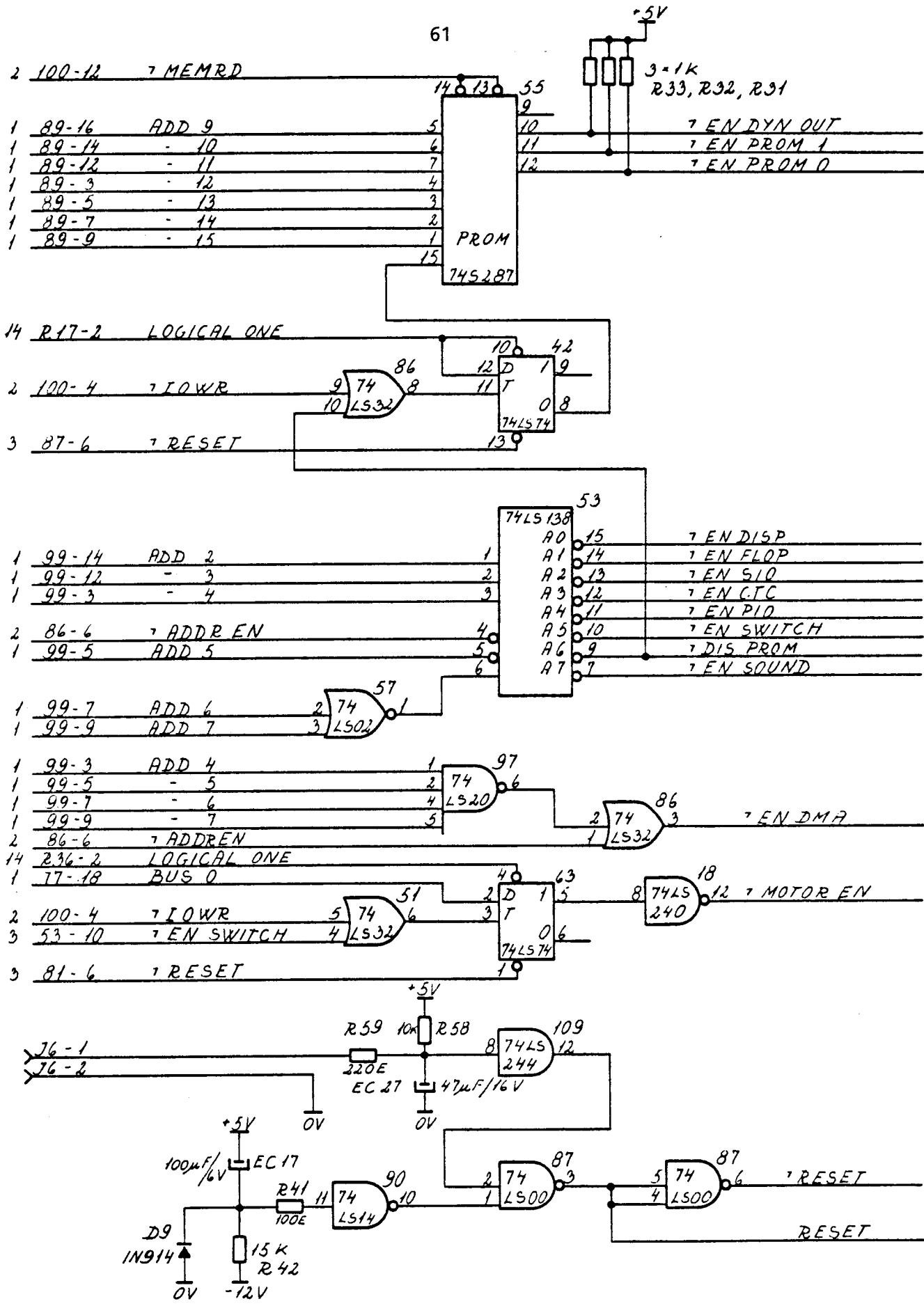
MVP
80.08.14
AGA

MIC 702
R13078

CONTROL SIGNALS RECEIVERS
AND TRANSMITTERS

MIC 0

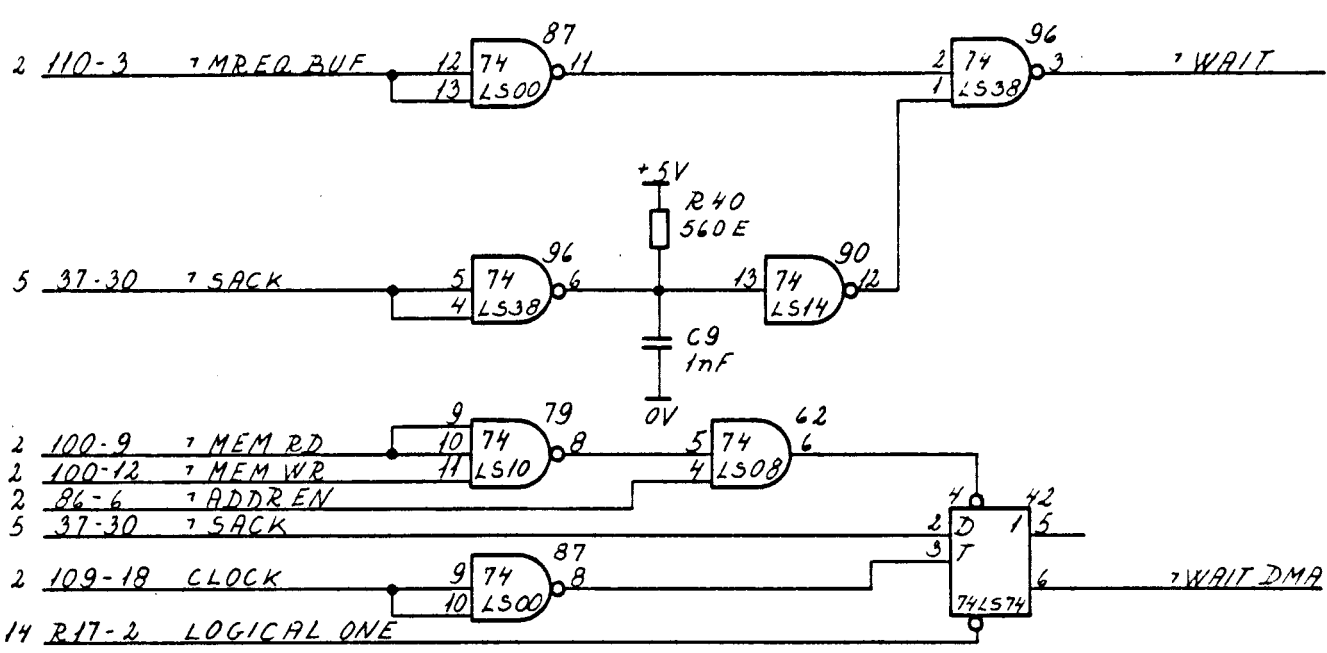
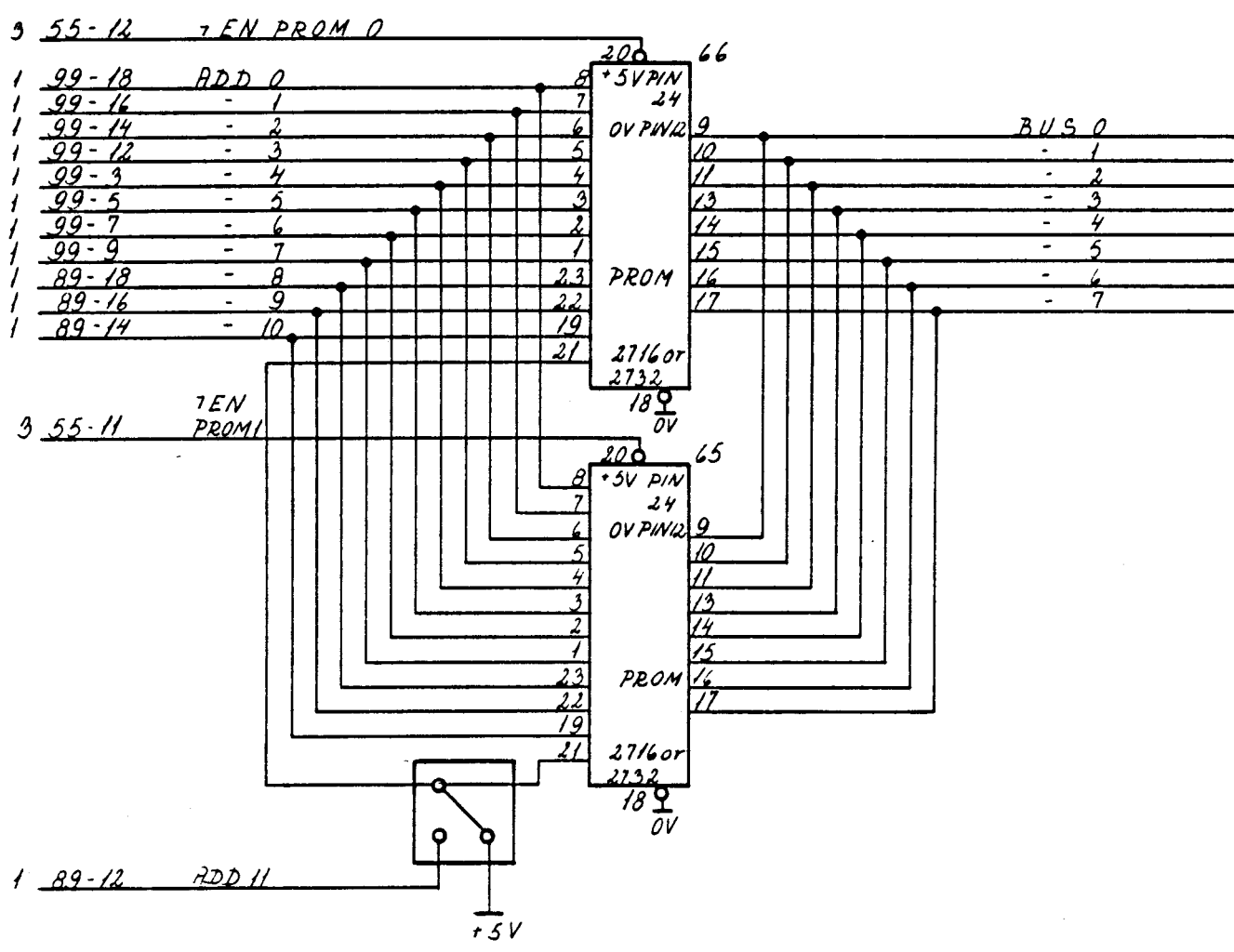
Signal	Destination MIC No.	Description
EN DYN OUT	5	* This signal enables the output register from the RAM.
EN PROM 1	4	* This signal enables the output from PROM 1 which is only used when running a testprogram.
EN PROM 0	4	* This signal enables the output from PROM 0 which contains the program used under initiation.
EN DISP	11	* ENABLE DISPLAY controller
EN FLOP	9	* ENABLE FLOPPY controller
EN SIO	16	* ENABLE SERIAL IN/OUT controller
EN CTC	15	* ENABLE COUNTER/TIMER controller
EN PIO	7	* ENABLE PARALLEL IN/OUT controller
EN SWITCH	3, 15	* ENABLE SWITCHES
DIS PROM		* DISABLE PROM, the signal is used to disable the PROM and enable the whole RAM
EN SOUND	7	* ENABLE SOUND gives the acoustic signal
EN DMA	6	* ENABLE DMA controller
MOTOR EN	10	MOTOR ENABLE is used to switch on and off the motor used in the Mini floppy disk drive.
RESET	1, 3, 6, 9, 11 15, 16	RESET is the power up reset or a RESET initiated from the switch on the front of the computer. * Subsection 2.3.3. describes the actual addresses used in MIC702.



MVP AGA
80 08.14

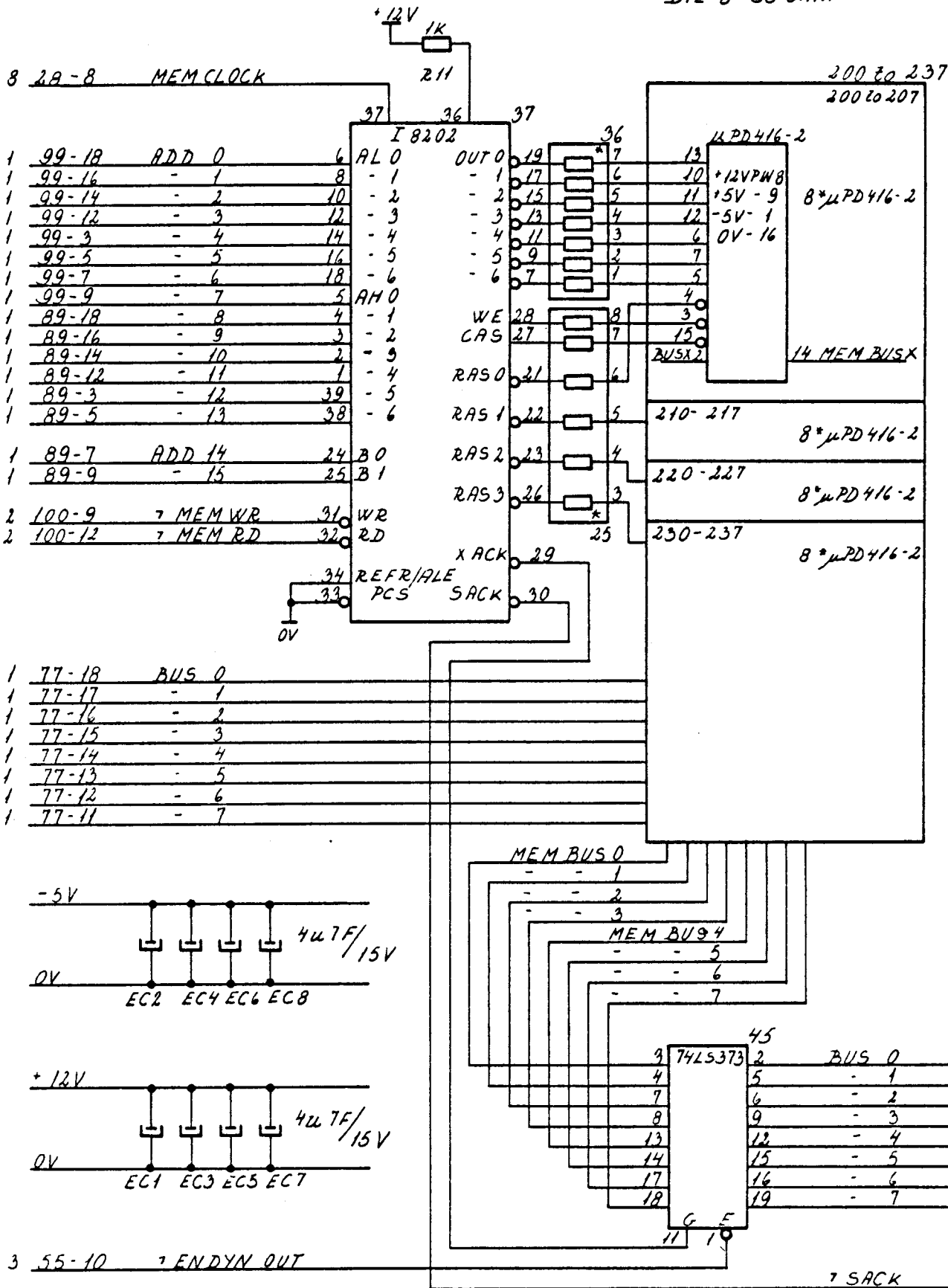
Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
WAIT	2	WAIT supplies at least one wait state to the CPU-fetch cycle. More wait states are inseted when the RAM controller is making a refresh cycle.
WAIT DMA	6	WAIT DMA supplies at least one wait state in the DMA-cycle. More wait states are supplied when the memory controller is making a refresh cycle.

702 ROA 375
 702 ROB 358
 703 ROB 357.



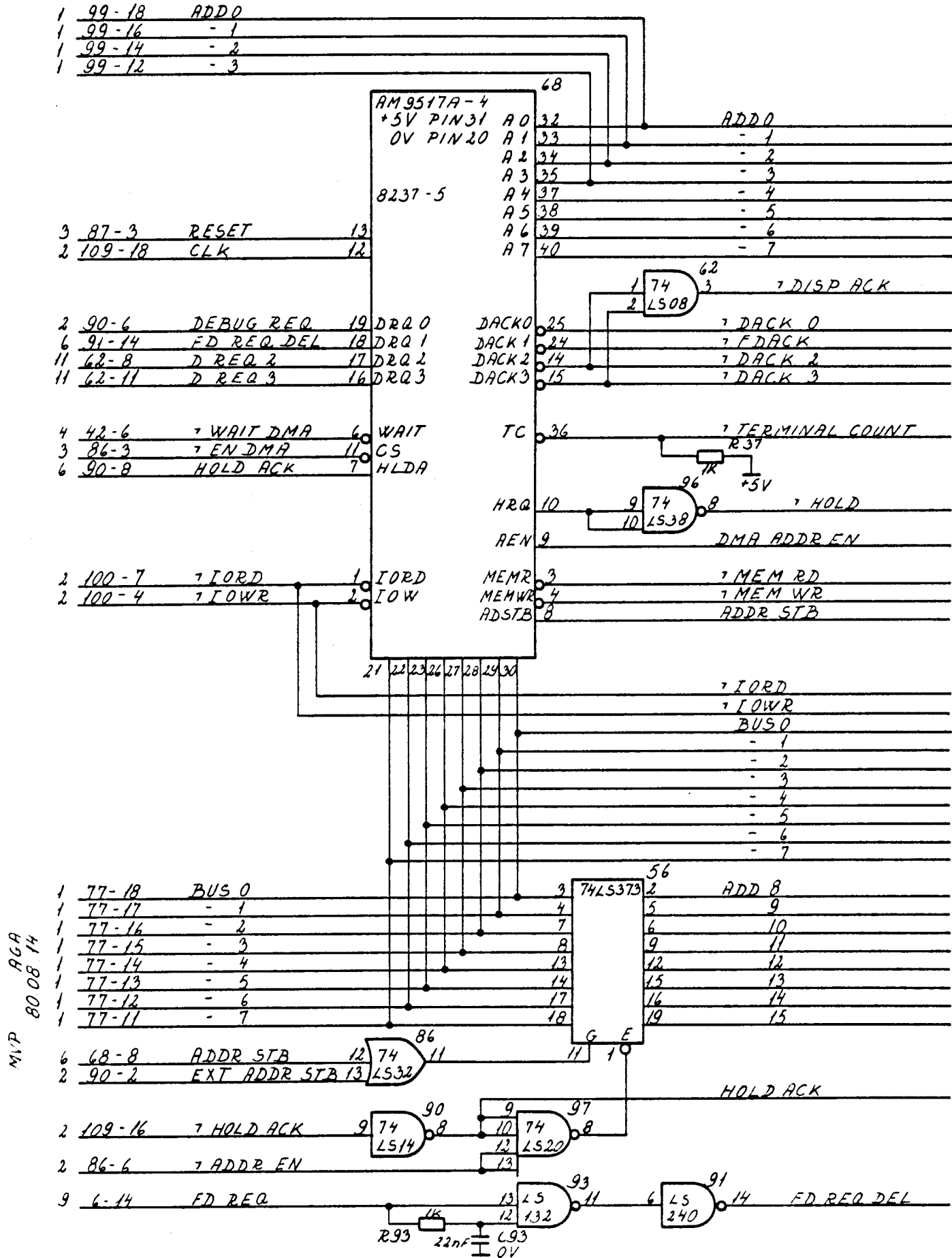
MVP RGA
 80 08 14

Signal	Destination MIC No.	Description
BUS(0:7)		The data bus is the TRI-state bus supplying data information between the CPU and the controllers.
SACK	4	Output signal from the RAM controller showing that the cycle is finished. (SACK means System Acknowledge).



MVP 80.08.14
RGA

Signal	Destination MIC No	Description
ADD(0:7)		Address lines containing the 8 most significant bits. Bit (0:4) is both input to the DMA controller (under programming) and output from the DMA controller (under DMA-cycle).
DACK 0	2	Data acknowledge answer to debug request.
FDACK	9	Floppy data acknowledge, answer to FD req. delay.
DACK 2	11	Data acknowledge answer to DREQ2.
DACK 3		Data acknowledge answer to DREQ3.
DISP ACK	11	Display acknowledge. The display controller uses two channels in the DMA.
TERMINAL COUNT	2, 9, 11	The signal is used to terminate the operation.
HOLD	2	Request to stop the CPU.
DMA ADDR EN	2	Request to gain control over the data and address bus.
MEM RD		Memory read output from the DMA.
MEM WR		Memory write output from the DMA.
ADDR STROBE	6	Address strobe is a pulse to load the address register.
BUS(0:7)		Data bus used to supply information between the CPU and the controllers. Here also used to send address information from the DMA controller to the address register.
HOLD ACK		Hold acknowledge is the replay from the CPU that the bus is idle.
FD REQ DEL		DMA request signal from floppy disk controller.



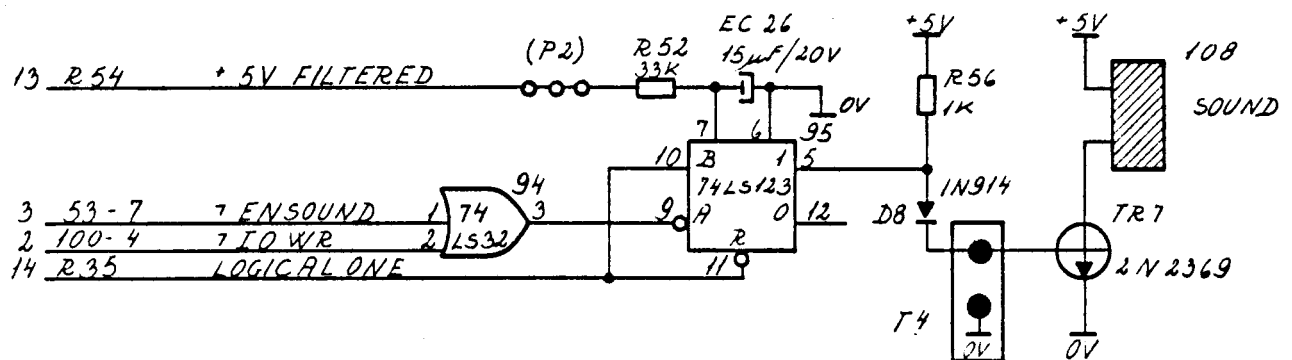
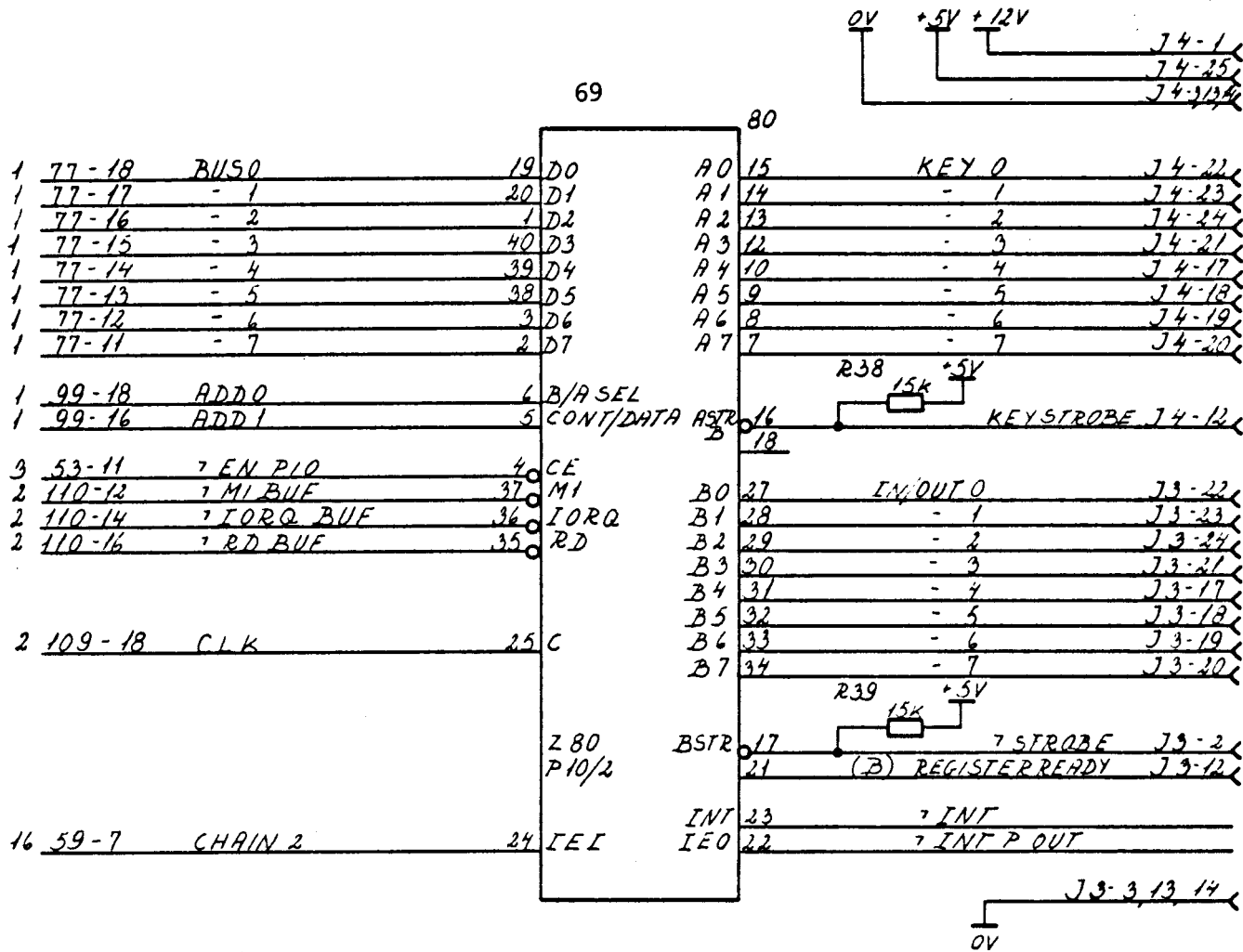
MIC 702

DMA-CONTROLLER

MIC 00

R13082

Signal	Destination MIC No.	Description
KEY(0:7)		8-bit parallel input used to receive information from the keyboard.
KEY STROBE		Input strobe from the keyboard.
IN/OUT(0:7)		8-bit parallel input/output used to receive or transmit information to and from an external unit.
STROBE		Input strobe from external unit.
REGISTER READY		Output showing that output from the 8-bit input/output port is ready.
INT	2	Interrupt request.
INT P OUT	2	Interrupt priority out.



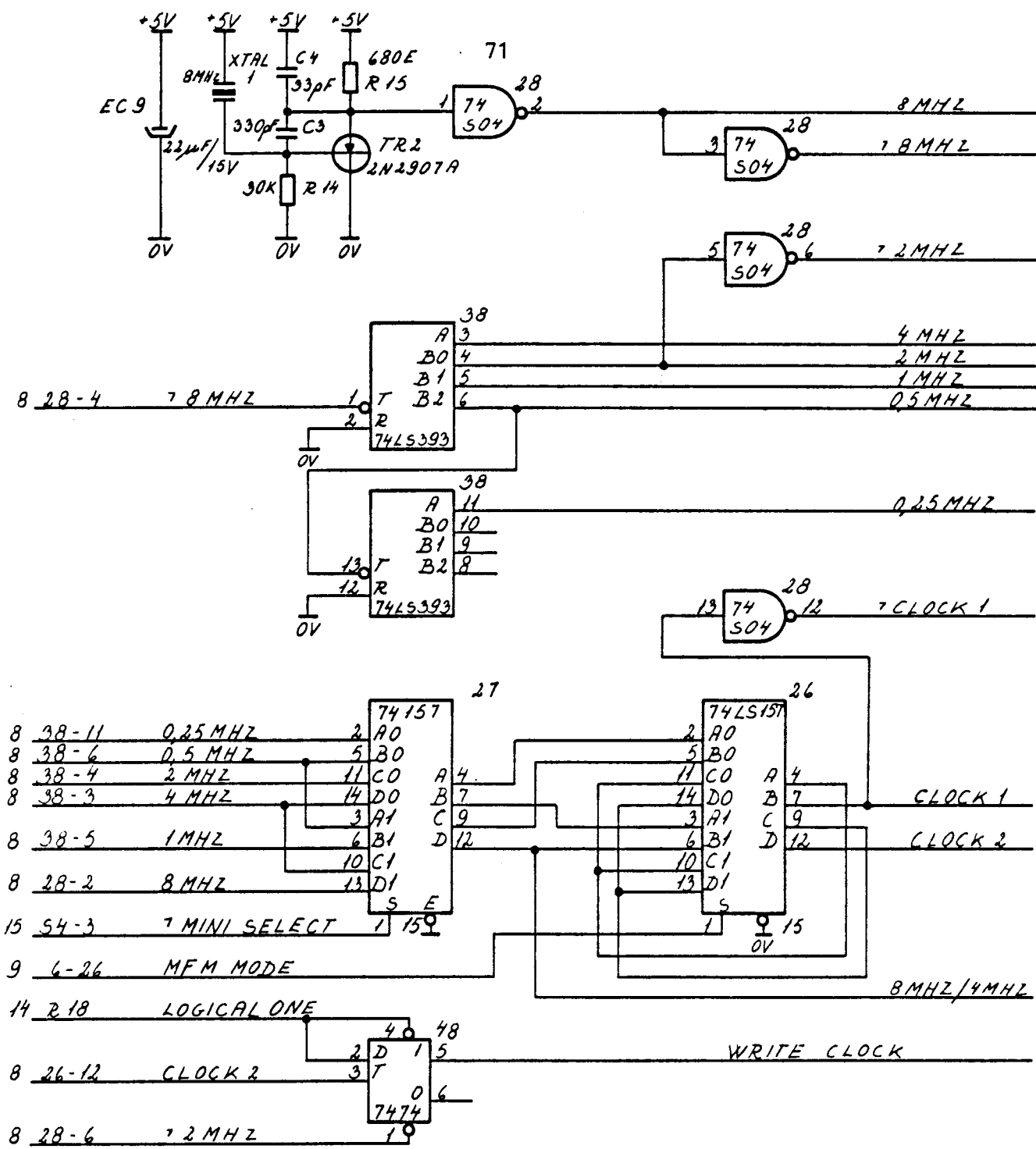
MVP 80 08 14
HGA

MIC 702
R 12083

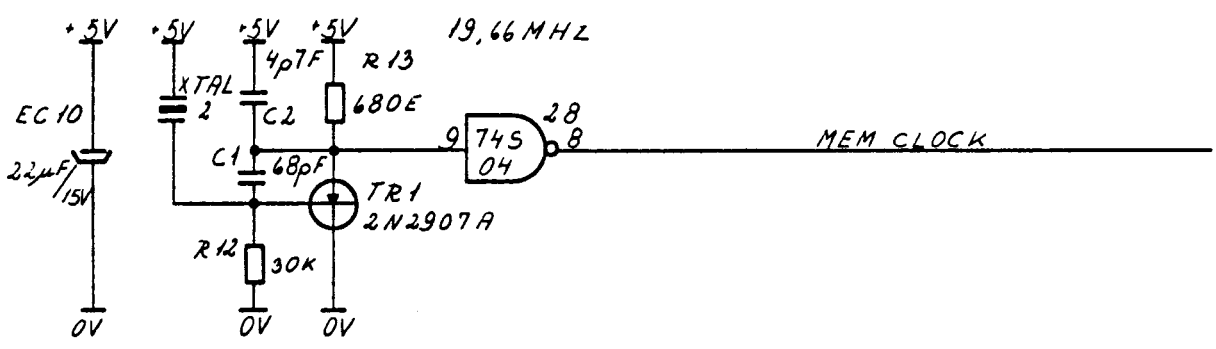
KEYBOARD & PARALLEL IN/OUT

MIC 01

Signal	Destination MIC No.	Description
8 MHz	8, 9	Symmetric clock signal of 8 MHz
4 MHz	2, 8	- - - - 4 MHz
2 MHz	8	- - - - 2 MHz
1 MHz	8	- - - - 1 MHz
0.5 MHz	8	- - - - 0.5 MHz
0.25 MHz	8	- - - - 0.25 MHz
CLOCK 1	10	Clock to read logic for the floppy controller. Frequency is selected by the controller and by the MINI SELECT switch.
CLOCK 2	8	
8 MHz/4 MHz	9	Clock to the floppy controller 8 MHz for Maxi floppy and 4 MHz for Mini floppy drive.
WRITE CLOCK	9	Clock input to floppy controller. The frequency is selected by the controller and by the MINI SELECT switch.
MEM CLOCK	5, 15	Clock to the memory controller. The frequency is 19.66 MHz.



MVP RGA 80 08.14



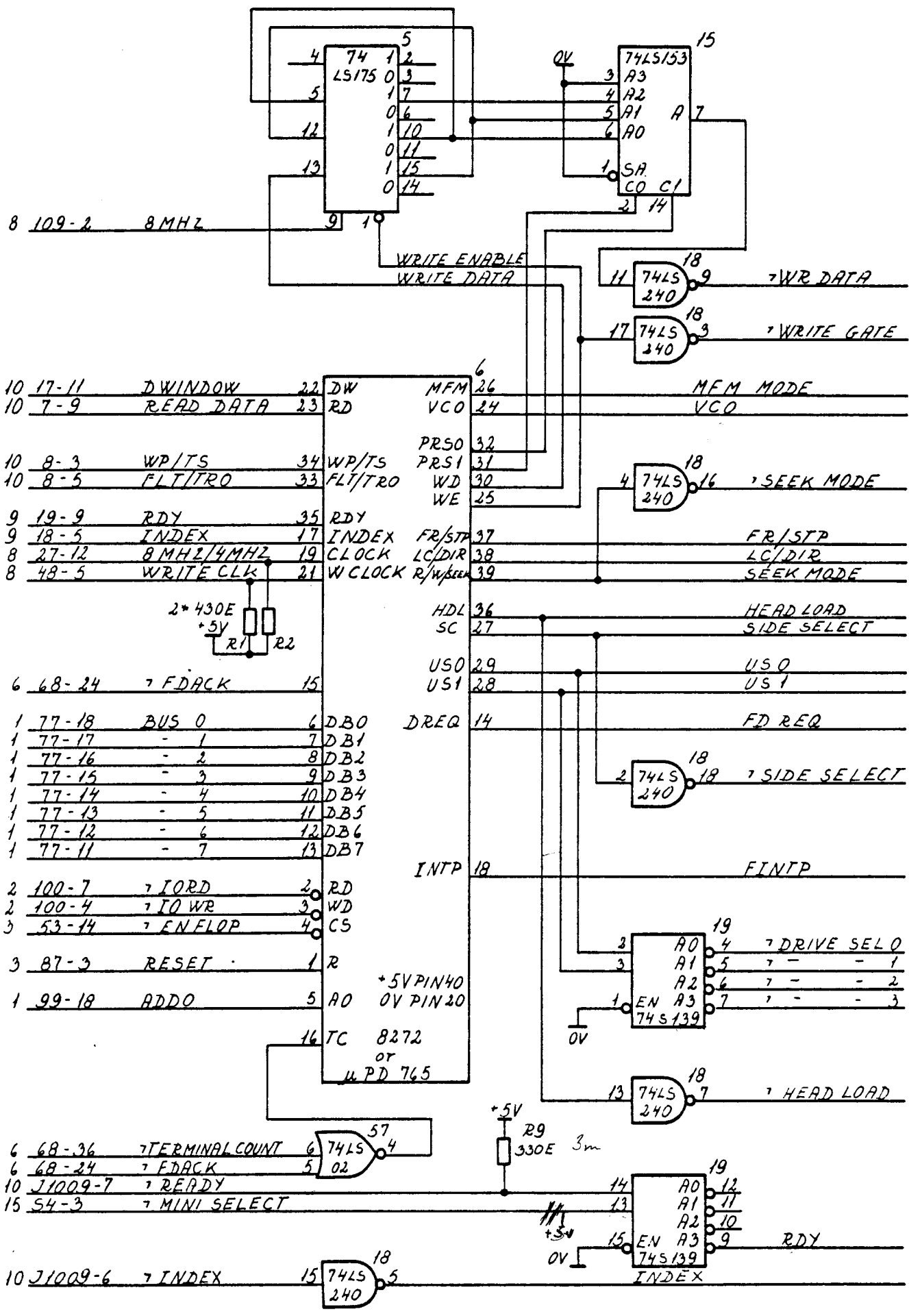
MIC 702
R 13084

CLOCK SYSTEM

MIC 08

Signal	Destination MIC No.	Description
WR DATA	10	WRITE DATA to the floppy disk drive. Valid when WRITE GATE is on.
WRITE GATE	10	Control signal to floppy disk drive. Informs that now the WR DATA is valid.
MFEM MODE	8	MFEM mode is dual density, FM mode is single density.
VCO	10	Signal to control the voltage controlled oscillator.
SEEK MODE	10	Sets the selectors in seek mode.
FR/STP	10	Control signal; Fault Reset/Step
LC/DIR	10	Control signal; Low Current/Direction
HEAD LOAD	10	Control signal; Head Load
SIDE SELECT	10	Control signal; Side Select
US0, US1		Unit select decoded to:
DRIVE SEL 0	10	Drive Select 0
DRIVE SEL 1	10	Drive Select 1
DRIVE SEL 2	10	Drive Select 2
DRIVE SEL 3	10	Drive Select 3.
FD REQ	6	DMA request from floppy controller.
F INTP	15	Floppy controller interrupt request.
RDY	9	Ready from floppy controller. Note that Mini floppy is always ready.
INDEX	9	Index mark from floppy disk drive.

MVP
80.08.14
RGA

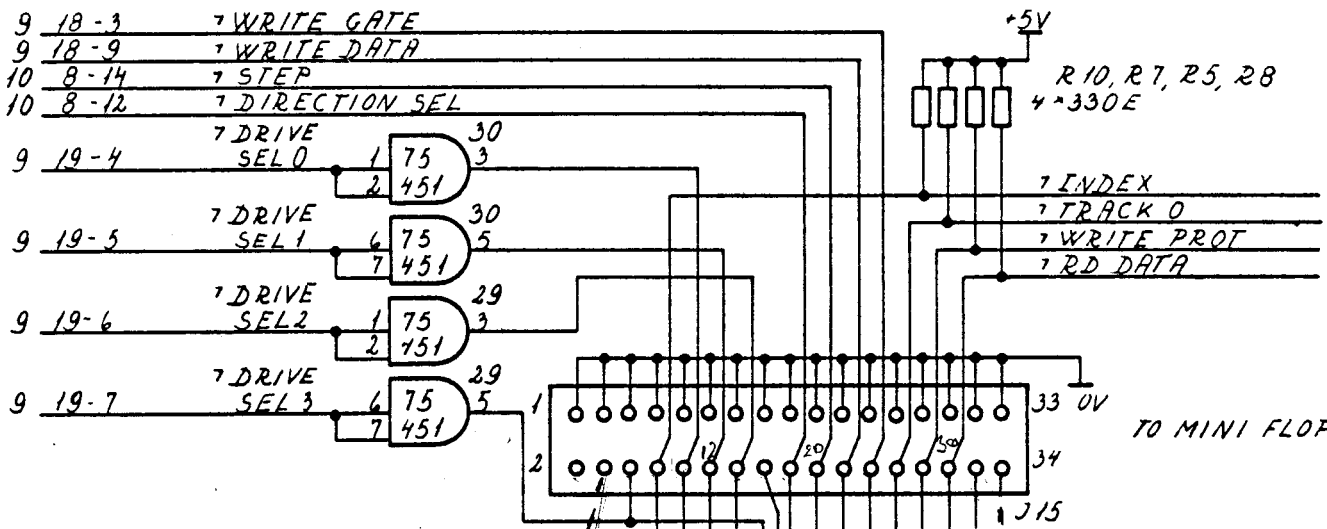
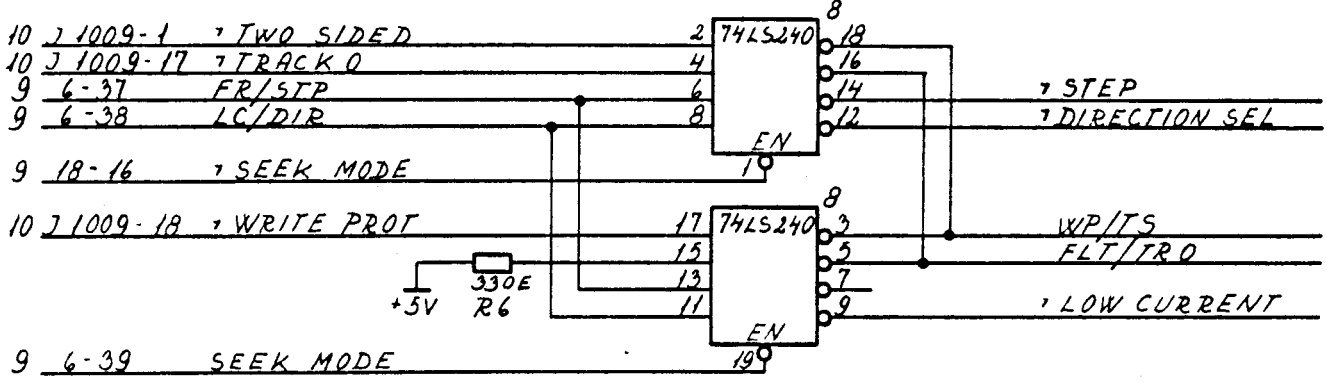
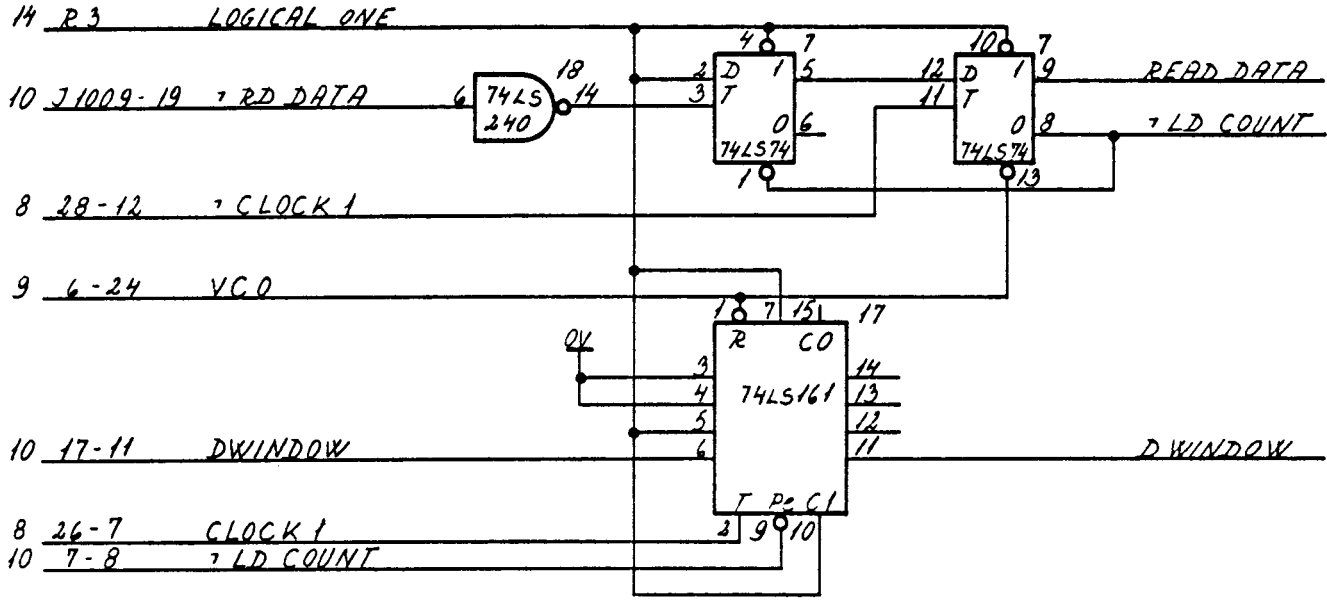


MIC 702
R 13085

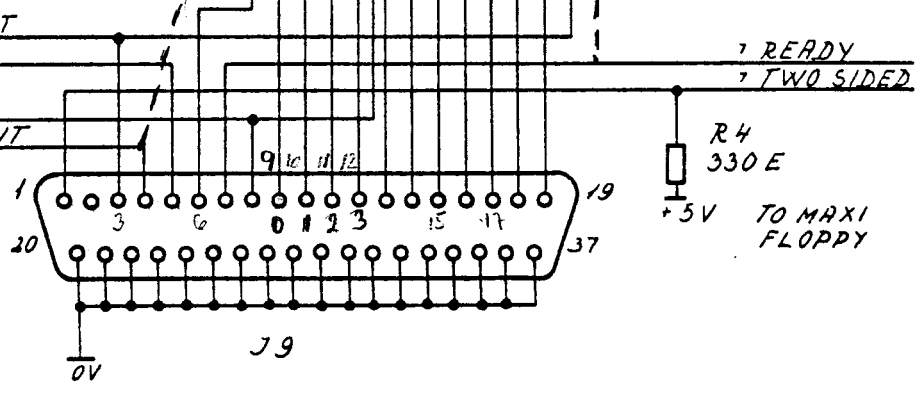
FLOPPY DISK CONTROLLER

MIC 09

Signal	Destination MIC No.	Description
READ DATA	9	Read data from the floppy, synchronized with the VCO to separate phase bits and data bits.
LD COUNT	10	Load counter is used to synchronize the window counter.
D WINDOW	9, 10	Data Window is used by the controller to separate data bits from phase bits.
STEP	10	Output pulse to make the floppy head move from one cylinder to the next.
DIRECTION SEL	10	Direction select is used together with the STEP pulse. A low signal and the head moves towards the counter of the disc.
WP/TS	9	Write Protect/Two Sided signal from the floppy disk drive.
FLT/TRO	9	Fault/Track 0 signal from floppy disk drive.
LOW CURRENT	10	Output signal to Maxi floppy disc drive. Used to decrease the write current when close to the center of the disk.
INDEX	9	Index mark signal from the floppy.
TRACK 0	10	Track 0 signal from the floppy.
WRITE PROT	10	The diskette used is writeprotected.
RD DATA	10	Read data supplied from the floppy disk drive including data and phase bits.
READY	9	Ready signal from the Maxi floppy drive.
TWO SIDED	10	The Maxi floppy is a two sided version.



MVP RGA
80 08 14

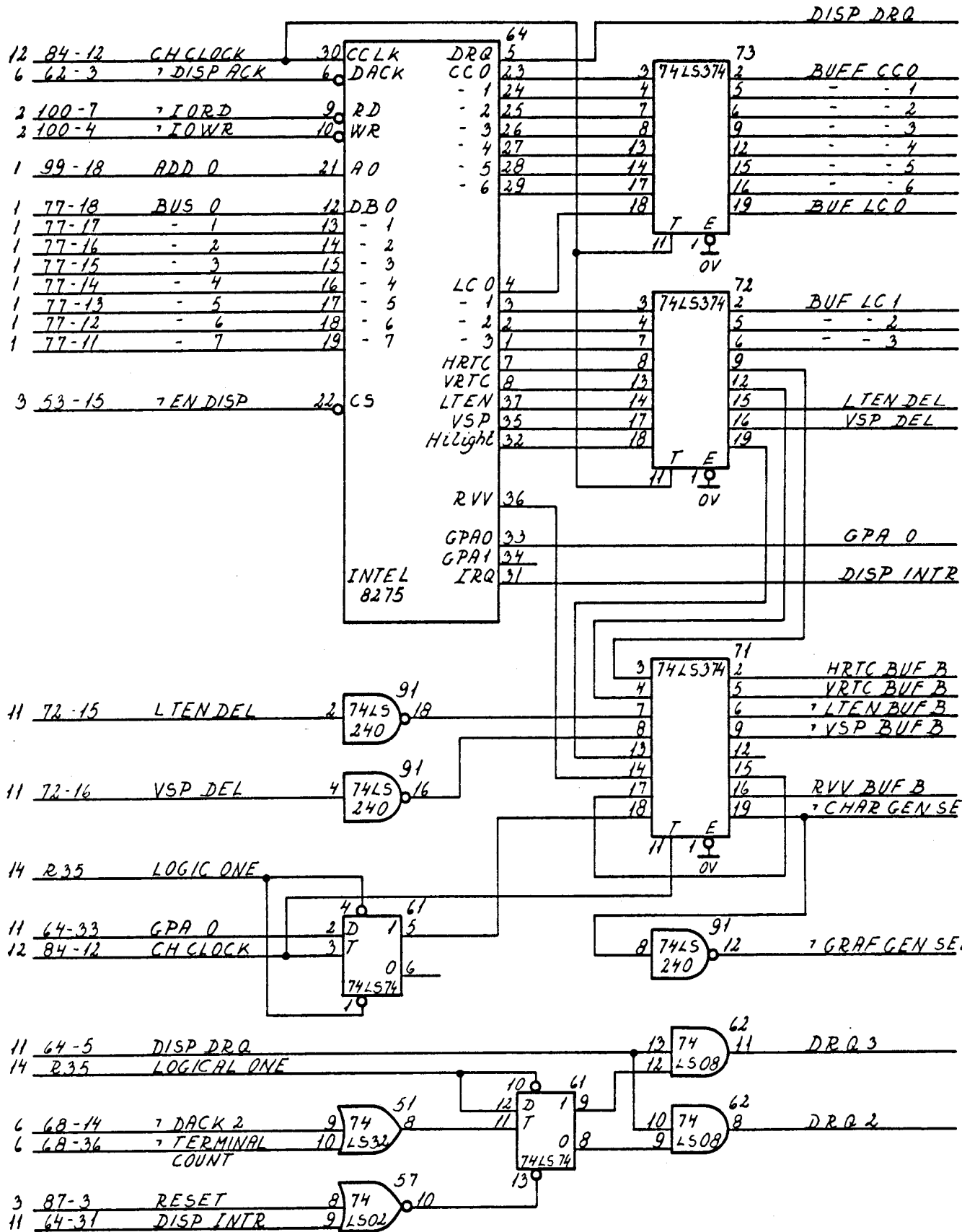


MIC 702
R13086

FLOPPY DISK READ & SELECT CIRCUIT

MIC 10

Signal	Destination MIC No.	Description
DSP DRQ	11	DMA request from the display controller.
BUFF CC(0:6)	12	Output from the display controller containing the address of the character to be written on the display.
BUFF LC(0:3)	12	Output from the display controller containing the line number written on the display.
LITEN DEL	11	Light enable from the display.
VSP DEL	11	Video suppression. This output signal is used to blank the video to the display.
GPA 0	11	Control signal used to select semigraphic PROM.
DISP INTR	11, 15	Display interrupt request.
HRTC BUF B	13	Horizontal retrace signal.
VRTC BUF B	13	Vertical retrace signal.
LITEN BUF B	13, 14	LITEN DEL delayed one CHAR CLOCK
VSP BUF B	13	VSP DEL delayed one CHAR CLOCK
RVV BUF B	13	REVERSE VIDEO. This output is used to reverse the video signal to the display.
CHAR GEN SEL	12	This signal selects the standard character generator.
GRAF GEN SEL	12	This signal selects the semigraphic character generator.
DRQ3 and DRQ2	6	The display controller uses two channels out of the DMA's four channels. This is done to make the roll function of the display. DRQ2 and DRQ3 are the two data request signals.

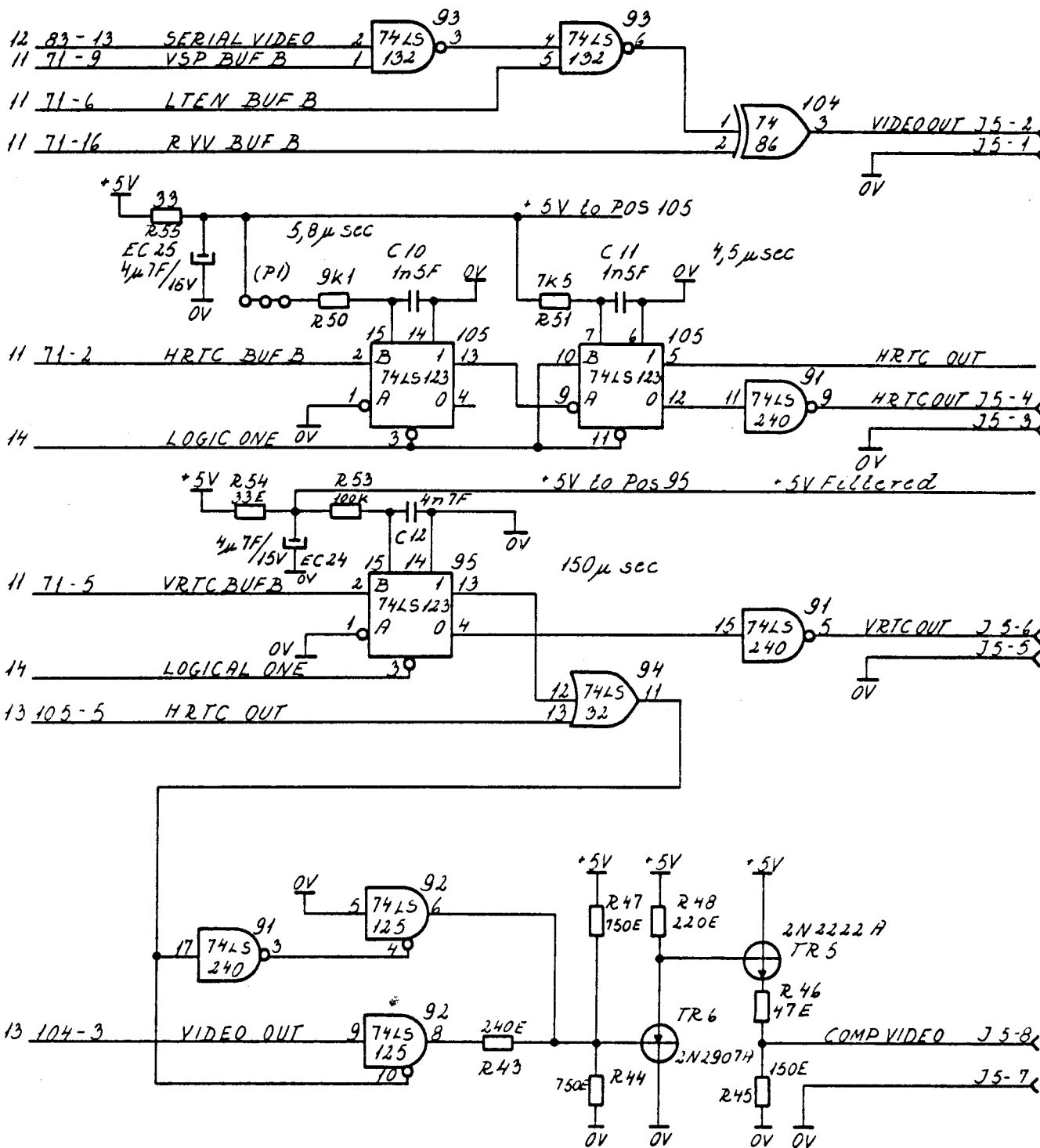


MVP 80.08.14

Signal	Destination MIC No.	Description
SERIAL VIDEO	13	The video output from the shift register.
LOAD	12	Signal to load the output from the character ROM or the semigraphic ROM into the shift register.
CH CLOCK	11	Character clock. The period time of this clock is 7 times the DOT CLOCK time.

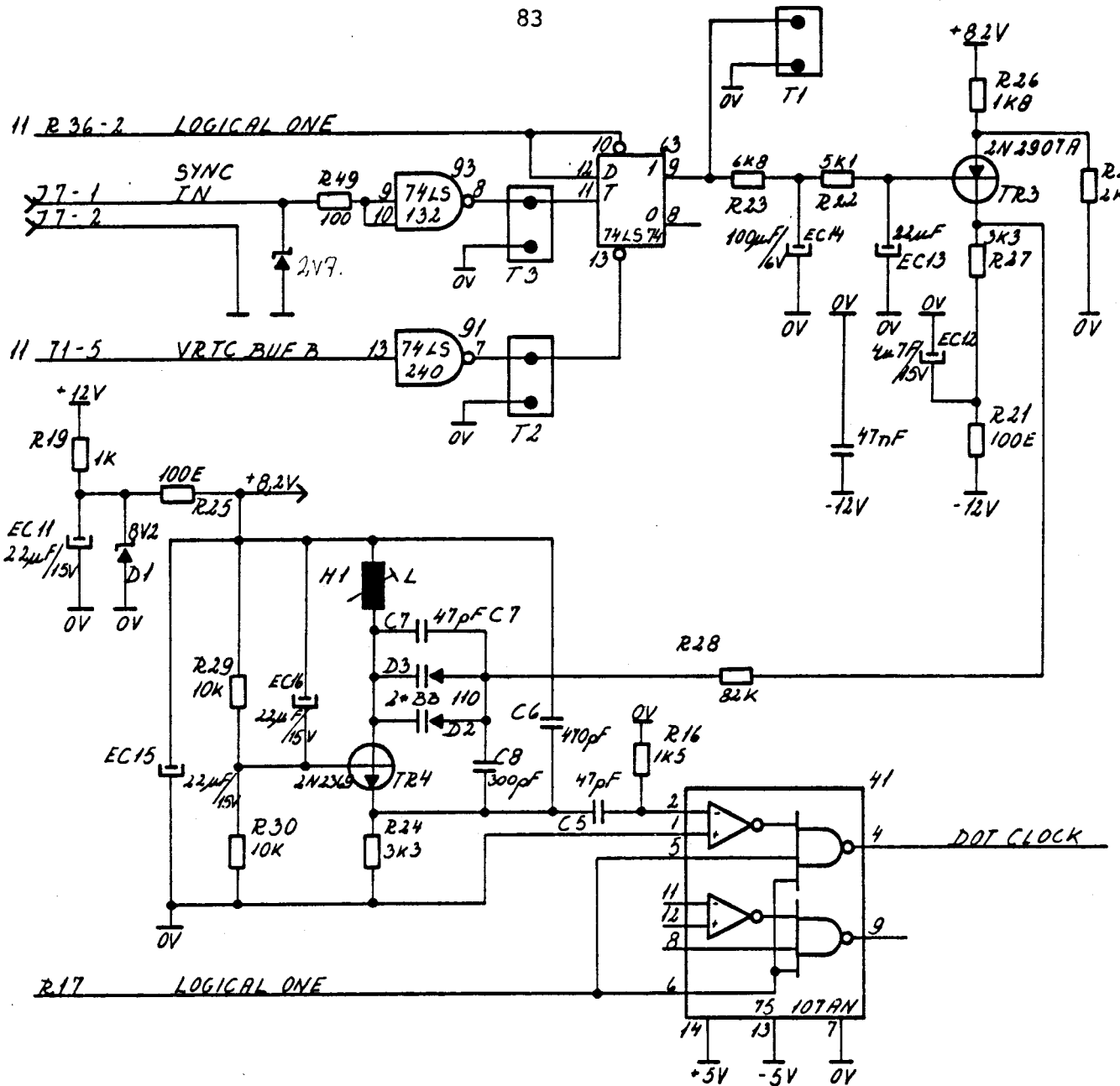
$$7 \times 86 \text{ nsec.} = 0.601 \text{ usec.}$$

Signal	Destination MIC No.	Description
VIDEO OUT	13	Video out signal. *)
HRTC OUT	13	Horizontal output pulse. *)
VRTC OUT		Vertical output pulse. *)
		*) These three signals are ready to be used if a video monitor without decoding for comp. video is used. RC702 uses comp. video signals.
COMP VIDEO		Compressed video is the signal containing both video horizontal sync. and vertical sync.
+5 V filtered	7	+5 V supply after an RC filter.

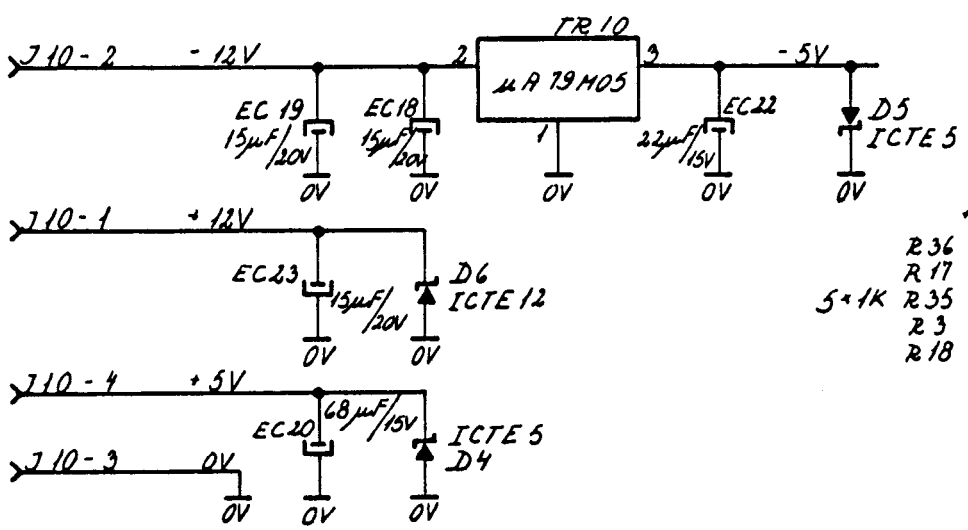


MVP 80.08.14

Signal	Destination MIC No.	Description
DOT CLOCK	12	The dot clock is an 11.64 MHz clock which is synchronized with the main frequency.
SYNC IN		The input is a 50 Hz signal from the REC701 rectifier unit.
T1		Testpoint 1. The signal here is a 50 Hz signal and the coil H1 is adjusted until the dutycycle of this signal is 50%.
-5 V		The -5 V is used to the dynamic RAM.



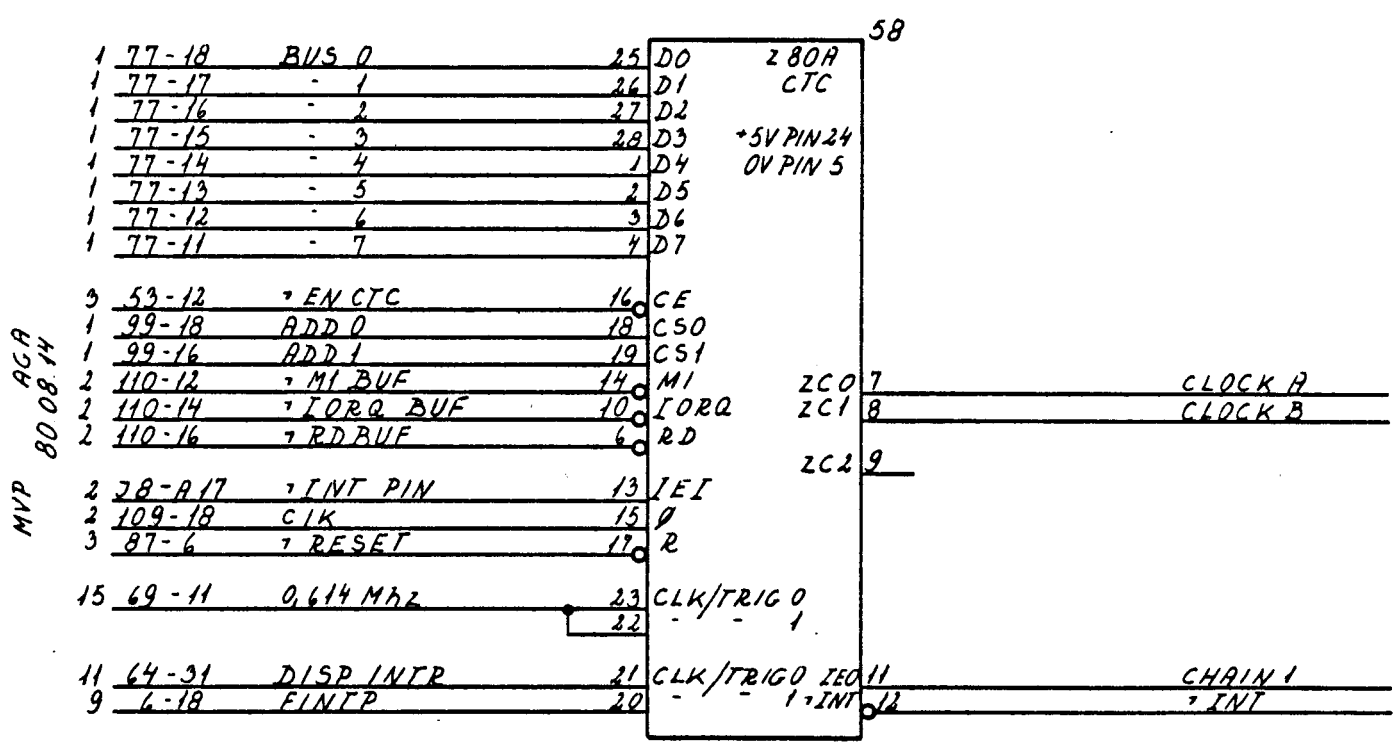
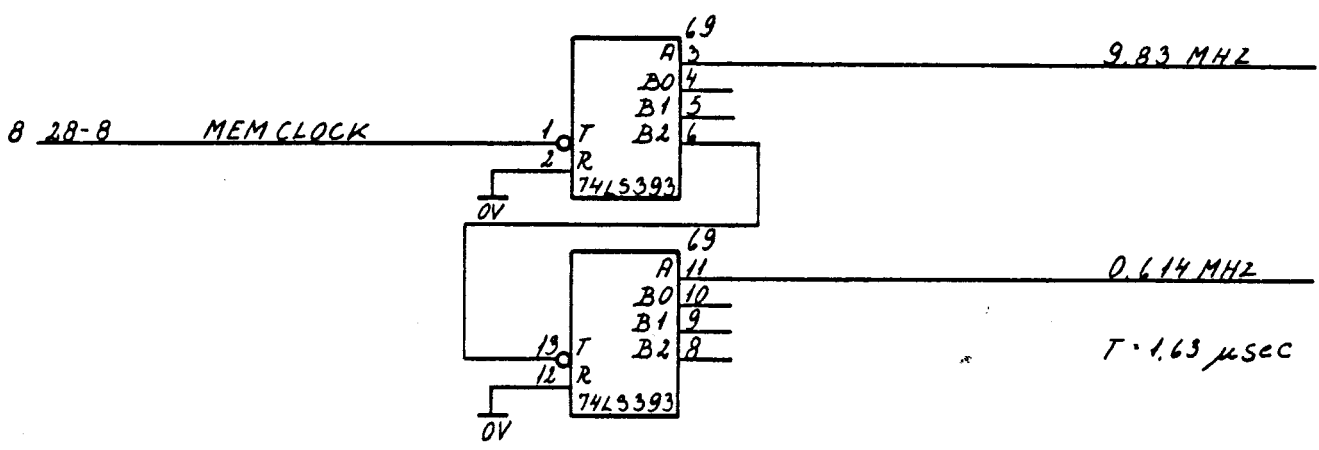
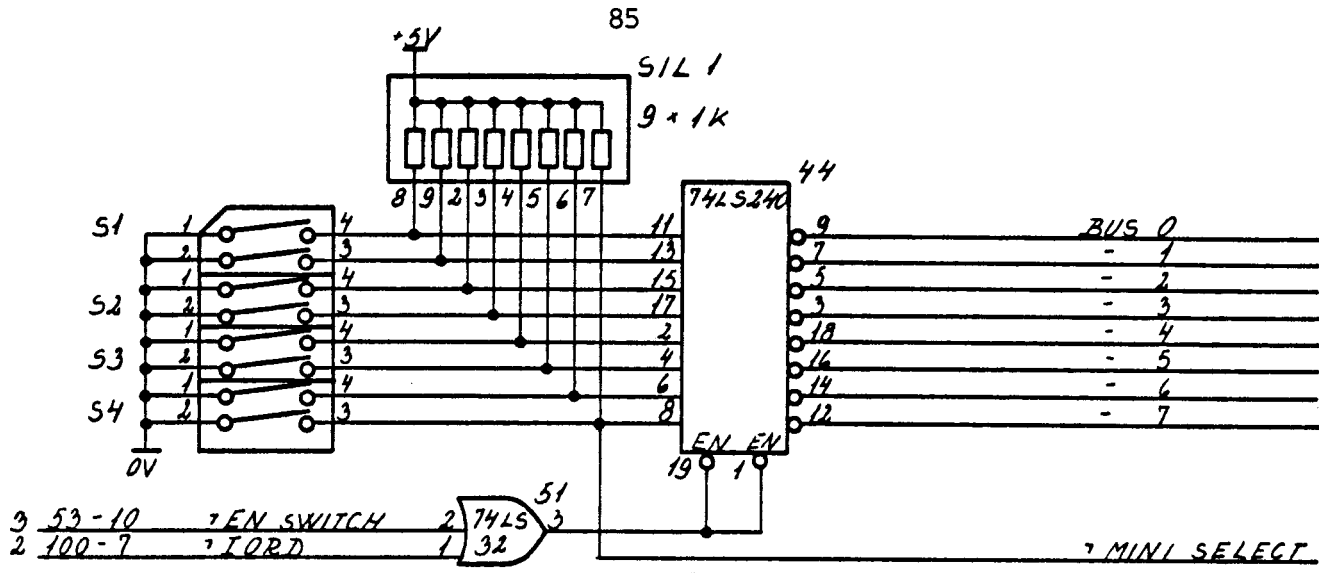
MVP 80 08 14
AGA



R36	1	2	LOGICAL ONE
R17	1	2	-
R35	1	2	-
R3	1	2	-
R18	1	2	-

5x1K

Signal	Destination MIC No.	Description
BUS(0:7)	1	The data bus is the TRI-state bus supplying data information between the CPU and all of the controllers.
MINI SELECT	8, 9	Control signal selects Mini floppy disk drives. The signal is supplied to the clock generator and divides the clock signals to the floppy controller by two.
9.63 MHz	2	Clock of 9.63 MHz is not used on the board but supplied to the output plug J8.
0.614 MHz	15	Clock of 0.614 MHz is used as input to the counter timer controller to be counted down to make the clock signal to the two Serial In/Out Channels.
CLOCK A	16	Clock signal to the two Serial In/Out Channels just mentioned.
CLOCK B	16	
CHAIN 1	16	Interrupt priority chain
INT		Interrupt from the counter timer controller.



MIC 702
R 13091

SWITCH INPUT TO PROGRAM & BAUD RATE GENERATOR MIC 15

Signal	Destination MIC No.	Description
WAIT	4	This open collector output from the SIO is connected to the WAIT signal generated on page 04 and slows the CPU down to wait for the SIO.
INT	2	Interrupt request from the SIO/2.
CHAIN	2	Interrupt priority chain out from the SIO/2.

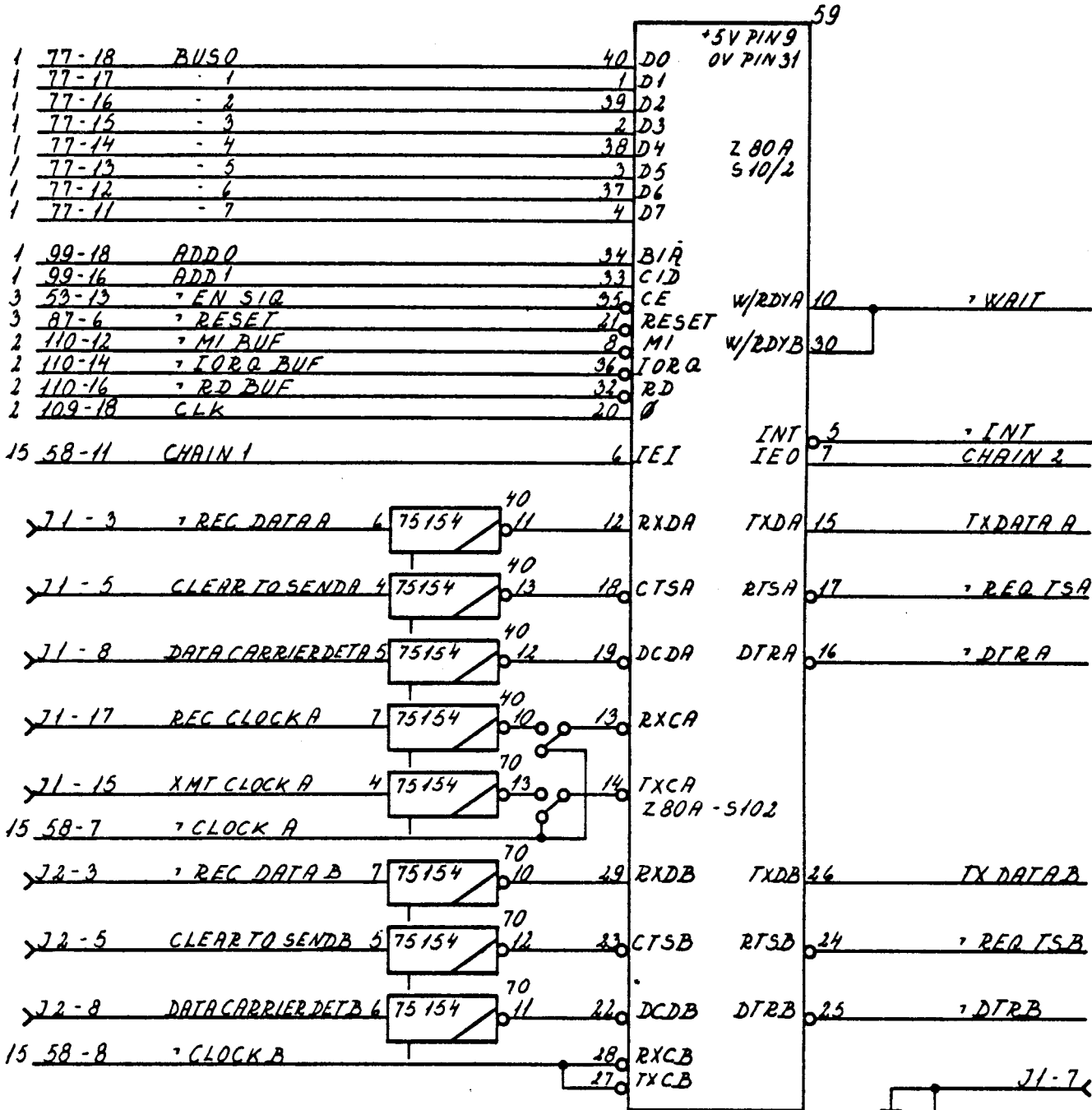
V.24 input outputs

Pin 2 TRANS DATA

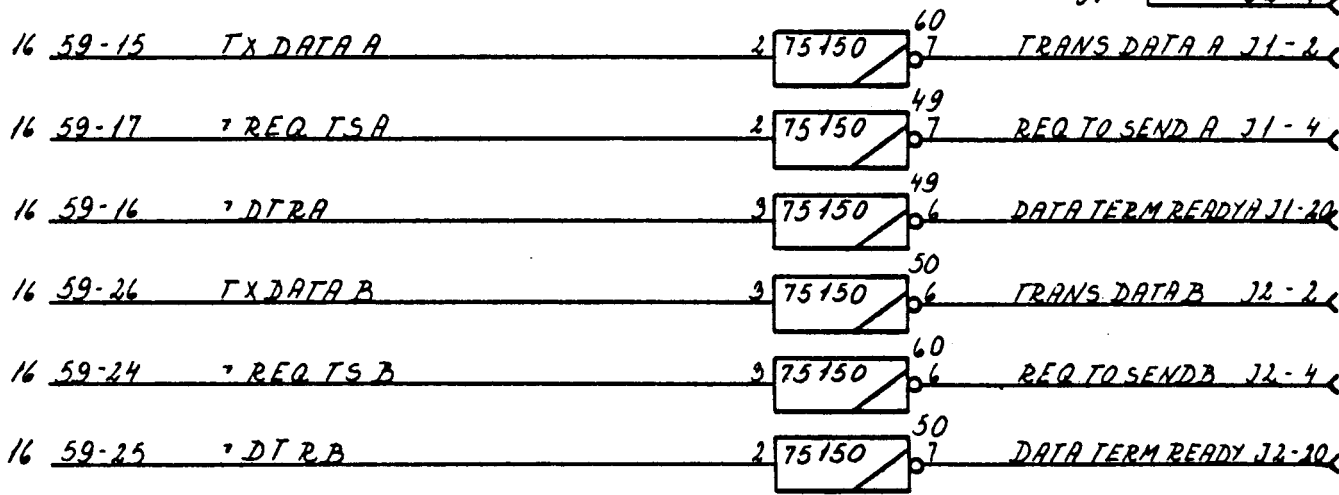
- 3 REC DATA
- 4 REQ TO SEND
- 5 CLEAR TO SEND
- 7 Ground
- 8 DATA CARRIER DETECT
- 20 DATA TERM READY

J1 to channel A (Terminal)

J2 to channel B (Printer)



MVP
80 08.14
RCA



MIC 702
R13092

SERIAL INPUT OUTPUT

MIC 1

The character generator is made of the ROM with the technical name ROA296 and the layout is shown in fig. 2.5. The different national alphabets are chosen via the software.

Fig. 2.6 shows the ROM with the name ROA327 which makes the semigraphic alphabeth.

				b ₇	0	0	0	0	1	1	1	1
				b ₆	0	0	1	1	0	1	0	1
				b ₅	0	1	0	1	0	1	0	1
b ₄	b ₃	b ₂	b ₁		0	16	32	48	64	80	96	112
0	0	0	0	0	0	16	32	48	64	80	96	112
0	0	0	1	1	0	16	32	48	64	80	96	112
0	0	1	0	2	0	16	32	48	64	80	96	112
0	0	1	1	3	0	16	32	48	64	80	96	112
0	1	0	0	4	0	16	32	48	64	80	96	112
0	1	0	1	5	0	16	32	48	64	80	96	112
0	1	1	0	6	0	16	32	48	64	80	96	112
0	1	1	1	7	0	16	32	48	64	80	96	112
1	0	0	0	8	0	16	32	48	64	80	96	112
1	0	0	1	9	0	16	32	48	64	80	96	112
1	0	1	0	10	0	16	32	48	64	80	96	112
1	0	1	1	11	0	16	32	48	64	80	96	112
1	1	0	0	12	0	16	32	48	64	80	96	112
1	1	0	1	13	0	16	32	48	64	80	96	112
1	1	1	0	14	0	16	32	48	64	80	96	112
1	1	1	1	15	0	16	32	48	64	80	96	112

Fig. 2.5. CHARACTER GENERATOR ROA 296

MIC 702
R 13093

				b ₇	0	0	0	0	1	1	1	1
				b ₆	0	0	1	1	0	0	1	1
				b ₅	0	1	0	1	0	0	0	1
b ₄	b ₃	b ₂	b ₁		0	16	32	48	64	80	96	112
0	0	0	0	0								
0	0	0	1	1								
0	0	1	0	2								
0	0	1	1	3								
0	1	0	0	4								
0	1	0	1	5								
0	1	1	0	6								
0	1	1	1	7								
1	0	0	0	8								
1	0	0	1	9								
1	0	1	0	10								
1	0	1	1	11								
1	1	0	0	12								
1	1	0	1	13								
1	1	1	0	14								
1	1	1	1	15								

Fig. 2.6 SEMIGRAPHIC CHARACTER GENERATOR ROA 327

MIC 702
R 13094

3. KBN702 CABINET WITH CABLES ECT.

3.

Fig. 3.1 shows the cabinet KBN702 with the power supply POW739 mounted. The cabinet itself contains transformer, blower, mains connection, rectifier unit RC702, and the internal cable.

Fig. 3.2 shows the cabinet with MIC702 mounted.

Fig. 3.3 shows diagram for rectifier unit and transformer, blower, and main connection.

Fig. 3.4 shows the internal cable in the KBN702.

Fig. 3.5 shows the cables connection KBN702 to MIC702 and POW739.

Fig. 3.6 shows the power cable CBL440.

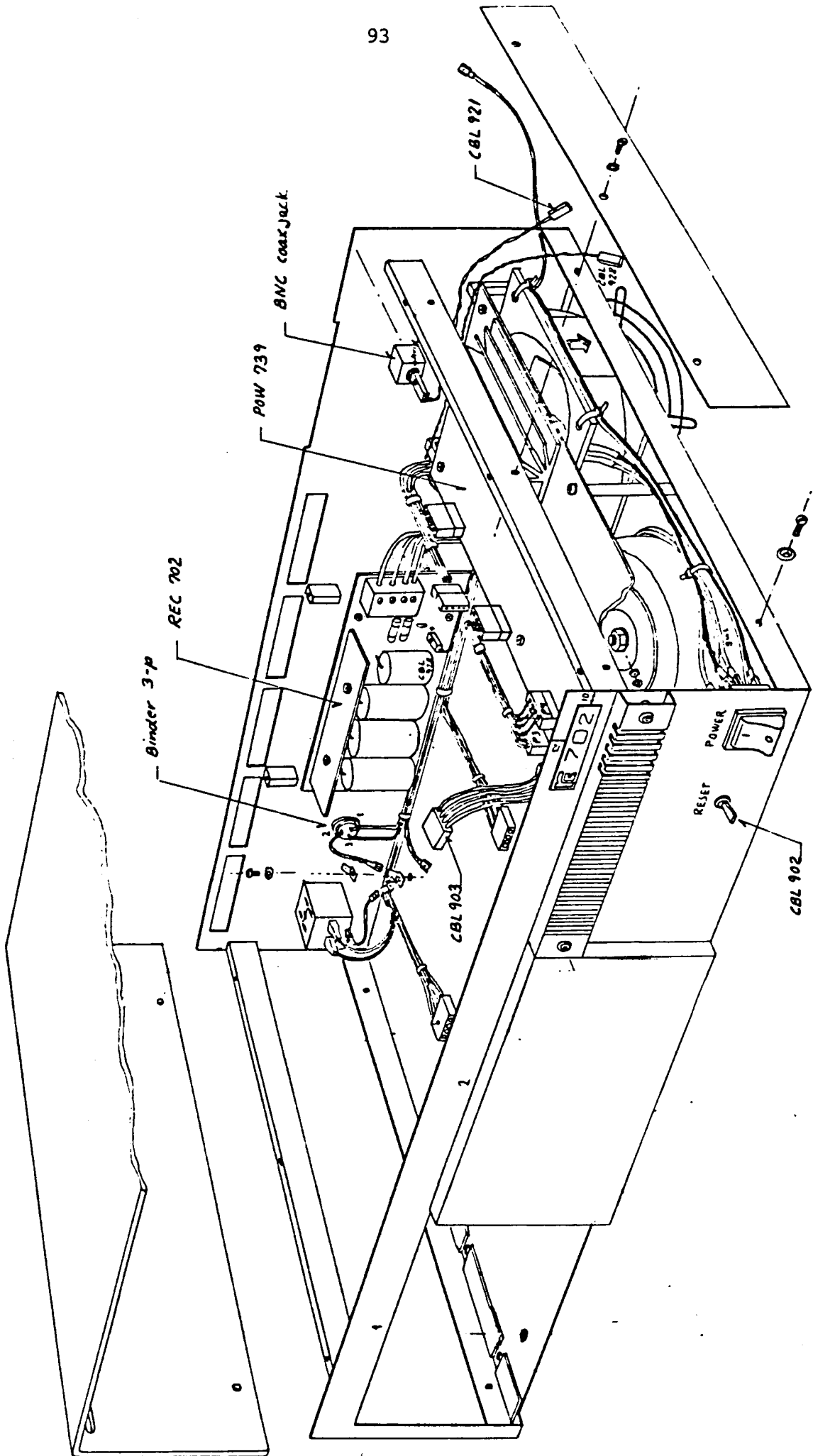


Fig. 3.1. KBN 702 with POW 739 mounted.

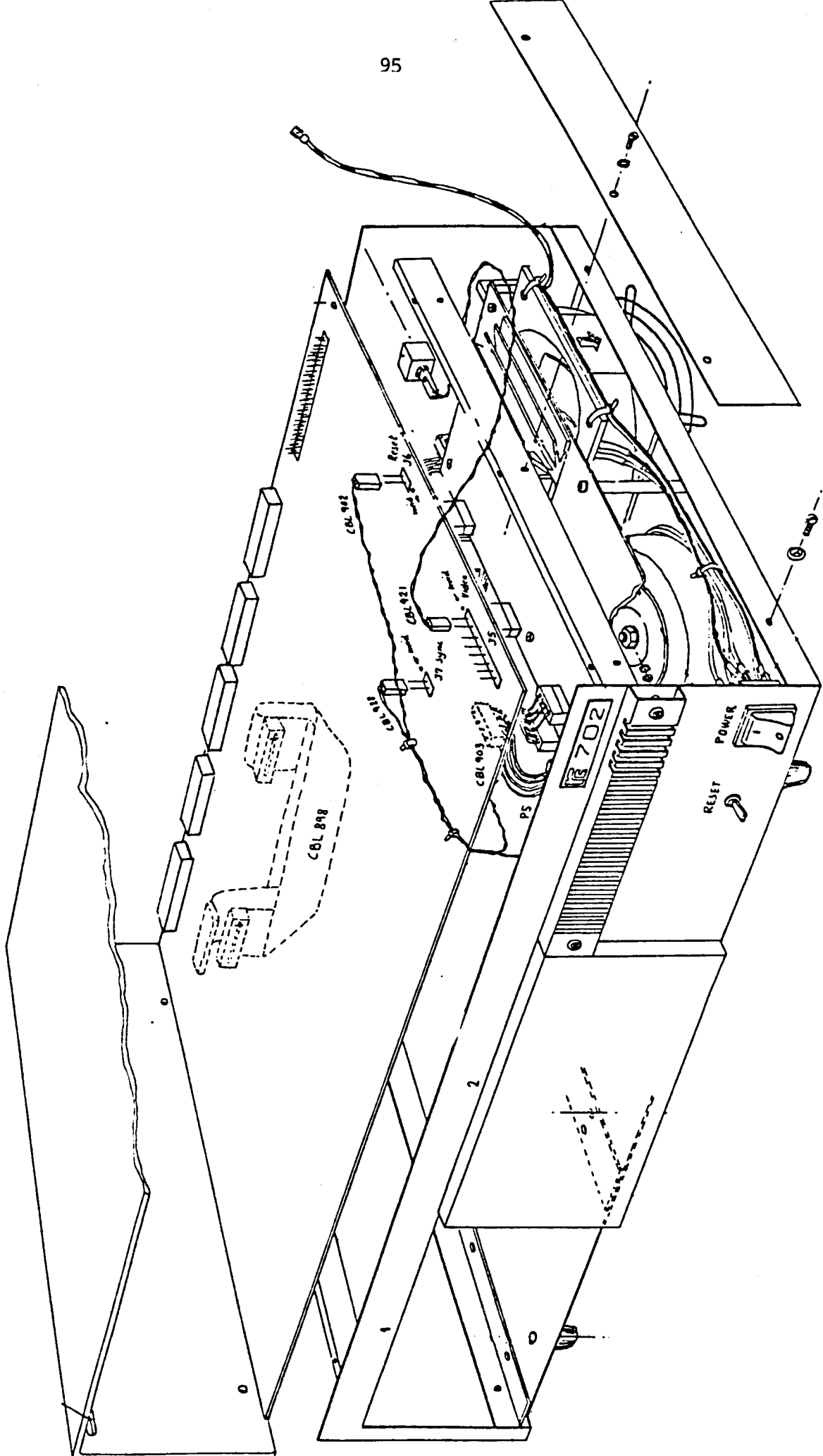
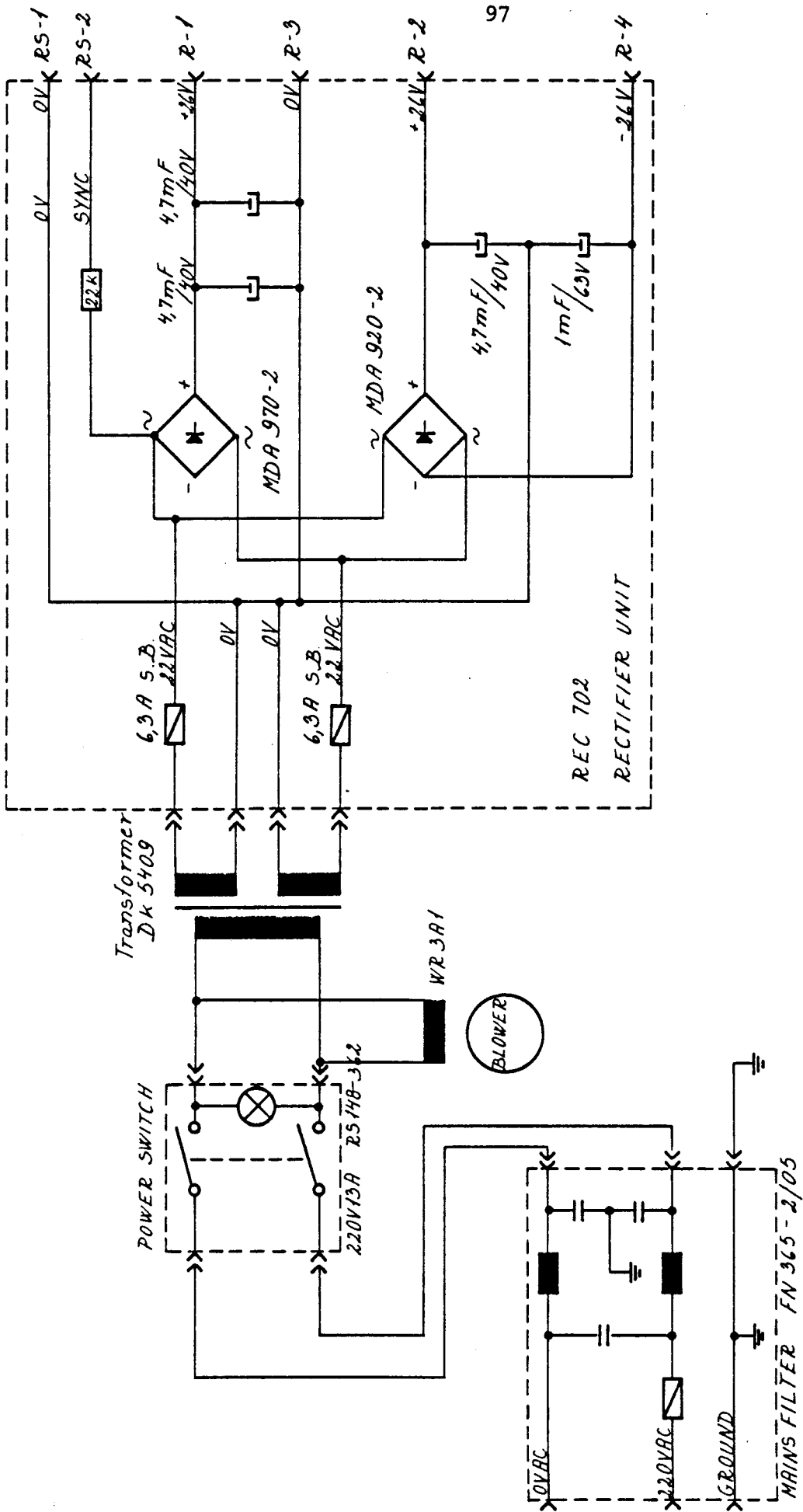
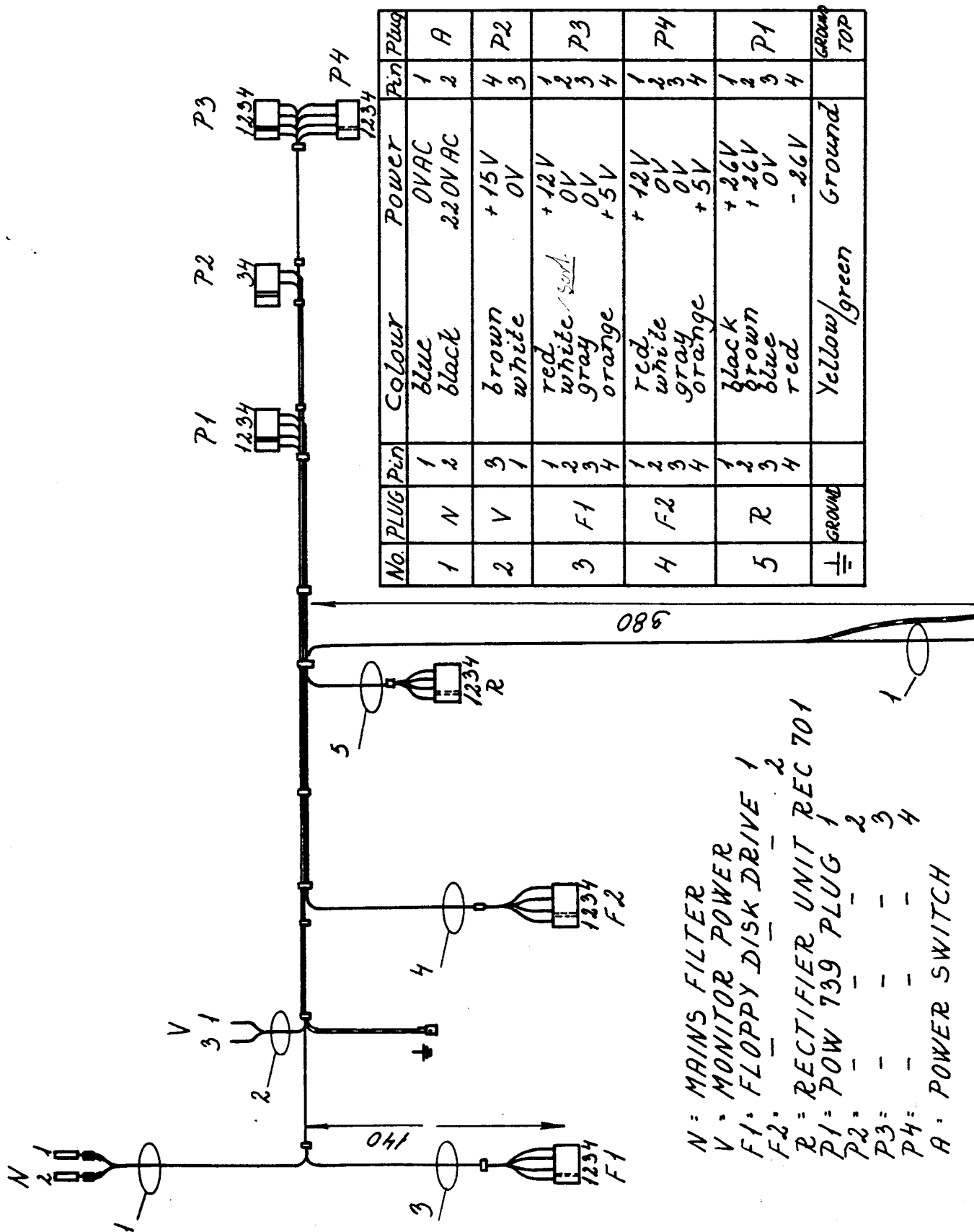


Fig. 3.2. KBN 702 with MIC 702 mounted.



MIC 702
R 13095

Fig. 33. Fuller, Transformer, Blower and REC 702.



N = MAINS FILTER
 V = MONITOR POWER
 F1 = FLOPPY DISK DRIVE 1
 F2 = FLOPPY DISK DRIVE 2
 R = RECTIFIER UNIT REC 701
 P1 = POW 739 PLUG 1
 P2 = - - - 2
 P3 = - - - 3
 P4 = - - - 4
 A = POWER SWITCH

Fig. 3.4. Internal Cable in KBN 701.

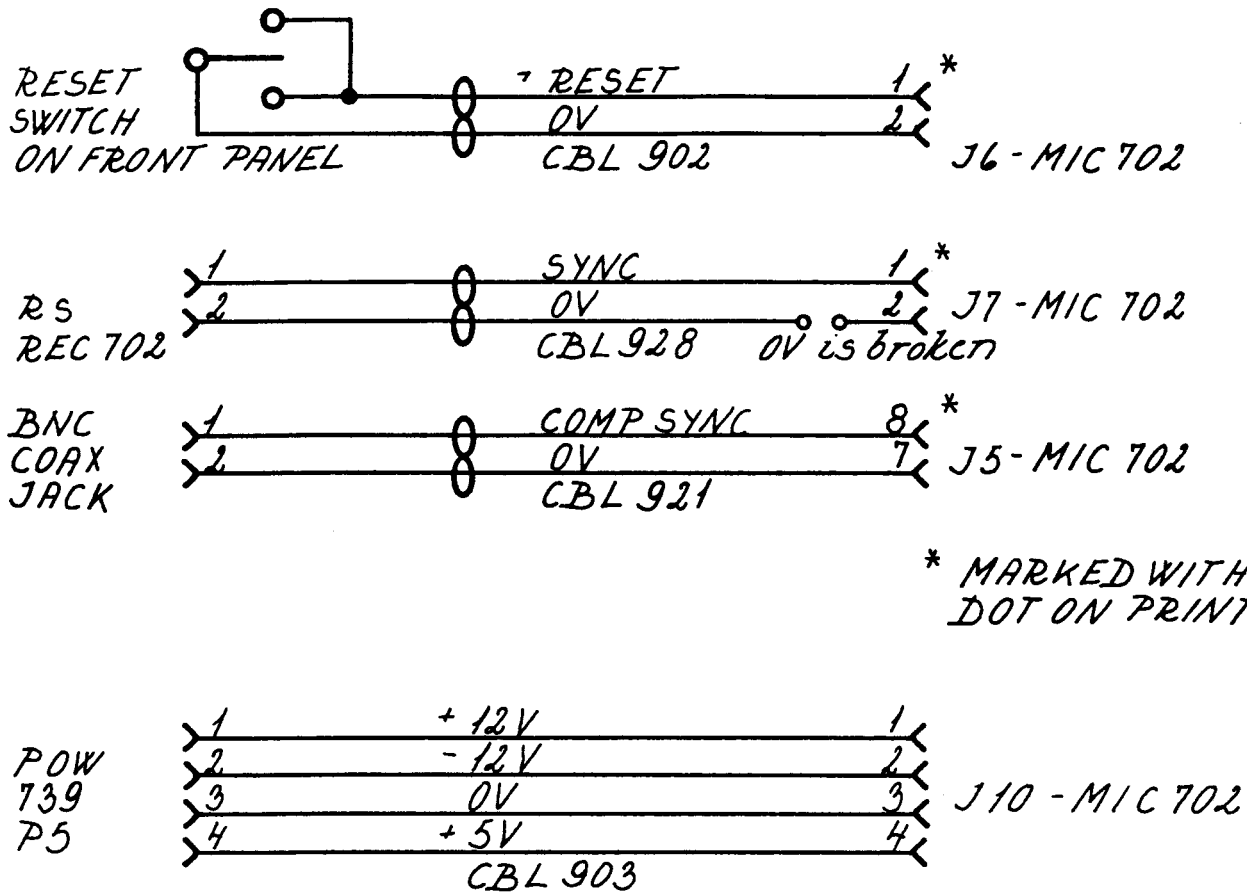




Fig. 3.5. Cable Connections KBN 702 to MIC 702 and POW 739.

Connector	Wire	Connector
F	BROWN	L
	YELLOW/GREEN	
0	BLUE	N

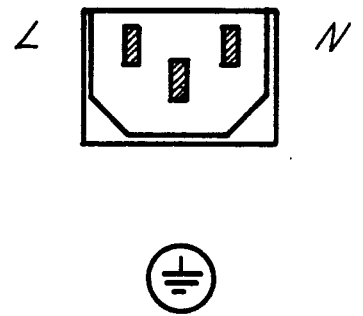
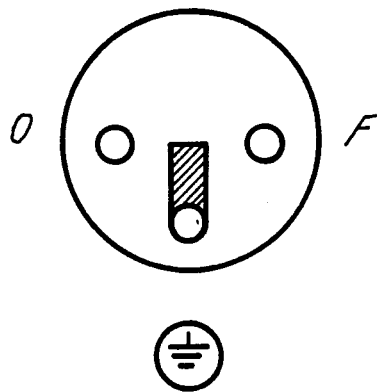


Fig. 3.6. Power Cable CBL 440.

4. POW739 POWER SUPPLY

4.

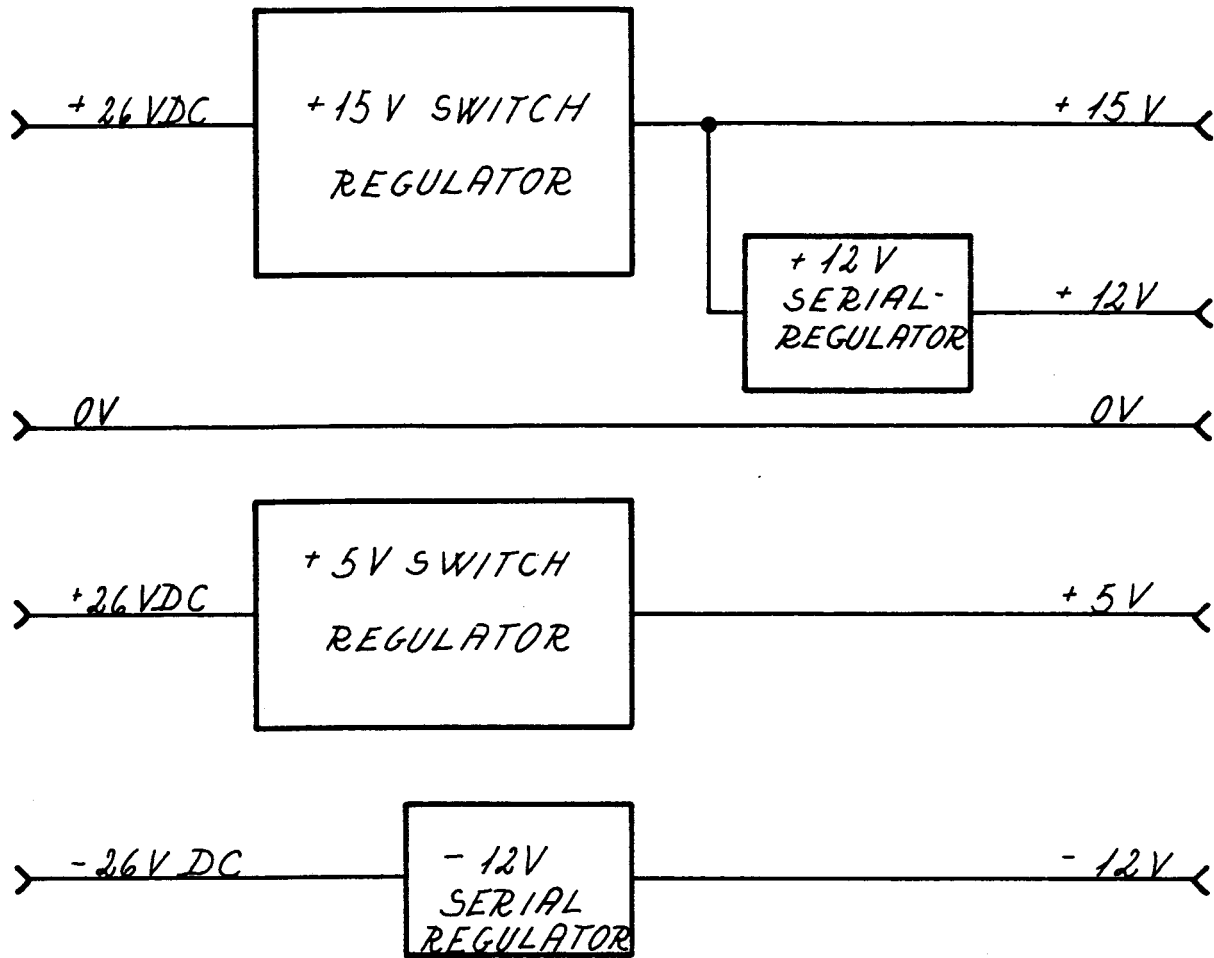
The power supply to RC702 is built on a single printed circuit board. Fig. 4.1 shows a block diagram for the POW739.

Input to the powersupply is +26 V DC or -26 V DC delivered from REC702 rectifier unit. This unit is described in chapter 3.

Fig. 4.2 shows the layout of the printed circuit board.

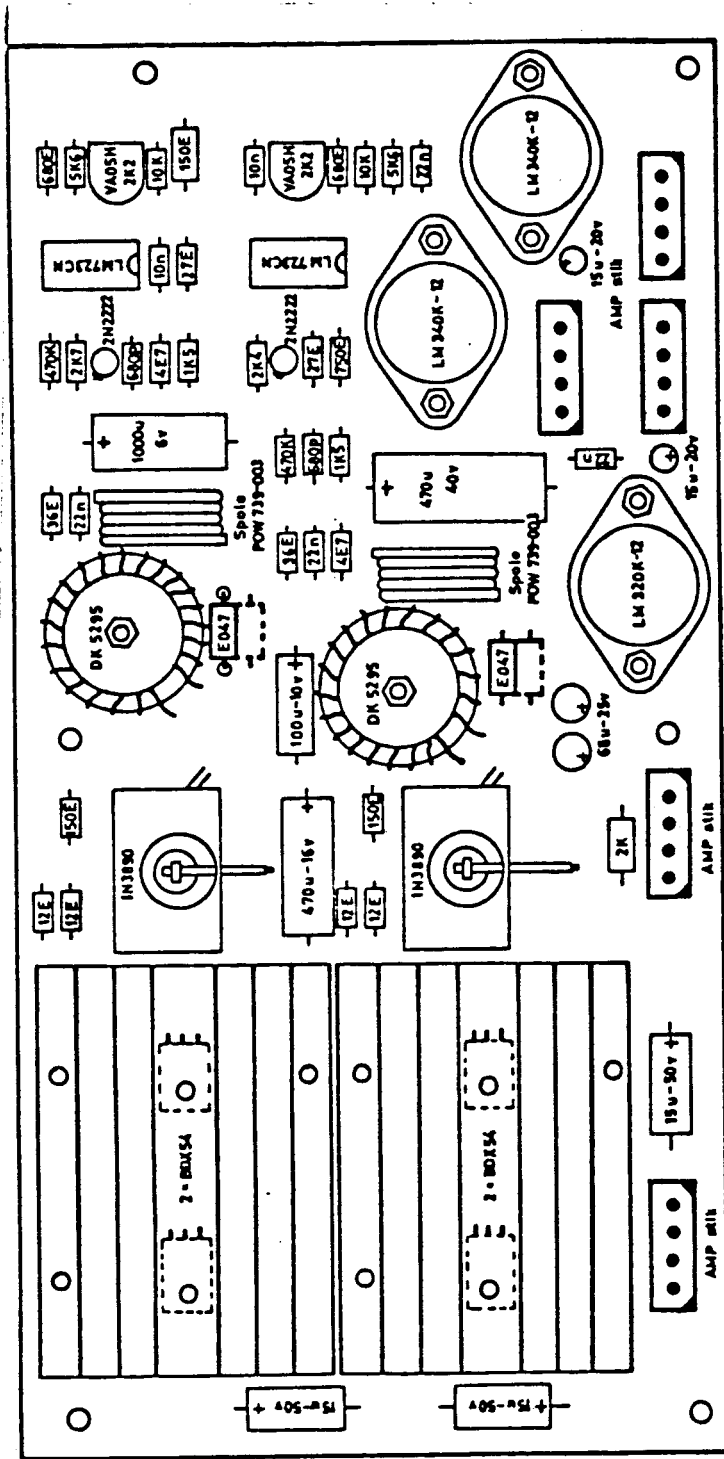
Fig. 4.3 and fig. 4.4 show the circuit diagram for the unit.

Fig. 4.5 and fig. 4.6 show the timing diagram for the unit.



V_{OUT}	I_{MAX}	ΔV_{MAX}
$+15\text{V}$	$1,4\text{A}$	$\pm 0,5\text{V}$
$+12\text{V}$	$2,6\text{A}$	$\pm 0,5\text{V}$
$+5\text{V}$	$5,0\text{A}$	$\pm 0,1\text{V}$
-12V	$0,2\text{A}$	$\pm 0,5\text{V}$

Fig. 4.1. POW 739 Block Diagram.



P5 to MIC 702

MICRO PROCESSOR

P3, P4 to RC 761

FLOPPY DISK DRIVE

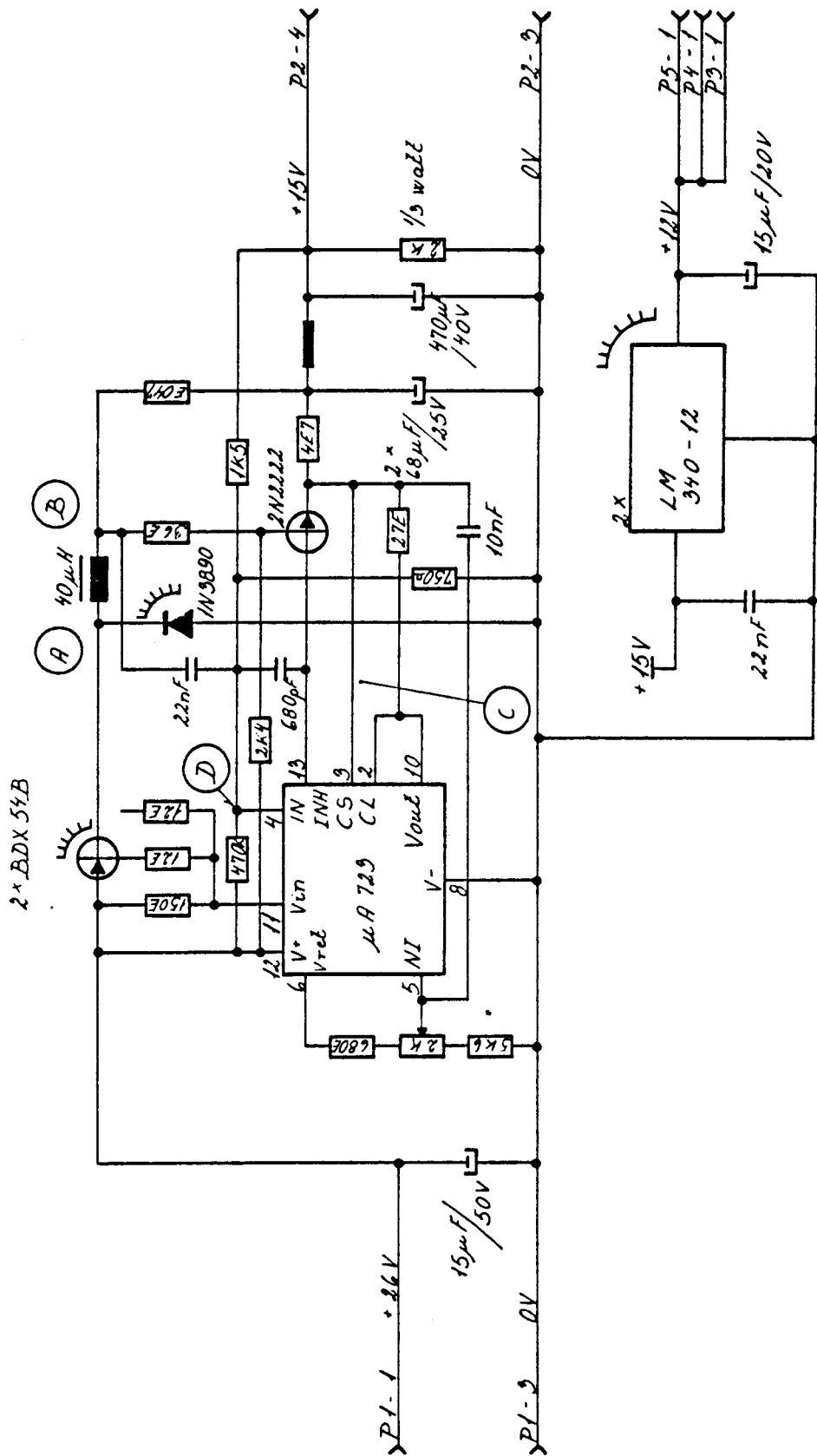
P2 to RC 752

VIDEO MONITOR

P1 from REC 701

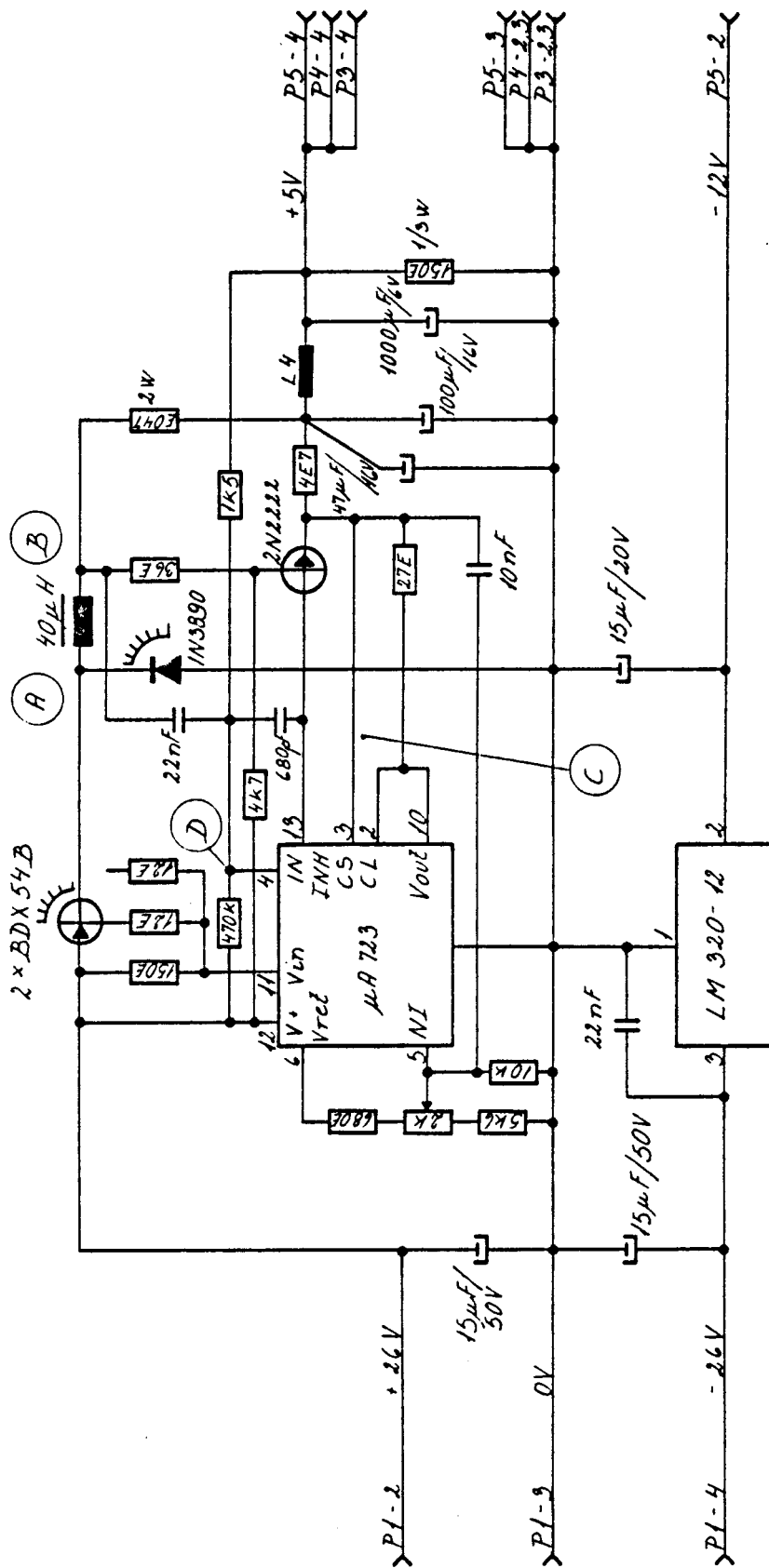
RECTIFIER UNIT

Fig. 4.2. POW 739 LAY OUT



MIC 702
R 13096

Fig. 4.3. POW 739, +15V and +12V



MIC 702
R 13097

Fig. 4.4 POW 739, +5V and -12V

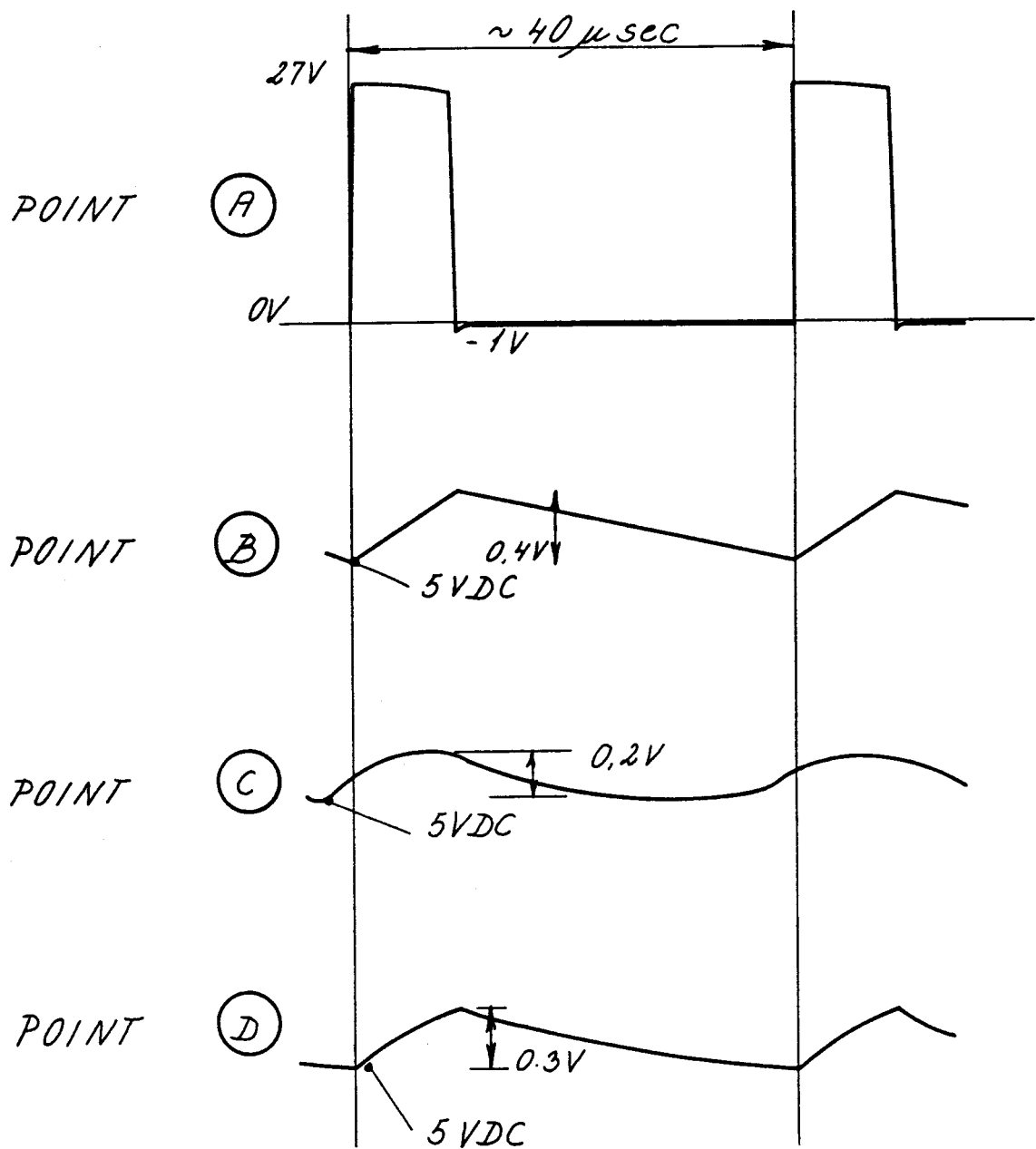


Fig. 4.5. Timing diagram for +5V supply loaded with MIC 702 and one mini floppy.

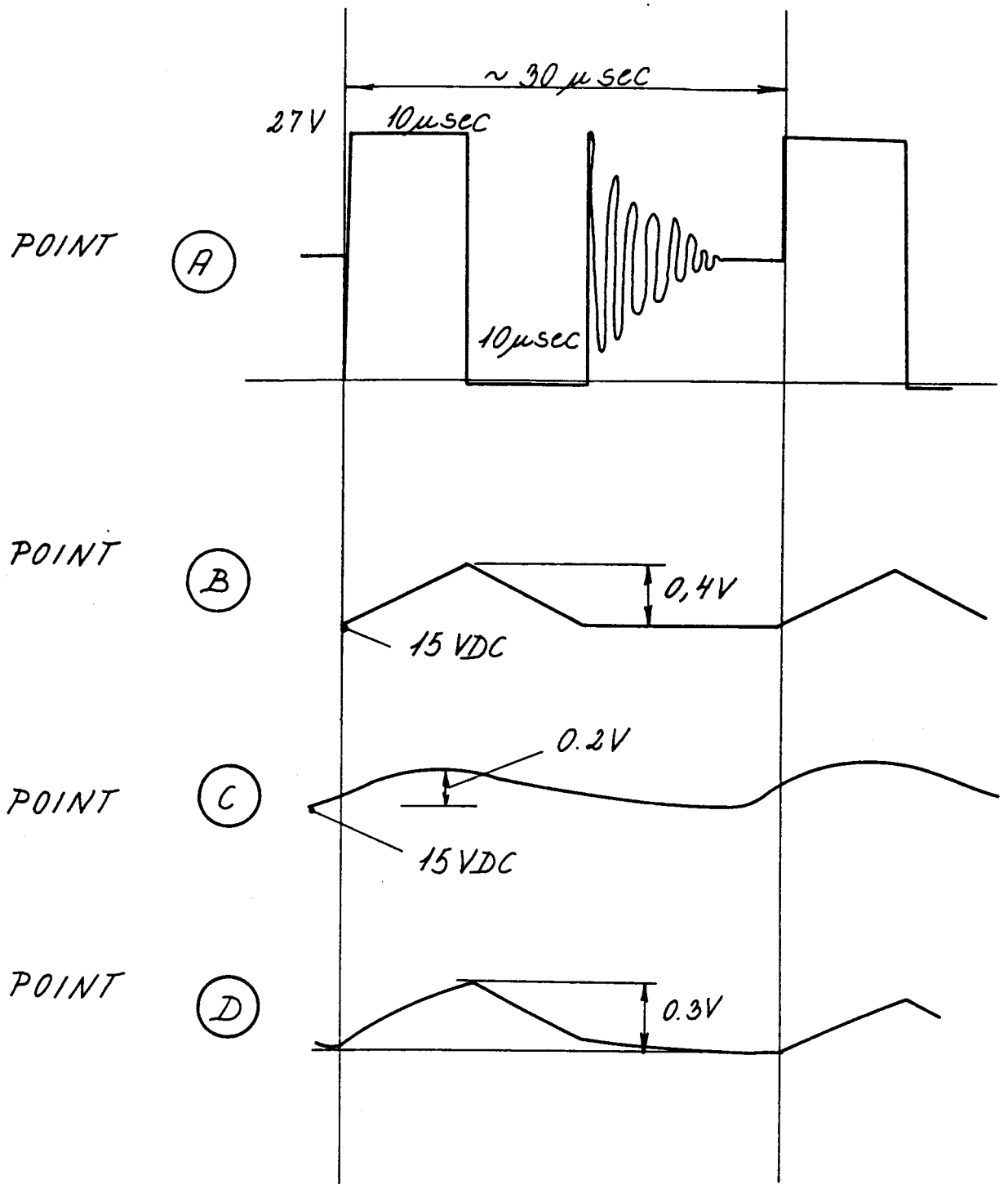


Fig. 4.6. Timing Diagram for +15V supply Loaded with MIC 702 and mini Floppy and RC 752.

RETURN LETTER

Title: RC702 Microcomputer, Technical Manual RCSI No.: 44-RT1974

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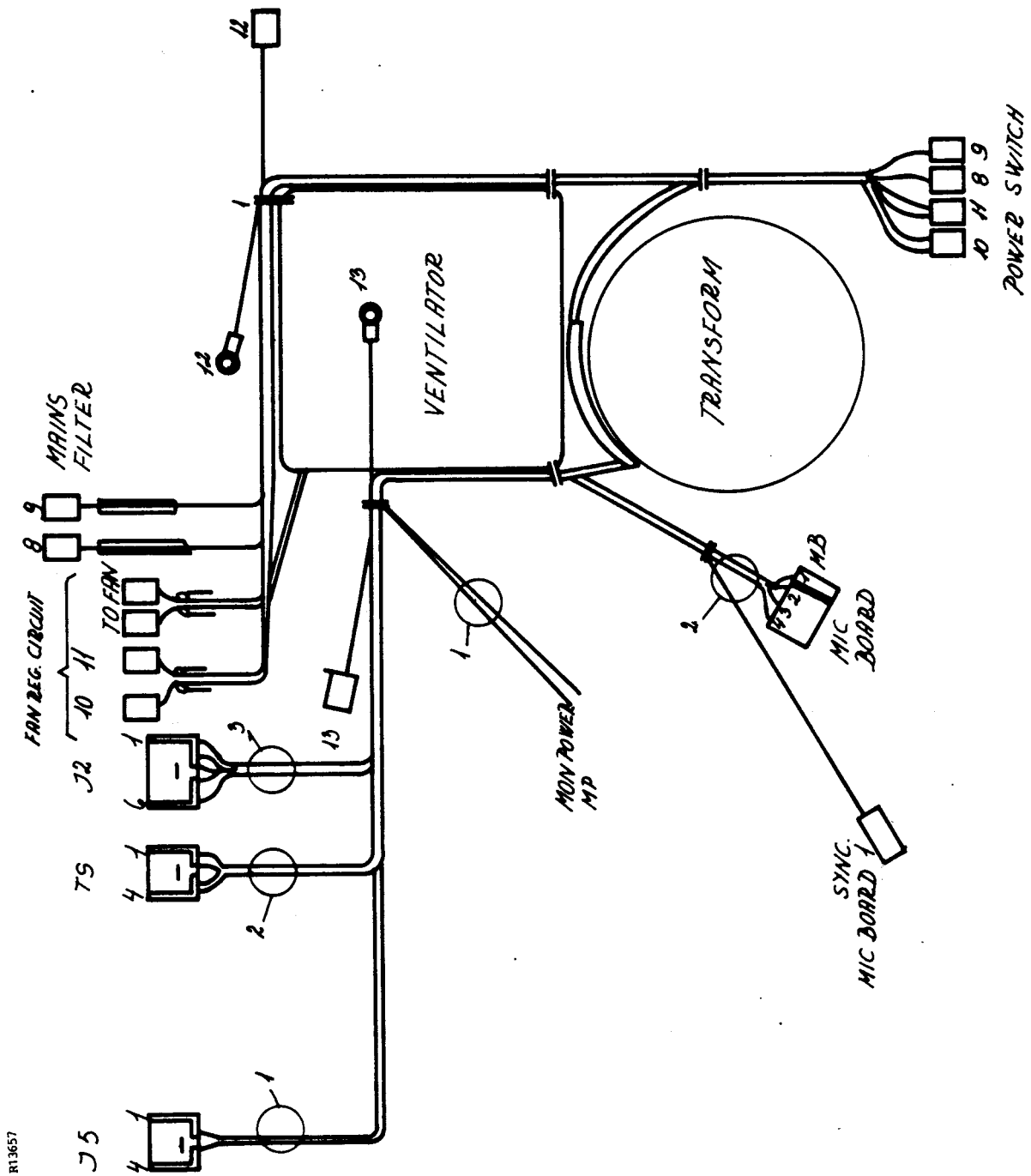
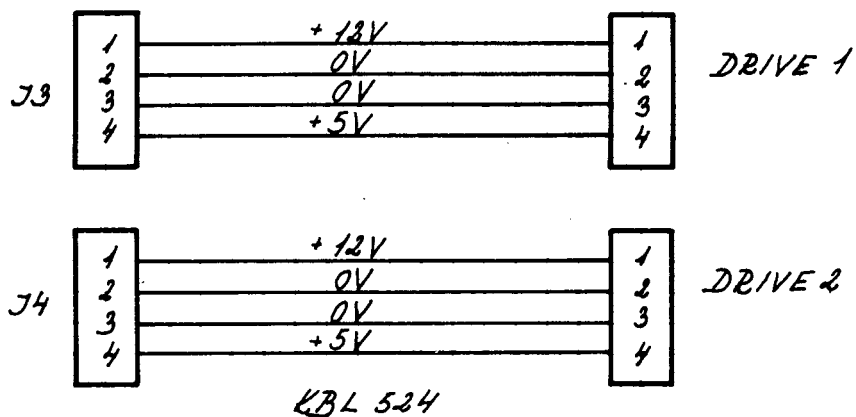


Figure 49: KEN705; internal cables.



Power Cables to mini Floppy drives

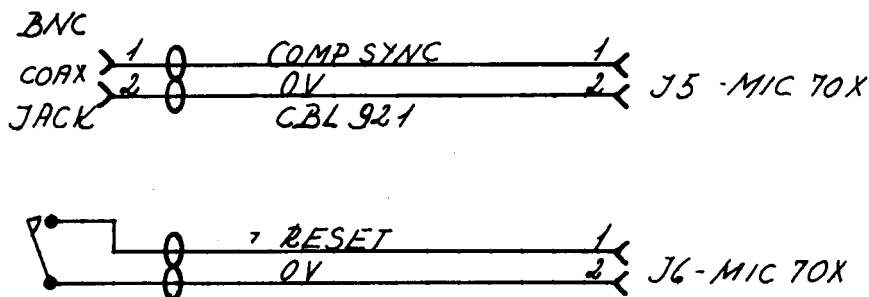


Figure 50: KEN705; cable connections to MIC70x and Floppy Disc Drive.

The POW746 - Power Supply is built on a single print board.

Fig. 51 shows the block diagram for the power supply, including the input/output connections. Input is 2x24 V AC which is supplied by the transformer (DK7755) housed in KEN705.

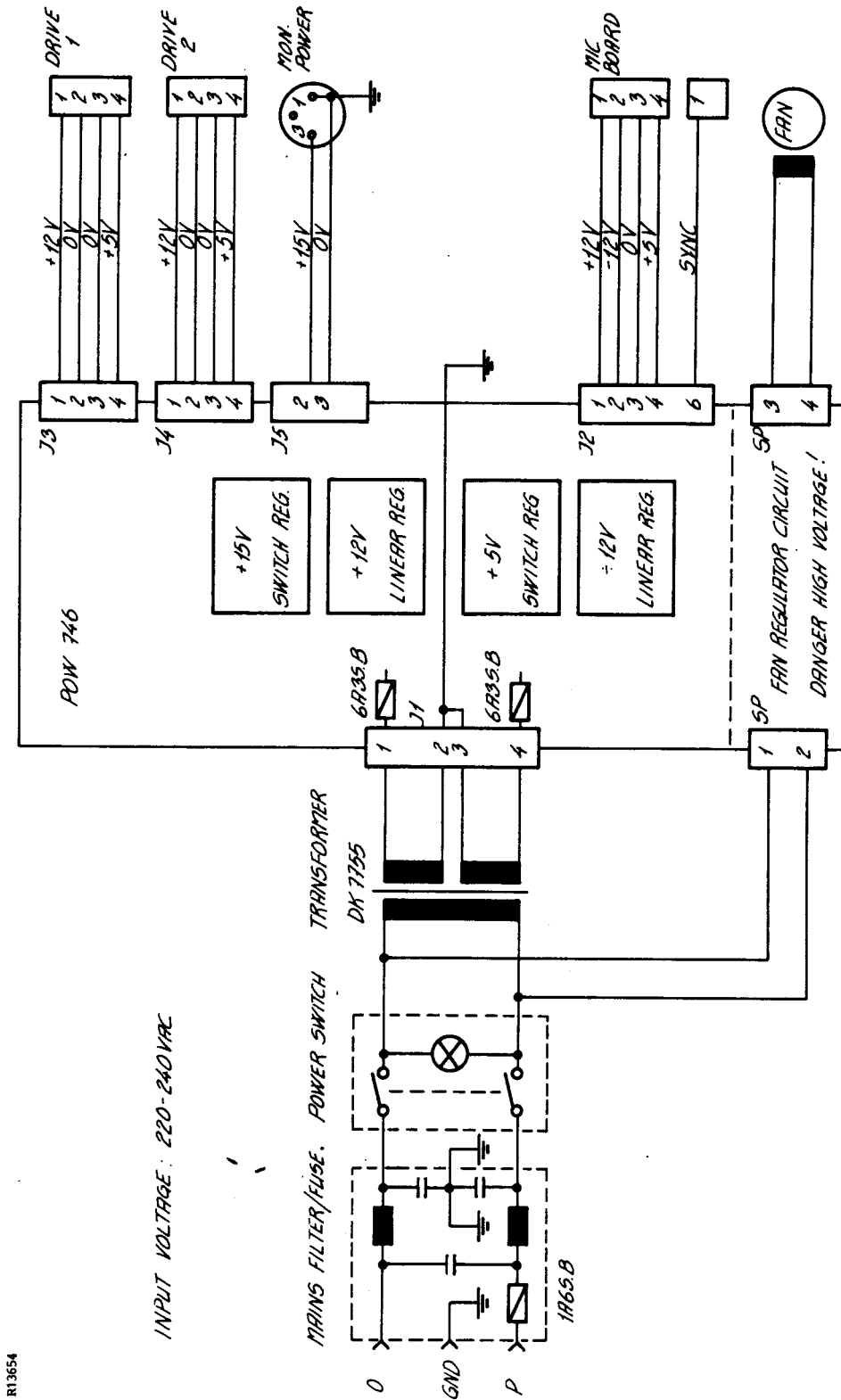
Fig. 52 gives the specifications for POW746 and transformer (DK7755).

Note: Input voltage range covers both Continental Europe and United Kingdom.

Fig. 53 shows the POW746 Layout.

Fig. 54 shows the Circuit diagram for POW746.

Fig. 55 shows the timing diagram for POW746.



R13654

Figure 51: POW746; block diagram.

Input voltage: 220 V - 240 V \pm 10%, 50 Hz

Power consumption: Max. 150 W

Output voltages:

V out	V out	V ripple	I max
+15 V	\pm 0,5 V	<100 mV _{pp}	1,4 A
+12 V	\pm 0,5 V	< 50 mV _{pp}	2,6 A
+ 5 V	\pm 0,5 V	< 50 mV _{pp}	5 A
-12 V	\pm 0,5 V	<100 mV _{pp}	0,2 A

Fan regulator range: \sim 0-1600 rpm.

Figure 52: POW746; power specifications.

OUTPUT

INPUT

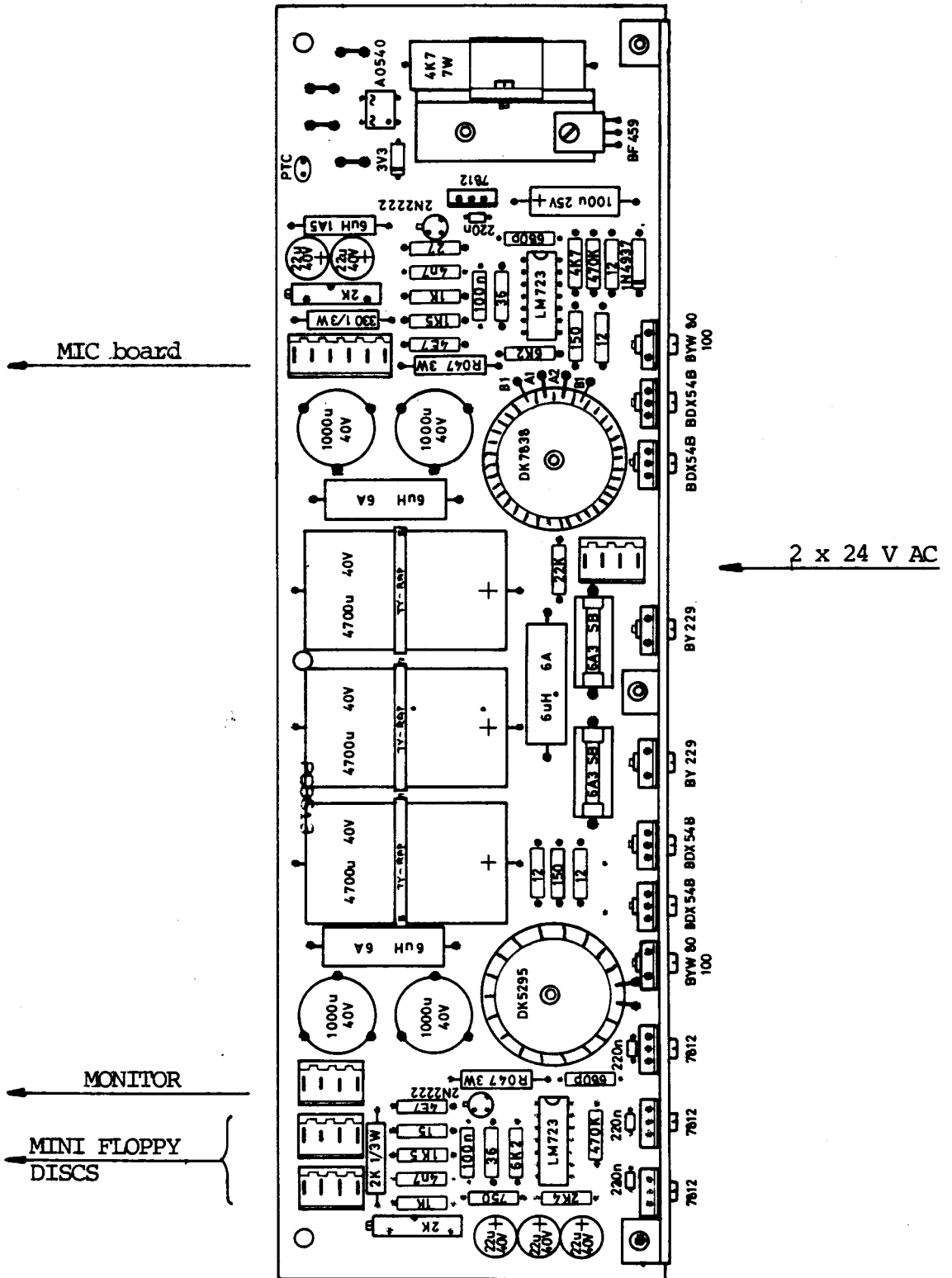
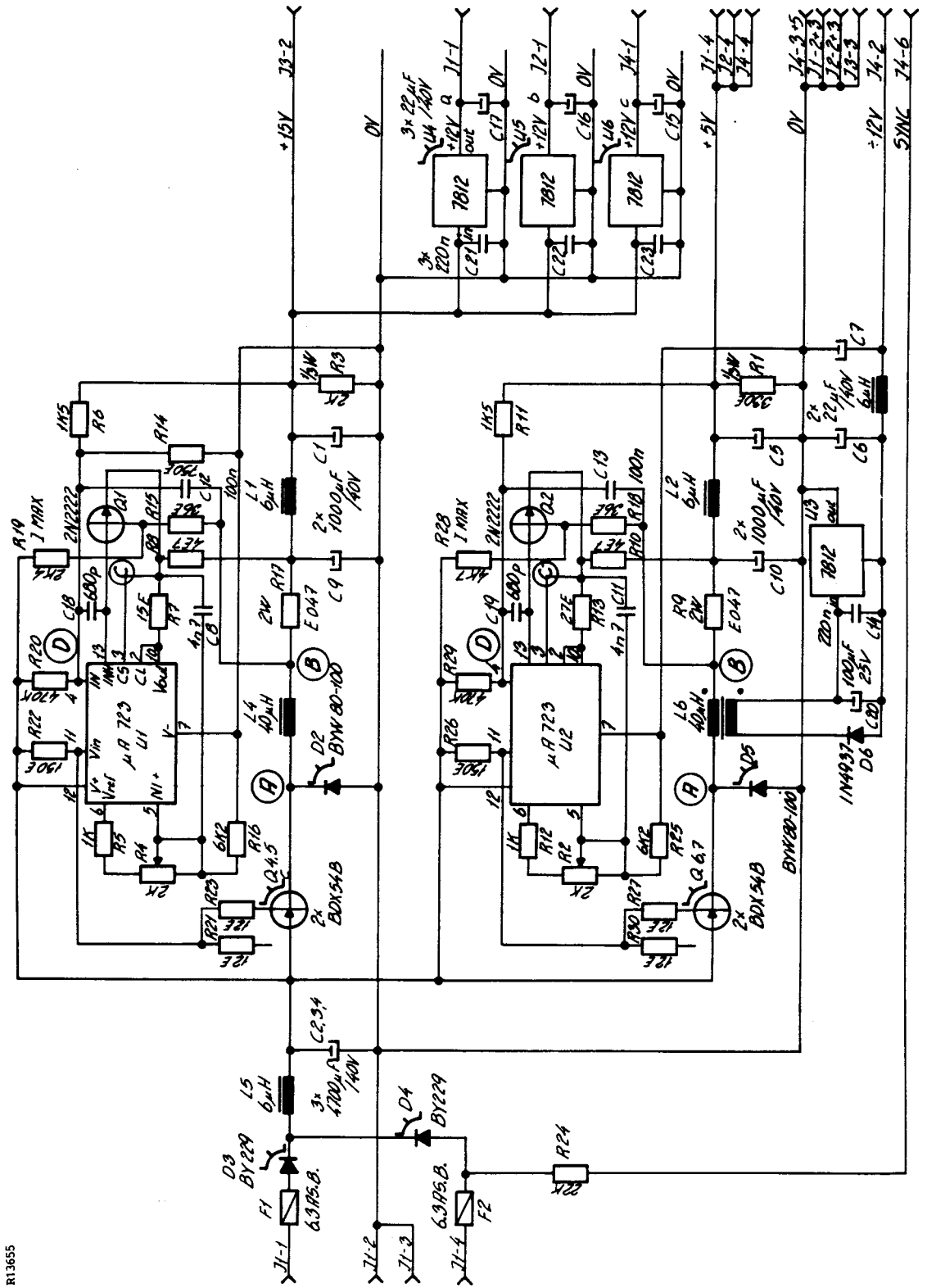
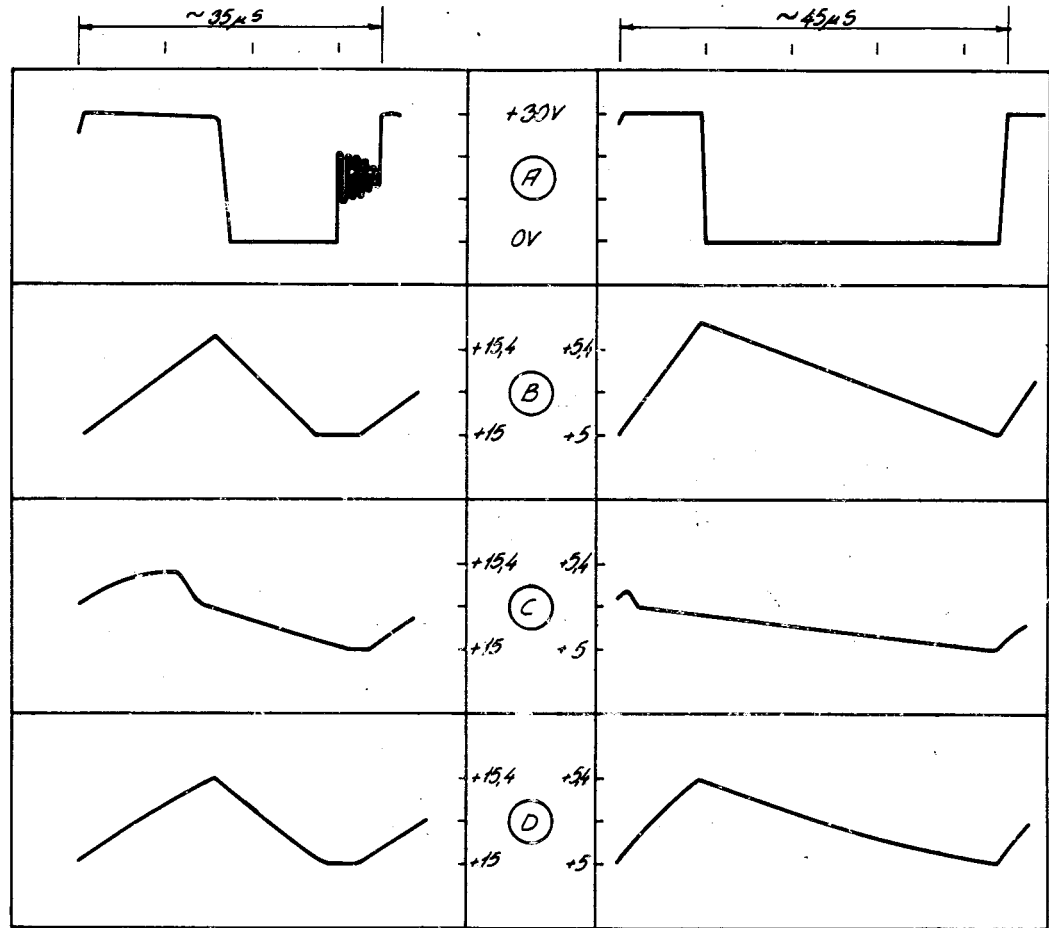


Figure 53: POW746; layout.



R13655

Figure 54: POW746; schematic diagram.



+15V switch. reg.

+5V switch. reg.

Load: +15V, 2A
+5V, 3A

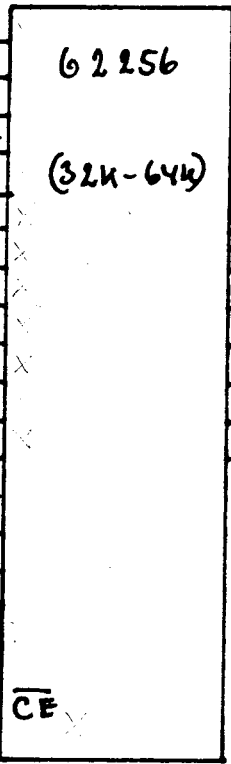
≈

MIC-board
1x5 1/4" drive
Monitor

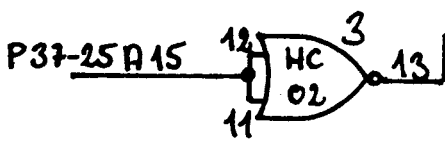
RI 9656

Figure 55: POW746; timing diagram.

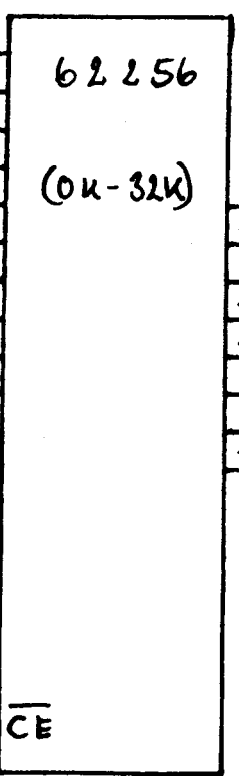
P37-6	ADD 0	10
P37-8	ADD 1	9
P37-10	ADD 2	8
P37-12	ADD 3	7
P37-14	ADD 4	6
P37-16	ADD 5	5
P37-18	ADD 6	4
P37-5	ADD 7	3
P37-4	ADD 8	25
P37-3	ADD 9	24
P37-2	ADD 10	21
P37-1	ADD 11	23
P37-34	ADD 12	2
P37-38	ADD 13	26
P37-24	ADD 14	1
P37-31	MEM WR	27
1-3-1	RAM RD	22



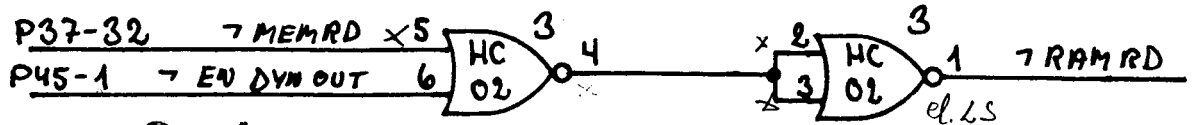
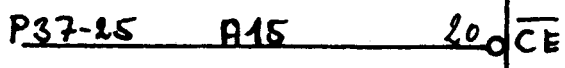
11	BUS 0	P45-2
12	- 1	P45-5
13	- 2	P45-6
15	- 3	P45-9
16	- 4	P45-12
17	- 5	P45-15
18	- 6	P45-16
19	- 7	P45-19



P37-6	ADD 0	10
P37-8	ADD 1	9
P37-10	ADD 2	8
P37-12	ADD 3	7
P37-14	ADD 4	6
P37-16	ADD 5	5
P37-18	ADD 6	4
P37-5	ADD 7	3
P37-4	ADD 8	25
P37-3	ADD 9	24
P37-2	ADD 10	21
P37-1	ADD 11	23
P37-34	ADD 12	2
P37-38	ADD 13	26
P37-24	ADD 14	1
P37-31	MEM WR	27
1-3-1	RAM RD	22



28 VCC
14 GND.



P37-30 SACK pin 30 på org. Lagetcontroller skal jordes

THH 010987

STATIC RAM FOR RC700

RCSL No: 44-RT1980
Edition: February 1981
Author: Mogens V. Pedersen

Title:

RC721 and RC722 Keyboards
Technical Manual

Keywords:

RC700, RC702, RC721, RC722, KTC401, KTC402, KTC403.

Abstract:

This manual contains a technical description of the two keyboards RC721 and RC722.

(26 printed pages)

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RC Computer A/S**

Printed by A/S Regnecentralen af 1979, Copenhagen

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FOREWORD

This paper describes the two keyboards RC721 and RC722. The first is without a numeric block, and the later is with this block. Both keyboards contain the same microcomputer and the same program. The other circuits in the boards are almost identical.

This paper is divided in the following parts:

Keyboards RC721 and RC722

Circuit diagrams

Cable CBL923

Alphabet

National variants.

<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
1. KEYBOARDS RC721 AND RC722	1
2. CABLE CBL923	7
3. ALPHABET	9
4. NATIONAL VERSIONS	11

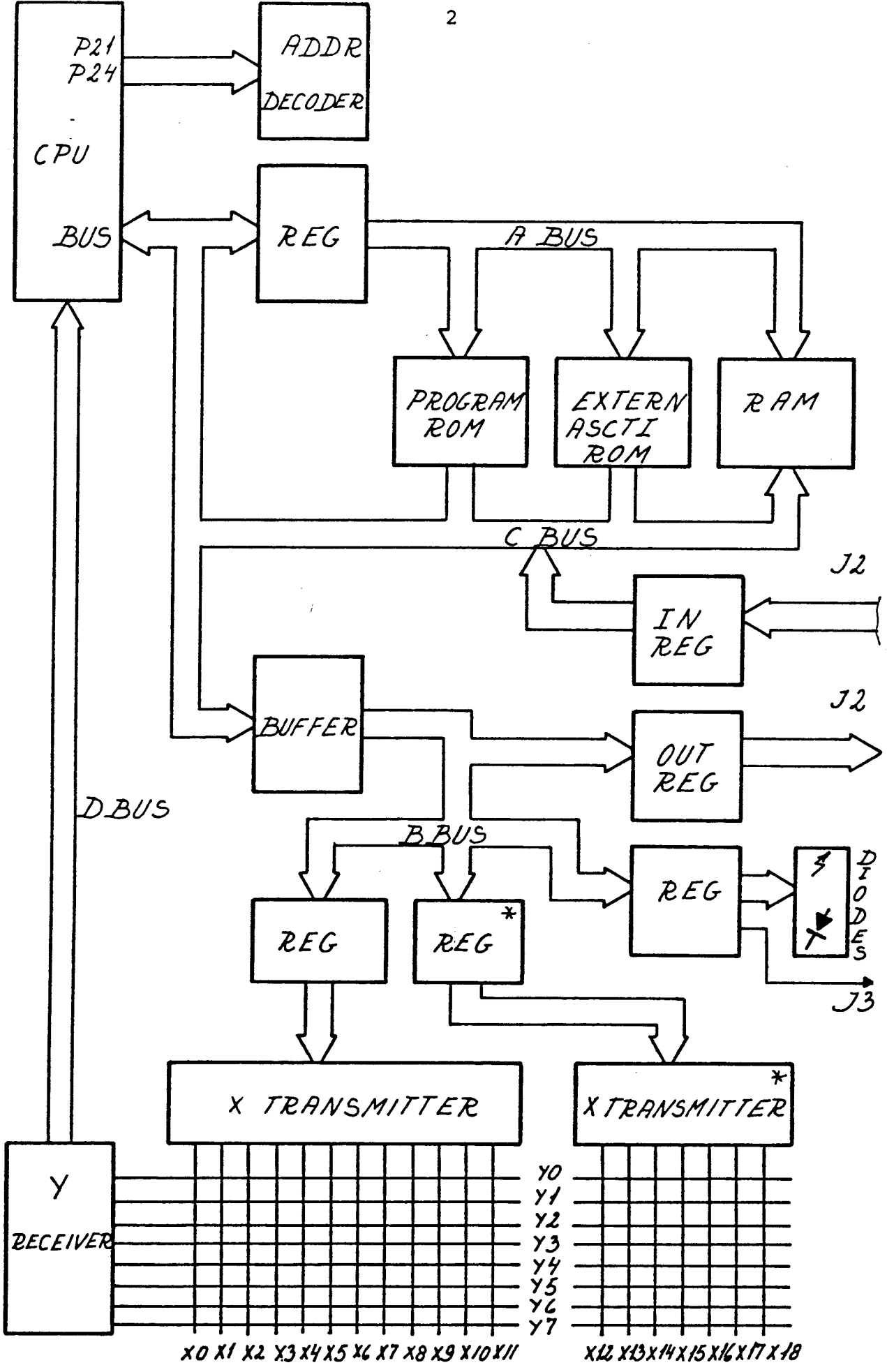
1. KEYBOARDS RC721 and RC722

1.

The technical name for RC721 is KTC401, and for RC722 it is KTC403. The block diagram in fig. 1 shows how the logic is made. The circuit is controlled by a CPU from the Intel family 8048. The block diagram for this CPU is shown in fig. 2. A more detailed description of the CPU may be obtained from an Intel manual.

When a key is pressed the capacity between the X wire and the Y wire increases. The CPU sends an address to the X transmitter, which sends a pulse on the wire addressed. When a key is pressed the pulse is received on the Y wire and information about the position of the pressed key is received by the CPU. The program takes care of any jitter which may accure, and also of the N-KEY roll-over function. The ASCII value of the key pressed is generated by the CPU and sent to the OUT REG together with a strobe signal.

The IN REG and the EXTERN ASCII ROM are not used in KTC401 and KTC403.



MVF 810202

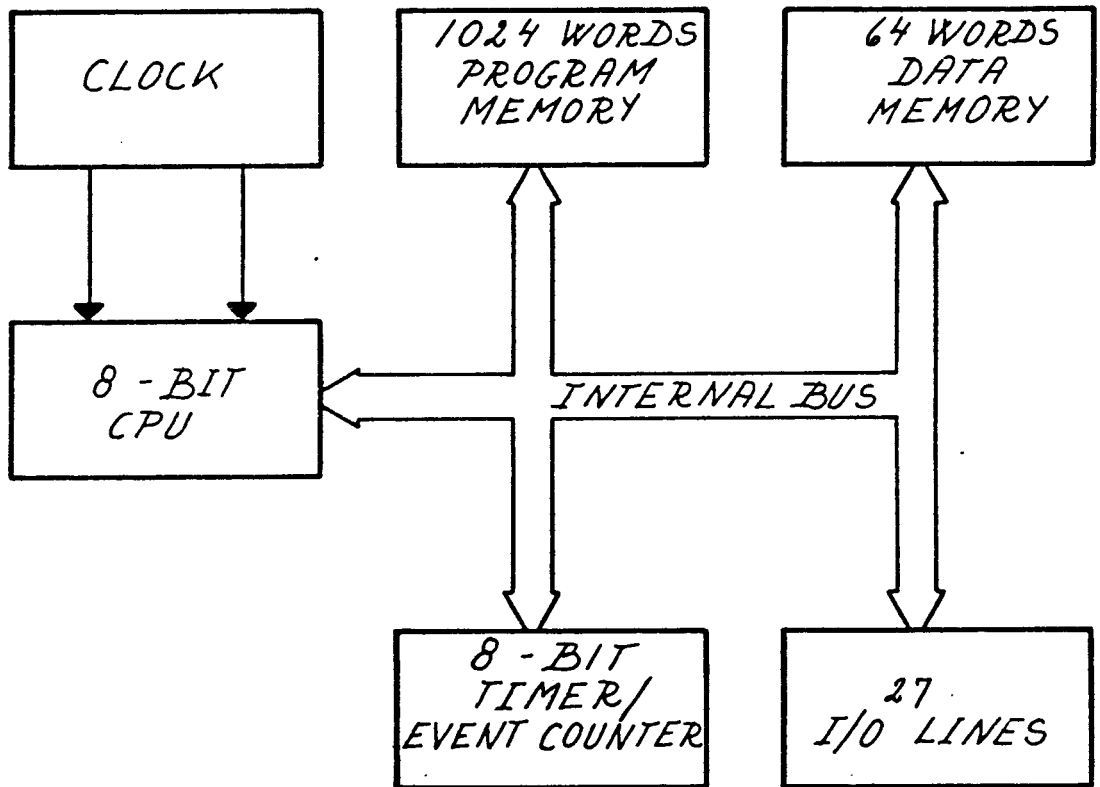
Fig. 1 BLOCK DIAGRAM KTC 401/KTC403.

R 21330

* Only in KTC 403

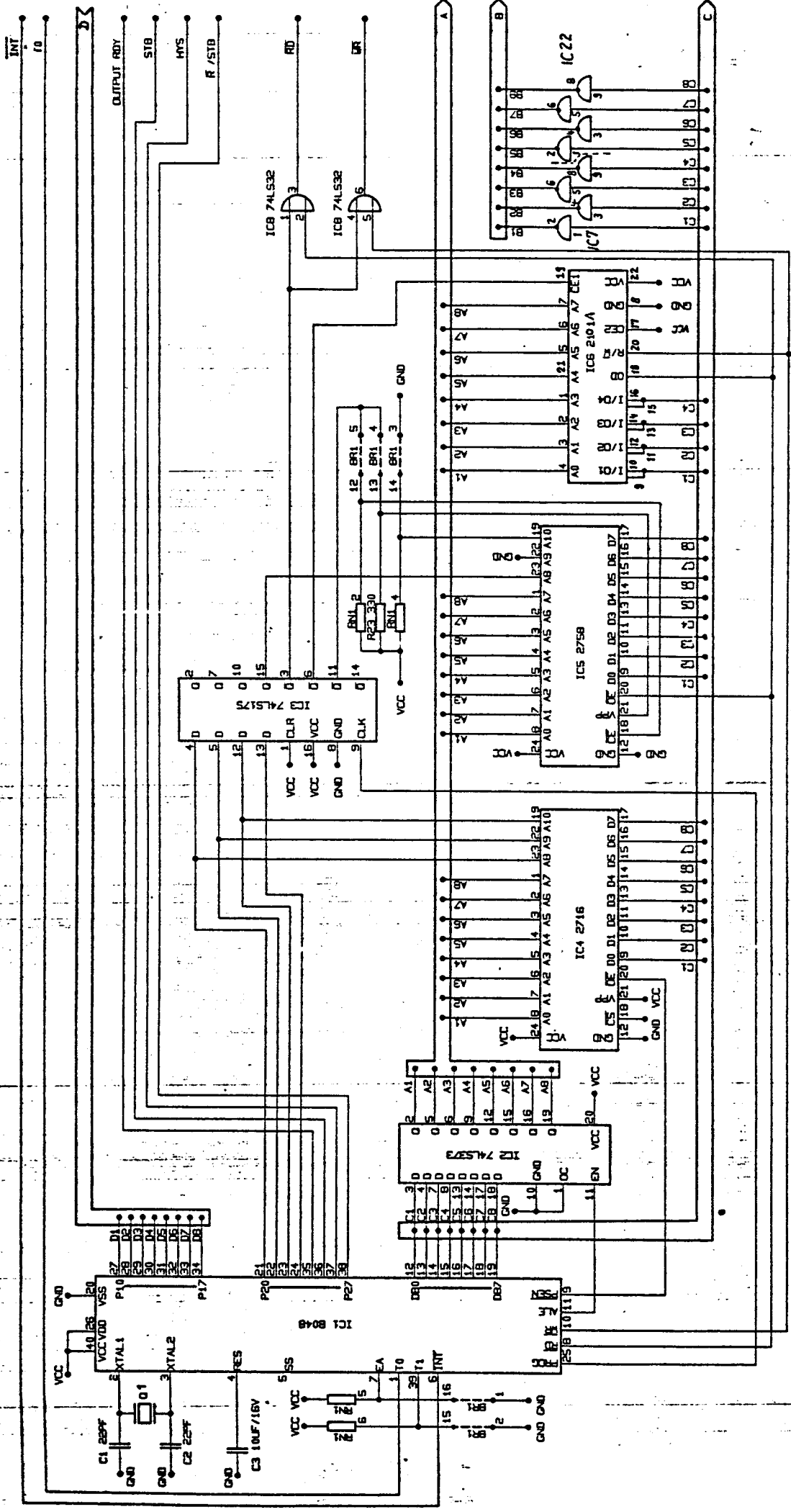
MCS - 48 MICROPROCESSORS

- I 8048 8-BIT microcomputer with ROM.
- I 8748 - - - - EPROM
- I 8035 - - - - ext. MEMOR



MVP 810202

Fig. 2. BLOCK DIAGRAM for CPU-8048.



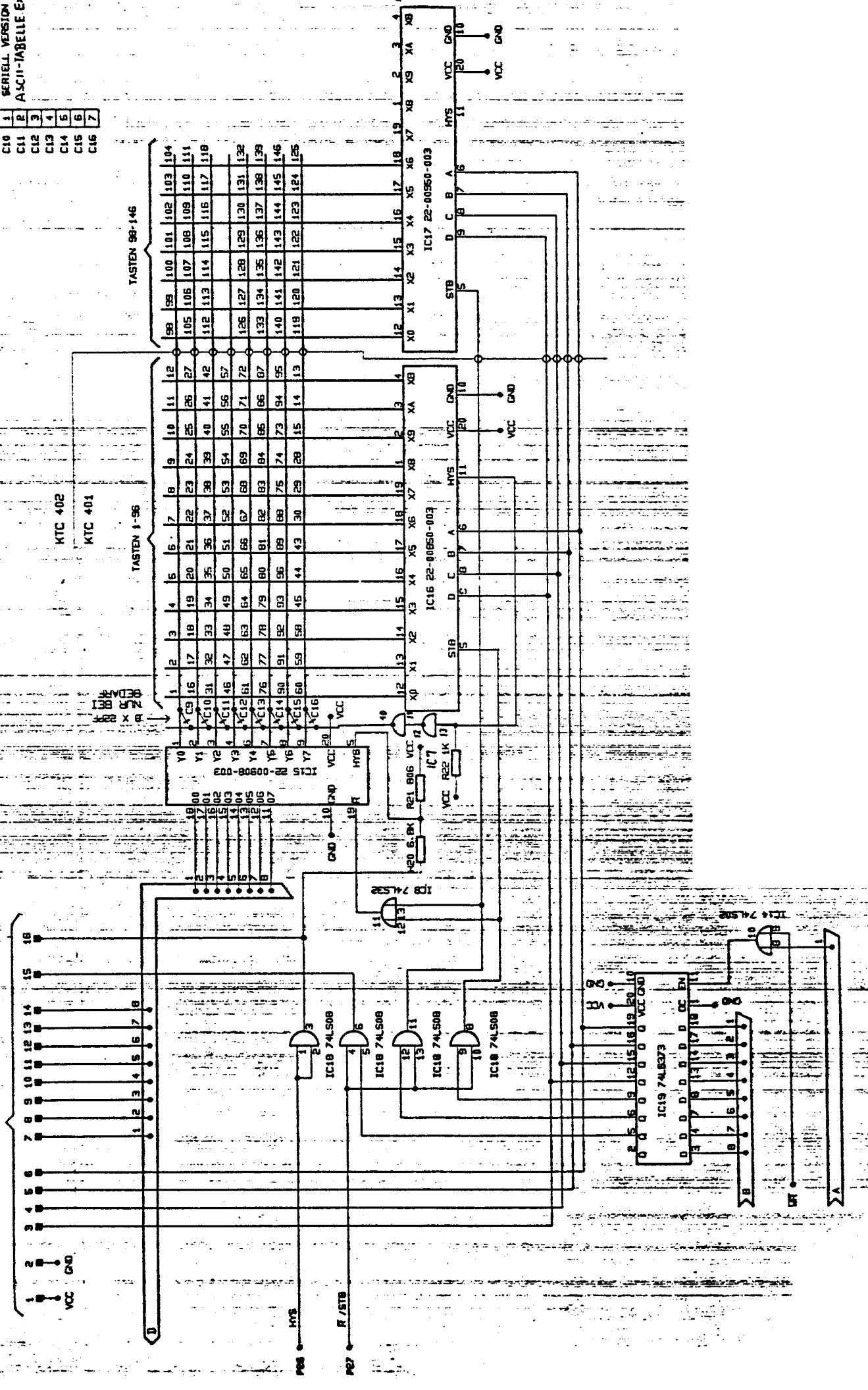
Connection BR 1 to 16 for 8048

- BR 3 to 14 } ASCII TABLE from ext 2758
- BR 5 to 12 }
- BR 4 to 13 } ASCII TABLE from ext 7641

18 POL. IC-FASSUNG (VERBINDLG ZUR TASTATURENWEITERUNG)

ASCII VERSION
SERIELL VERSION
ASCII-TABELLE EXT

C9	1
C10	2
C11	3
C12	4
C13	5
C14	6
C15	7
C16	7



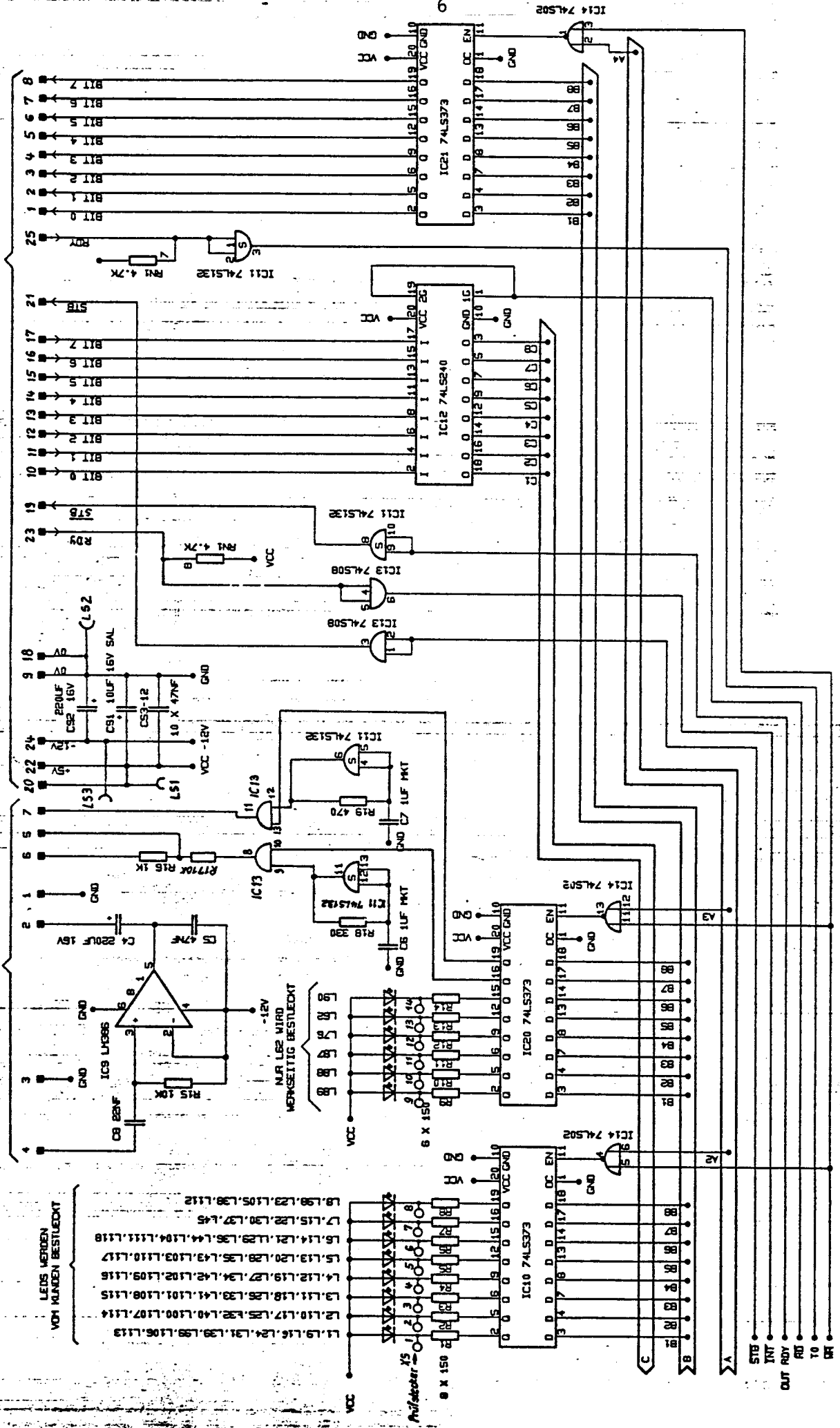
KTC 401/402 Circuit diagram page 2.

STECKER 2 (PARALLEL)

STECKER 3

LEIS WERDEN
VOM KUNDEN BESTELT

- 1. L1, L9, L16, L24, L31, L34, L39, L99, L106, L113
- 2. L10, L17, L21, L23, L28, L40, L100, L107, L114
- 3. L11, L18, L26, L33, L41, L101, L108, L115
- 4. L12, L19, L27, L34, L42, L102, L109, L116
- 5. L13, L20, L28, L36, L43, L103, L110, L117
- 6. L14, L21, L29, L36, L44, L104, L111, L118
- 7. L15, L22, L30, L37, L45
- 8. L18, L23, L35, L38, L112

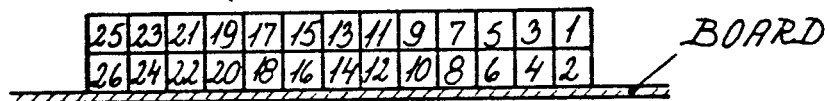


2. CABLE CBL923

2.

Fig. 3 shows the cable CBL923 which connects the keyboard to the computer, normally RC702. Power to the keyboard is supplied from the computer using CBL923.

CONNECTOR 1 TO KEYBOARD		CONNECTOR 2 TO COMPUTER	
PIN NO.	SIGN. NAME KEYBOARD	SIGN. NAME RC 702	PIN No.
1	OUT 0	KEY 0	22
2	OUT 1	KEY 1	23
3	OUT 2	KEY 2	24
4	OUT 3	KEY 3	21
5	OUT 4	KEY 4	17
6	OUT 5	KEY 5	18
7	OUT 6	KEY 6	19
8	OUT 7	KEY 7	20
21	\overline{STB}	KEY STROBE	12
9	0V	0V	13
18	0V	0V	3
22	+5V	+5V	25



25 POL CANNED
CONNECTOR

PIN LAY OUT FOR CONNECTION
TO KEYBOARD.

MVF 870602

Fig. 3. CABLE TO KEYBOARD CBL 923.

3. ALPHABET

3.

Fig. 4 shows the ASCII Alphabet supplied from the keyboard. Notice that 8 bits are used so it is an 'extended' ASCII alphabet which the keyboard supplies.

RC 721													RC 722																																
00	95	96	97	99	9C	9D	9E	9F	C0	E0	FD	FE	DD	DE	E5	E7	F4	E2	E3	F3	F8	80	81	82	83	84	86	87	88	8E	8F	90	91	92	93	94	E8	E9	EF	EB	E4	E3	D3	D8	
FF	8C	12	13	14	15	16	17	19	1C	1D	1E	1F	1A	1B	1C	1D	1E	1F	1A	1B	1C	1D	7F	0C	01	02	03	04	06	07	08	0E	0F	10	11	1A	0A	C8	C9	CF	CB	CC	C1	D2	
85	21	22	23	24	25	26	27	28	29	30	3D	7E	88	98	EA	EC	AA	F6	F0	F0	E6	AF	05	31	32	33	34	35	36	37	38	39	3F	5E	08	18	CA	CC	8A	D6	D0	C6	BF		
9B	09	51	57	45	52	54	59	55	49	50	50	50	2B	8D	ED	EE	85	A7	A8	A9	8D	1B	09	71	77	65	72	74	79	75	69	70	70	3B	0D	CD	CE	05	87	B8	B9	0D			
CTRL	ALPHA	41	53	44	46	47	48	4A	4B	4C	5B	5C	2A	8A	F1	F5	8D	A4	A5	A6	88	LOCK	61	73	64	66	67	68	68	6A	6B	6C	7B	7C	3A	0A	D1	D5	AD	B4	B5	B6	08		
SHIFT	60	5A	58	43	56	42	4E	4D	3C	3E	3F	SHIFT	FC	FC	F7	98	F9	A1	A2	A3	BC	SHIFT	40	7A	78	63	76	62	6E	6E	6D	7C	2E	2F	DC	D7	1B	D9	B1	B2	B3	AC			
SHIFT	LOCK	7F	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	LOCK	7F	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C	8C

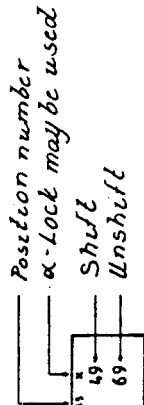


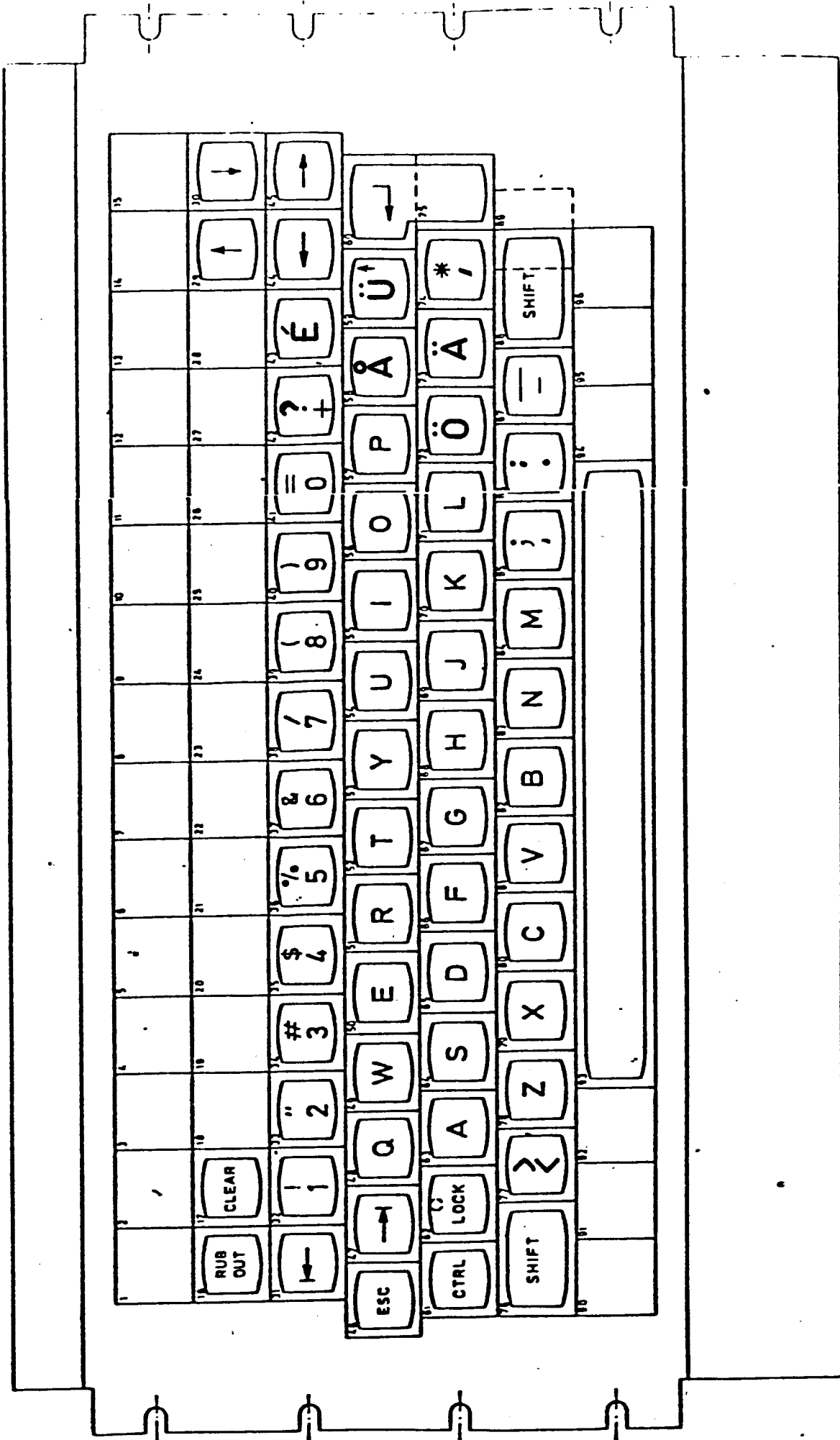
Fig 4 ASCII-CODE 0. PUT AND POSITION NUMBERS FROM RC 721 AND RC 722.

4. NATIONAL VERSIONS

4.

RC721 and RC722 may be supplied in a number of national versions. This is done only by changing a number of keytops. The rest of the change is done in the software in RC702. It is the same keytops which are changed in RC721 and RC722. Lay out of the following versions is shown:

- Fig. 5 shows RC721,001 keyboard Danish alphabet.
- Fig. 6 shows RC721,002 keyboard Swedish alphabet.
- Fig. 7 shows RC721,003 keyboard USA ASCII alphabet.
- Fig. 8 shows RC721,004 keyboard German alphabet.
- Fig. 9 shows RC721,005 keyboard UK ASCII alphabet.
- fig. 10 shows RC722,001 keyboard Danish alphabet.
- Fig. 11 shows RC722,006 keyboard Bibliotek alphabet.



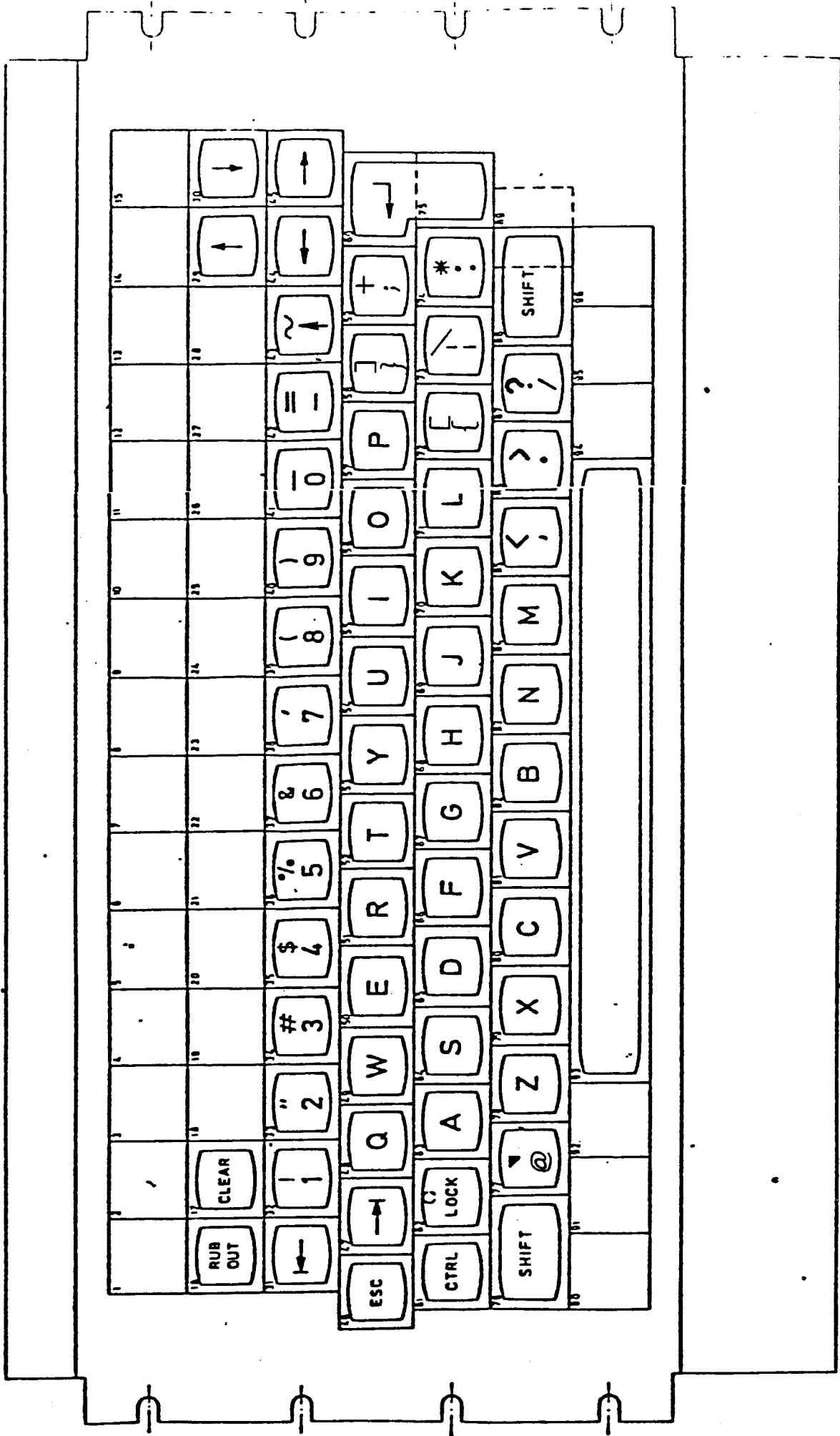
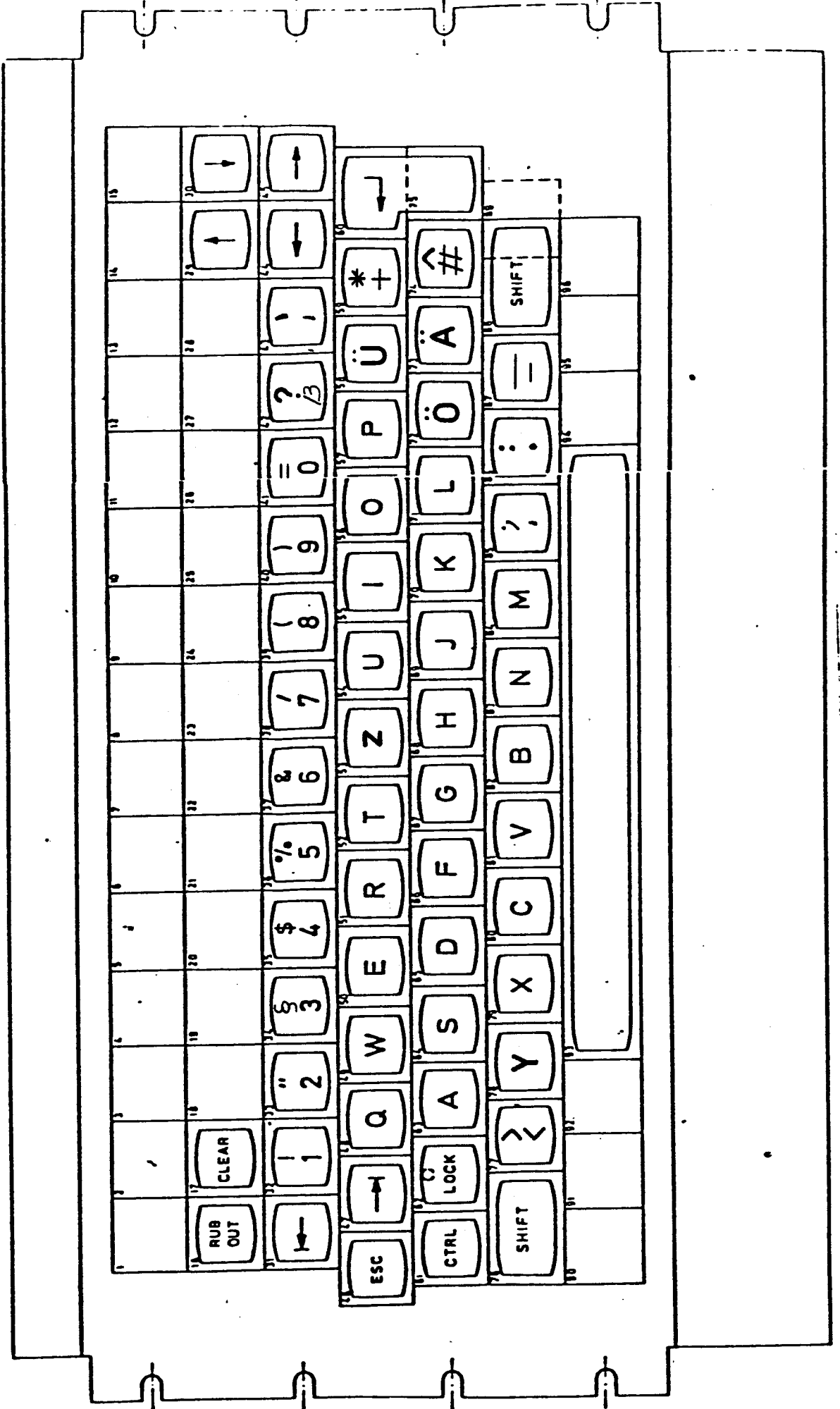


Fig. 7. LAY OUT RC 721, 003 US ASCII



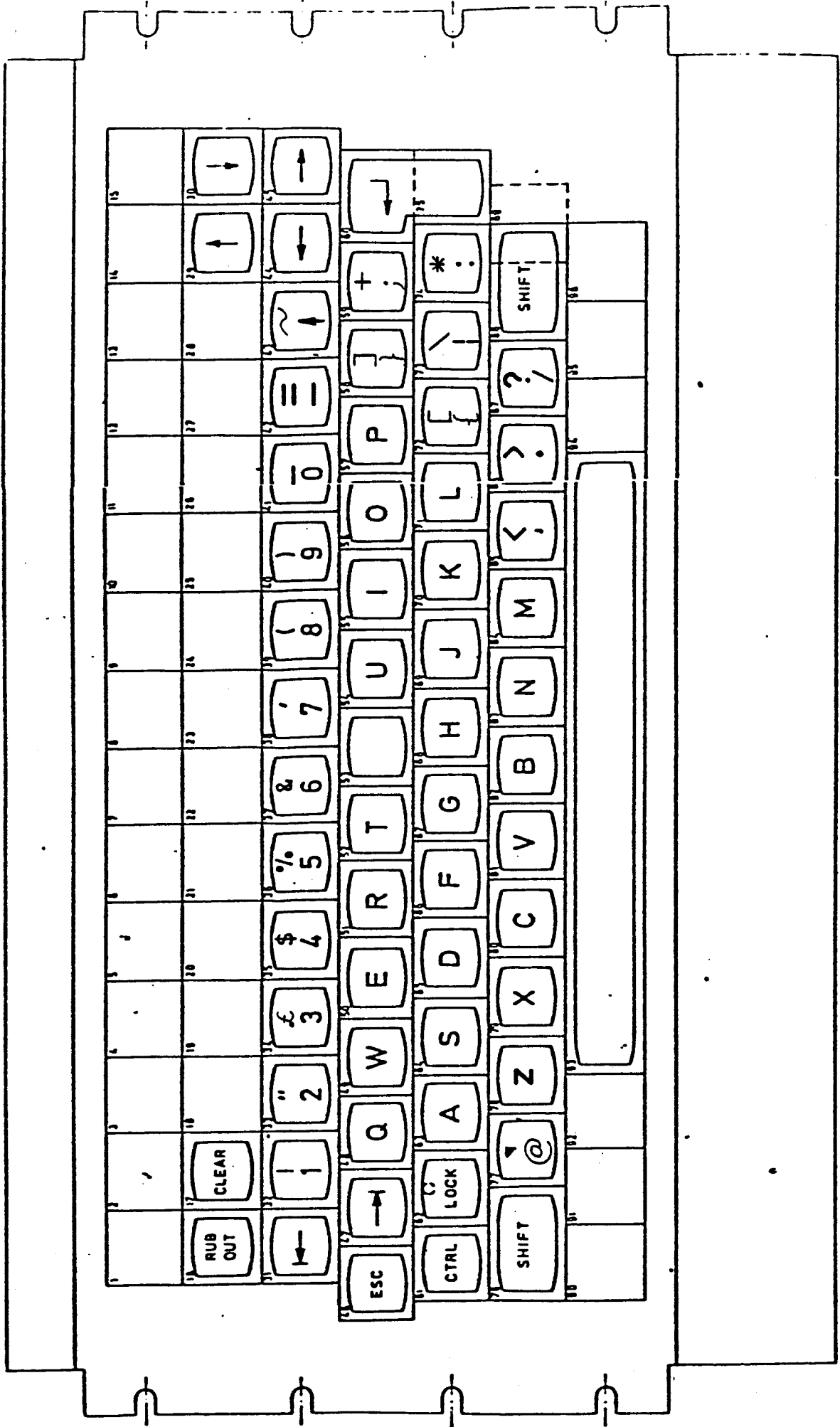


Fig. 9. LAY OUT RC 721, 005 UK ASCII

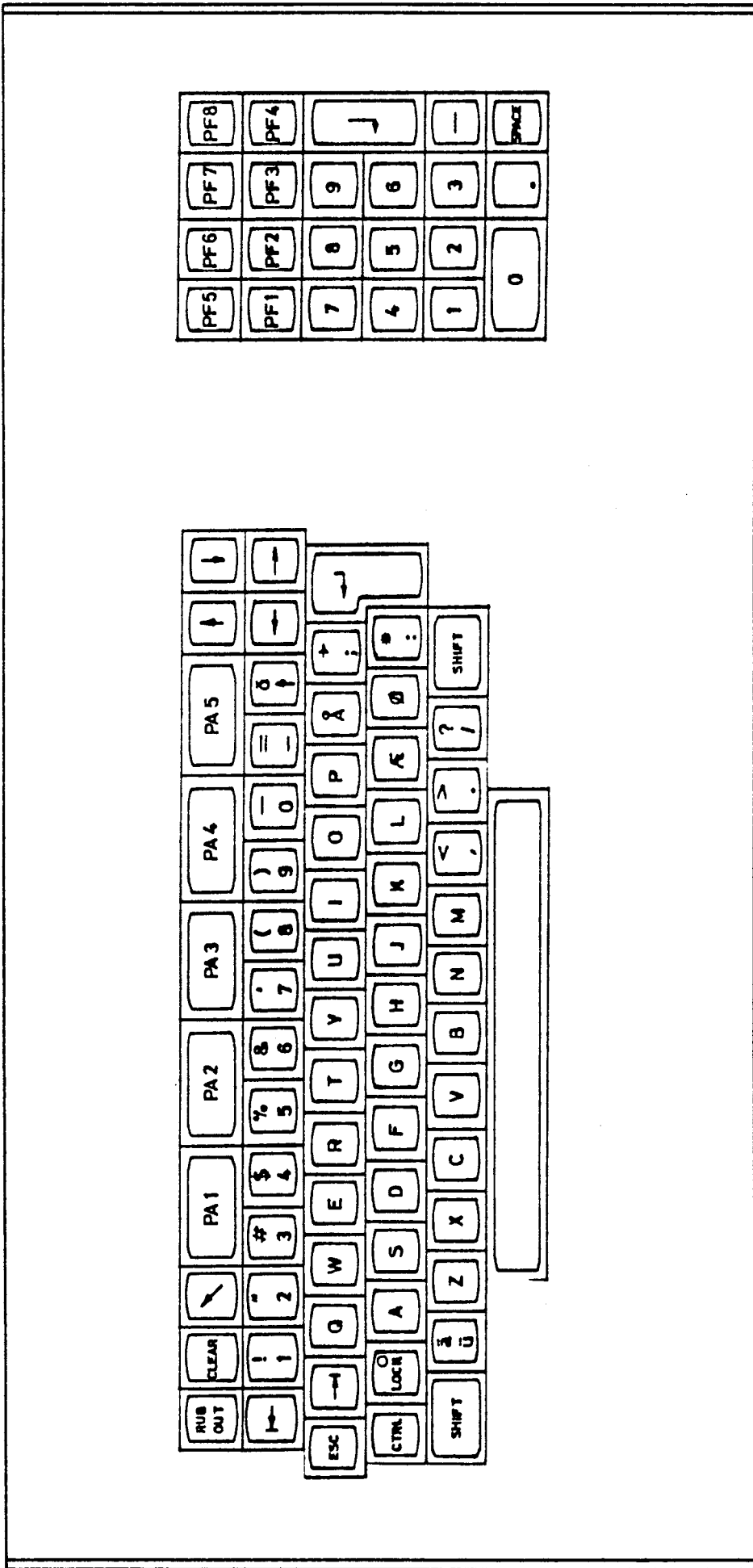


Fig 10 LAY OUT RC 722, 001 DANISH

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Technical Manual

RCSL No.: 44-RT1980

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WARRANTY	<input type="checkbox"/>	NON WARRANTY	<input checked="" type="checkbox"/>

PAGE	1	OF	3
RE: ECN NO:			

SERIAL EFFECTIVITY KBU 723/051 and upwards KBU 722/384 and upwards KBU 721 not implemented	EQUIPMENT AFFECTED RC700 RC721, RC722/KBU 723, KBU 722, KBU 721 Keyboard
NOTE	

REASON FOR CHANGE

The output from the keyboard is changed to be unique, in order to execute the future software.

DESCRIPTION OF CHANGE

If the keyboard is RC721 (short), refer to page 2
If the keyboard is RC722 (long) , refer to page 3

1. Insert two straps
2. Insert one capacitor
3. Insert ROA 434
4. Code the FCO label 19-007

ADDITIONAL COMMENTS

FCO 19-006 must be executed before this change

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK
UNDER RC-PARTNUMBER: 8-0907
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE	YES <input type="checkbox"/>	NO <input checked="" type="checkbox"/>
---------------------	------------------------------	--

DOCUMENTATION ENCLOSED

None

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
1	EPROM ROA 434	
1	22 pF capacitor	8-02-015
5 cm	Wrap wire	

ESTIMATED INSTALLATION TIME: 0,5 h

PROJECT ENGINEER	DEVELOPMENT MANAGER	SYS. PRODUCTION MANAGER	TECH. SERVICE MANAGER
SIGN.	SIGN.	SIGN.	SIGN.
MV Pedersen	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
DATE 21/9 81	DATE 21/9 81	DATE 23/9 81	DATE 22/9 81

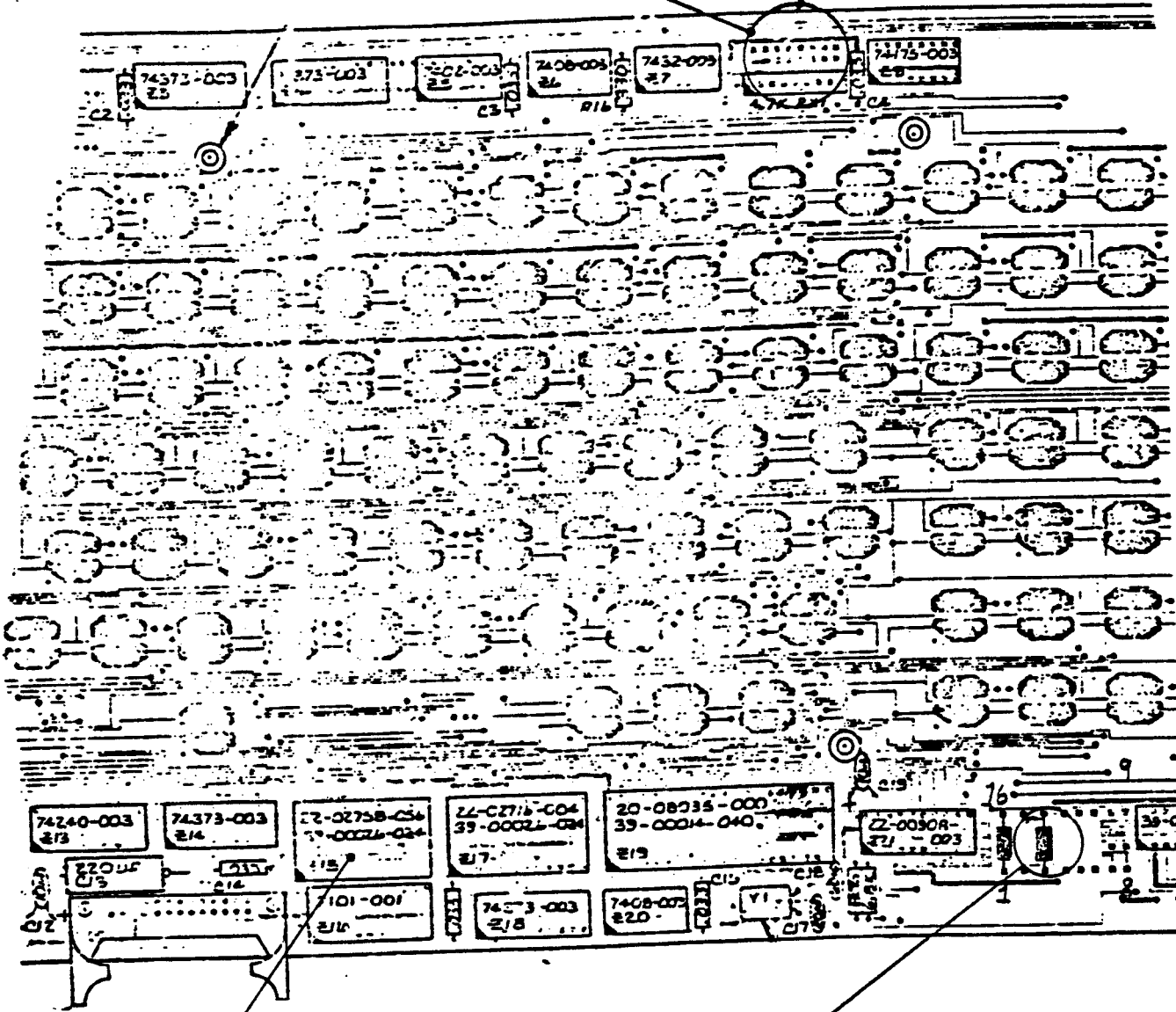
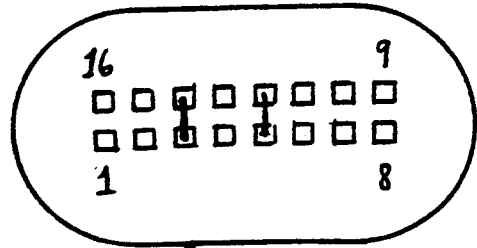


FIELD CHANGE ORDER

NO. 19-007

PAGE 3 OF 3

Connect pin 3 to 14
and pin 5 to 12
as shown.



Insert ROA 434
in empty socket

Insert 22PF pin 3
to pin 14

DATE



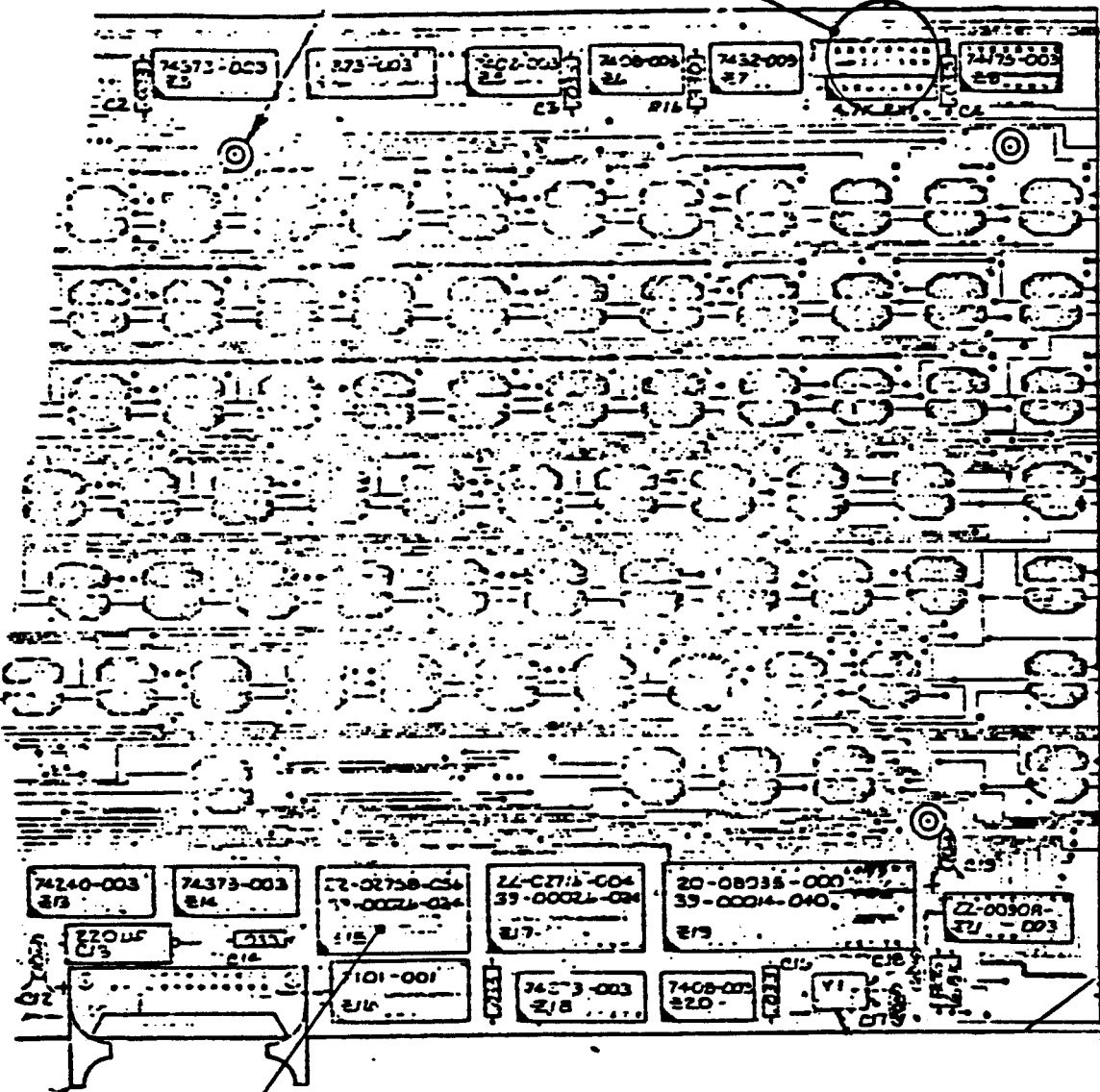
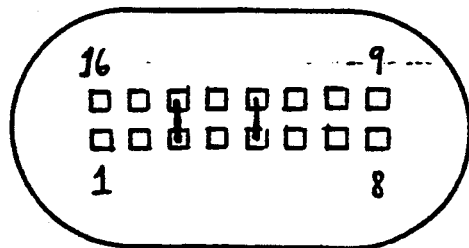
FIELD CHANGE ORDER

NO. 19-007

PAGE 2 OF 3

PRINT TOP VIEW

Connect pin 3 to 14
and pin 5 to 12
as shown.



Insert
22 pF
under
metal
cover
as-
shown

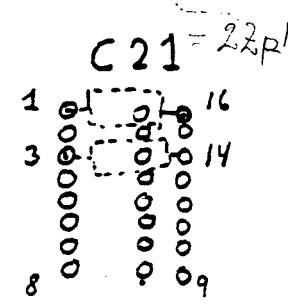
Insert ROA 434
in empty socket

Modification RC 721

BOTTOM
VIEW

Pin 1-16
already
installed

Pin 3-14
new
capacitor



RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input checked="" type="checkbox"/>	NON WARRANTY	<input type="checkbox"/>

PAGE	1	OF	2
RE: ECN NO:			

SERIAL EFFECTIVITY

All keyboards produced after september th 1st 1981

EQUIPMENT AFFECTED

Key-tronic keyboards

RC721, RC722, RC801, RC802, RC803, RC805 keyboards.

NOTE

REASON FOR CHANGE

The sockets for the CPU, the program ROM and the external ASCII ROM has too low contact pressure and too poor contact surface.
 The keyboard may fail after an interval of 1 to 12 months. The manufacturer of the sockets is "SCANBE",

The error sympton is keyboard in deadlock, normally with "LOCK" led lit

DESCRIPTION OF CHANGE

1. Change the 3 sockets to those supplied with the FCO-Kit. See next page.
2. Change the program PROM to a KTC-013. The old PROM must be returned.
3. Code the FCO-label: 19-006.

ADDITIONAL COMMENTS

The eprom must be returned for reprogramming

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: 8-0906
 ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE	YES <input checked="" type="checkbox"/>	NO <input type="checkbox"/>
---------------------	---	-----------------------------

THE FCO-KIT INCLUDES:

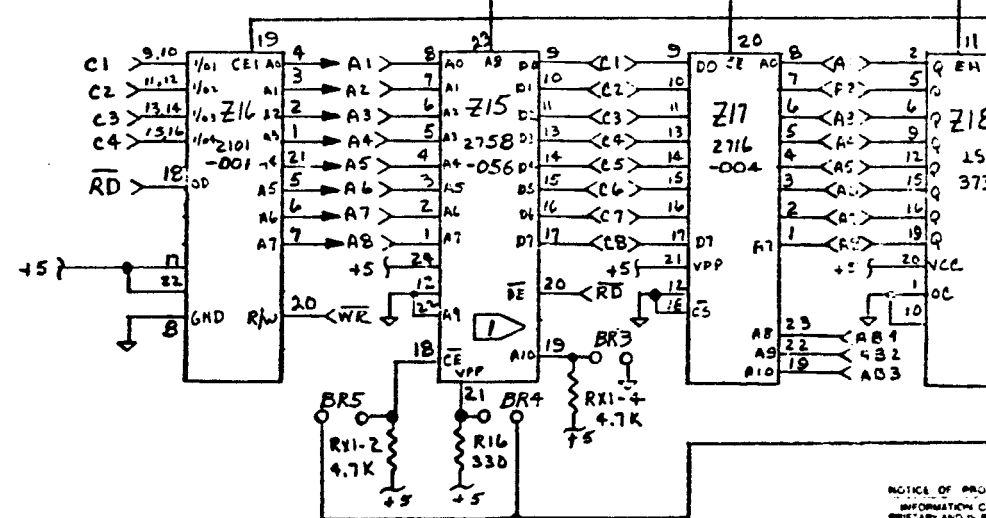
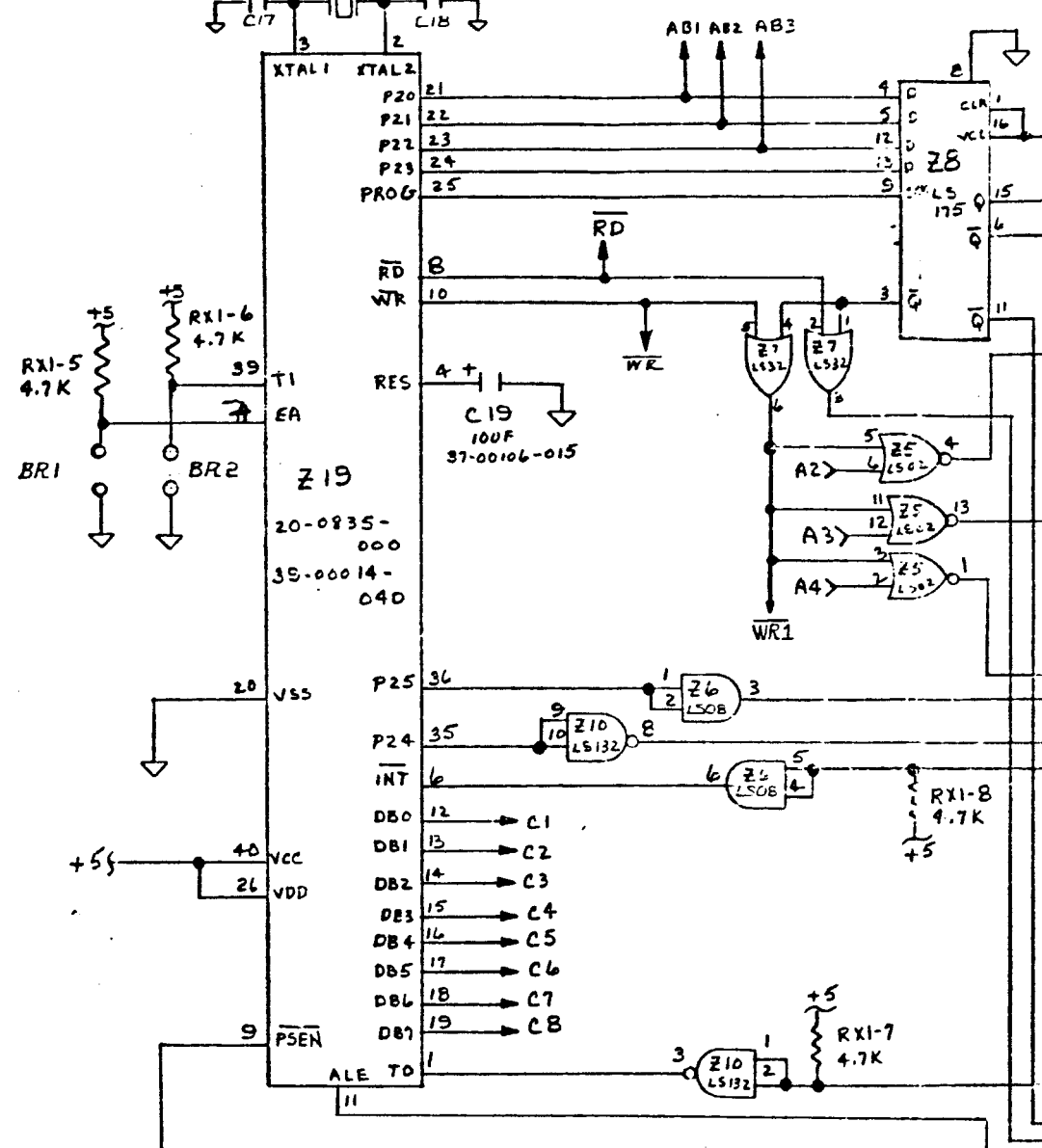
QTY	DESCRIPTION	RC P/N
1	40 pin socket	4-9818
2	24 pin socket	6-0005
1	2716 EPROM type KTC-013	

DOCUMENTATION ENCLOSED

ESTIMATED INSTALLATION TIME: 0,5 h

PROJECT ENGINEER	DEVELOPMENT MANAGER	SYS. PRODUCTION MANAGER	TECH. SERVICE MANAGER
SIGN.	SIGN.	SIGN.	SIGN.
<i>M. Tolboe</i>	<i>[Signature]</i>	<i>[Signature]</i>	<i>[Signature]</i>
DATE: 27/8 81	DATE: 27-81	DATE: 19-81	DATE: 23/8

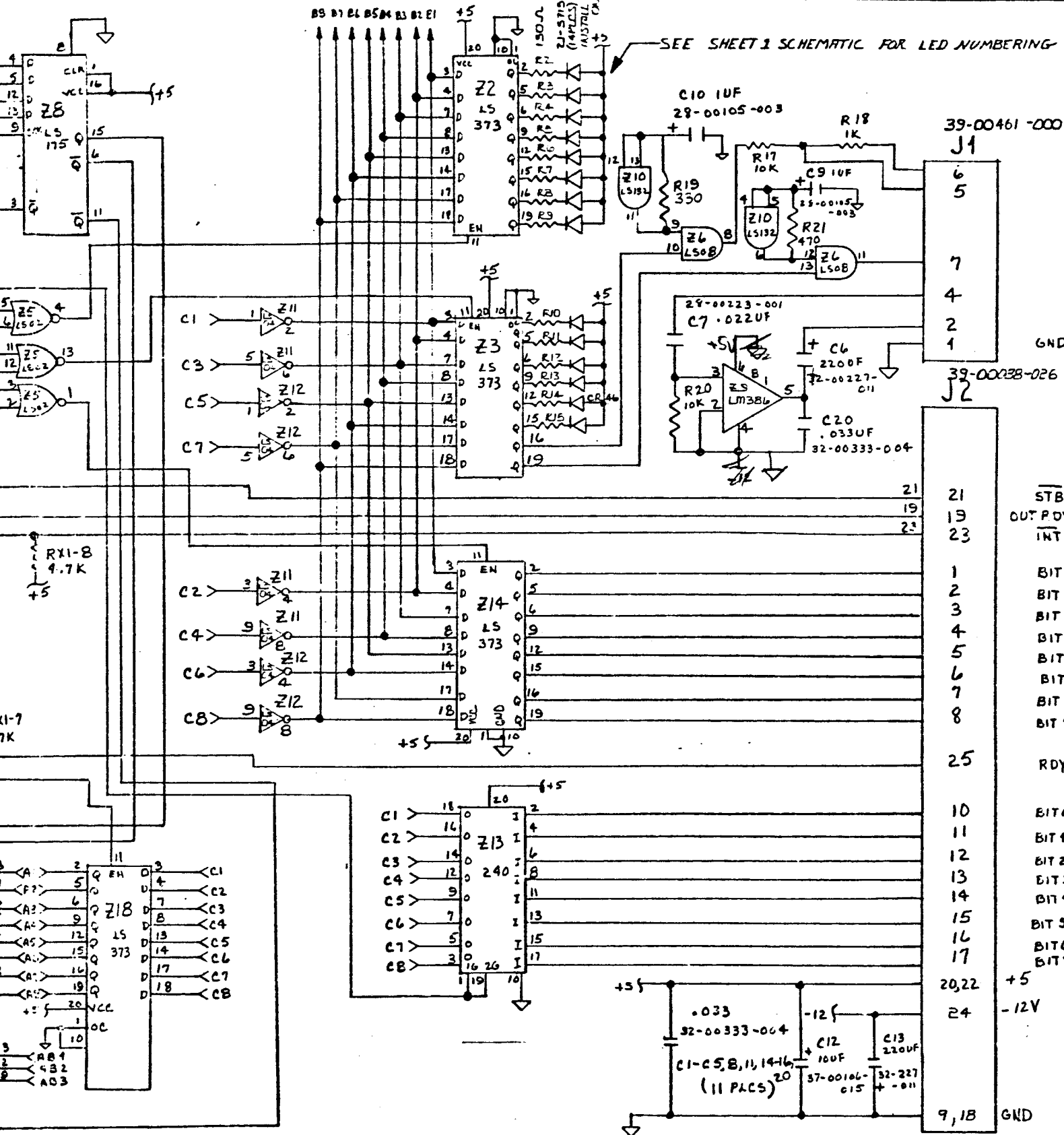
Y1 25-00001-004
20 DF (2PL05)



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EFF.	RLV	ECO	BY	DESCRIPTION	APP.
	~	~	HB	PRTO	JAH
	A	-	KL	MFG RELEASE	JAH



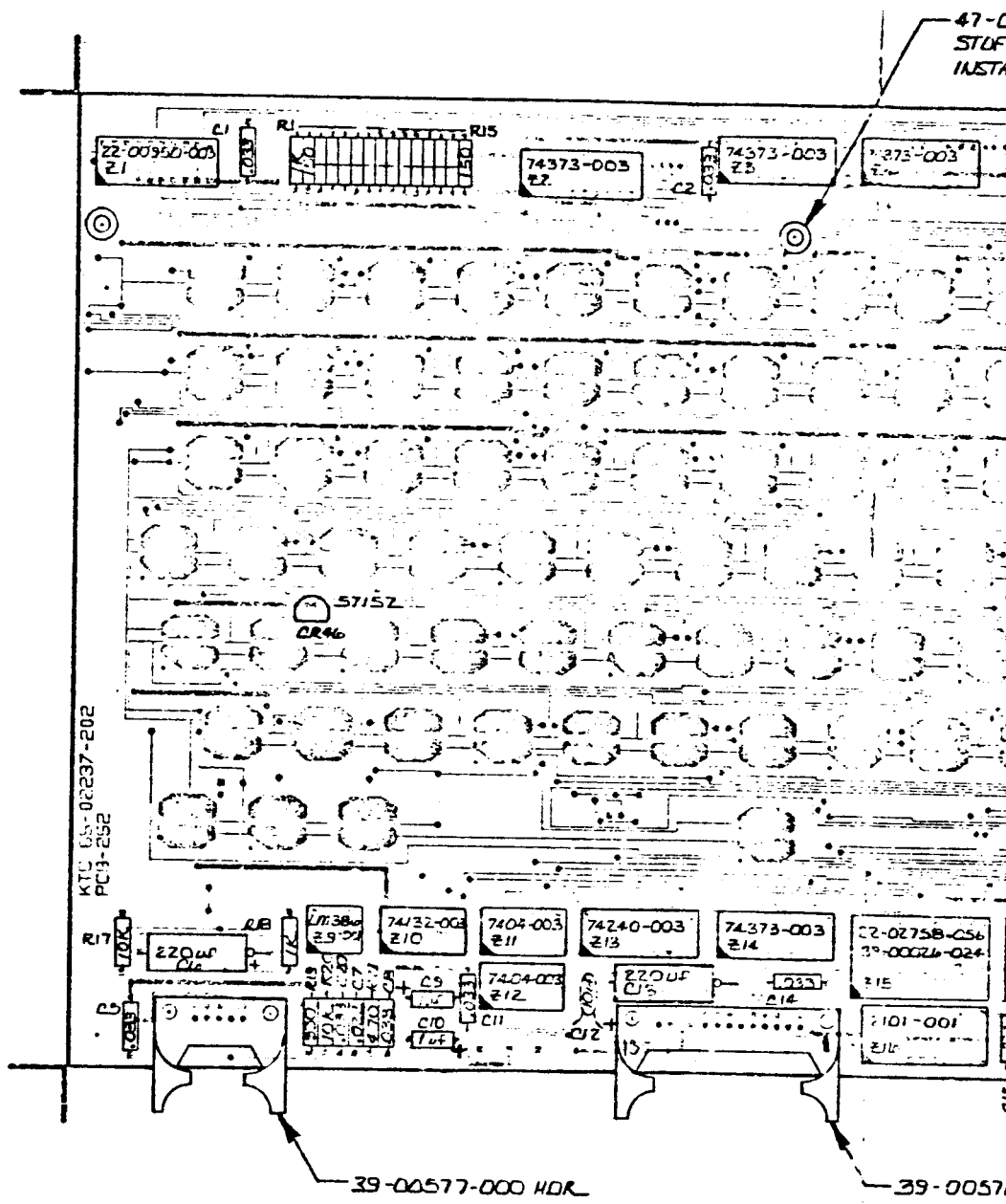
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MANUFACTURE PARTS
 AND/OR ASSY'S PER
 K.T.C. DOCUMENT:

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES	
XXX USED ON	DIMENSION NOT TO SCALE
RELEASED	
APP. JCL	11/3/6
CH.	
DR. BB	10/12/6

TOL. EXCEPT AS NOTED	ITEM	PART NO.	DESCRIPTION
MOLE DIA. FRACT. ± 1/64" XX ± .01" XXX ± .005" ANG. ± 1°	SCALE	TITLE	
		key tronic corporation	DWG. NO. 35-02237
		SPOKANE, WASH., U.S.A.	SHEET 2 OF 2

47-0
STOF
INSTA

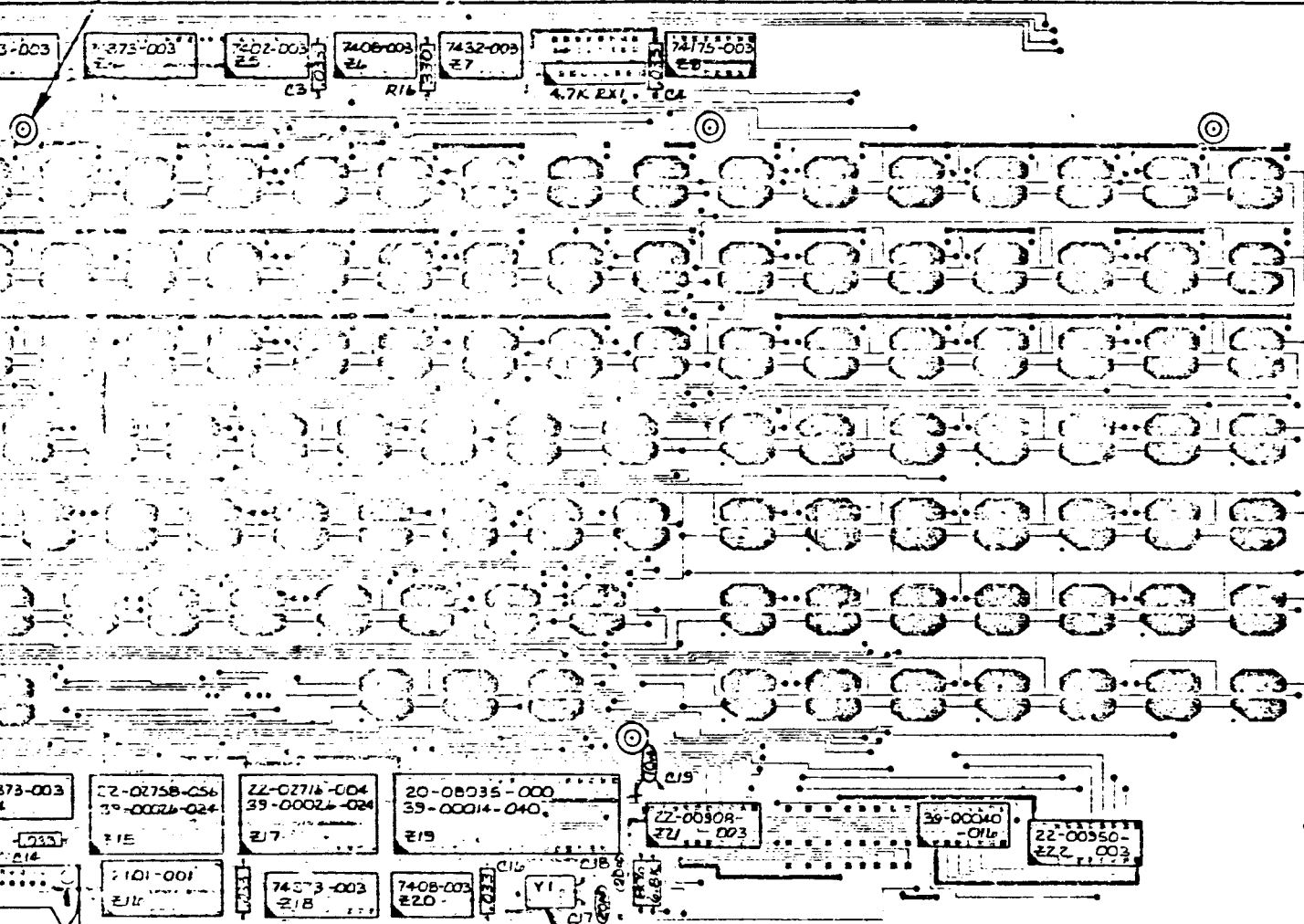


2
3
4

NOTES:

A B

47-00181-000
STDF (5PLCS)
INSTALL COMP SIDE OF PCB

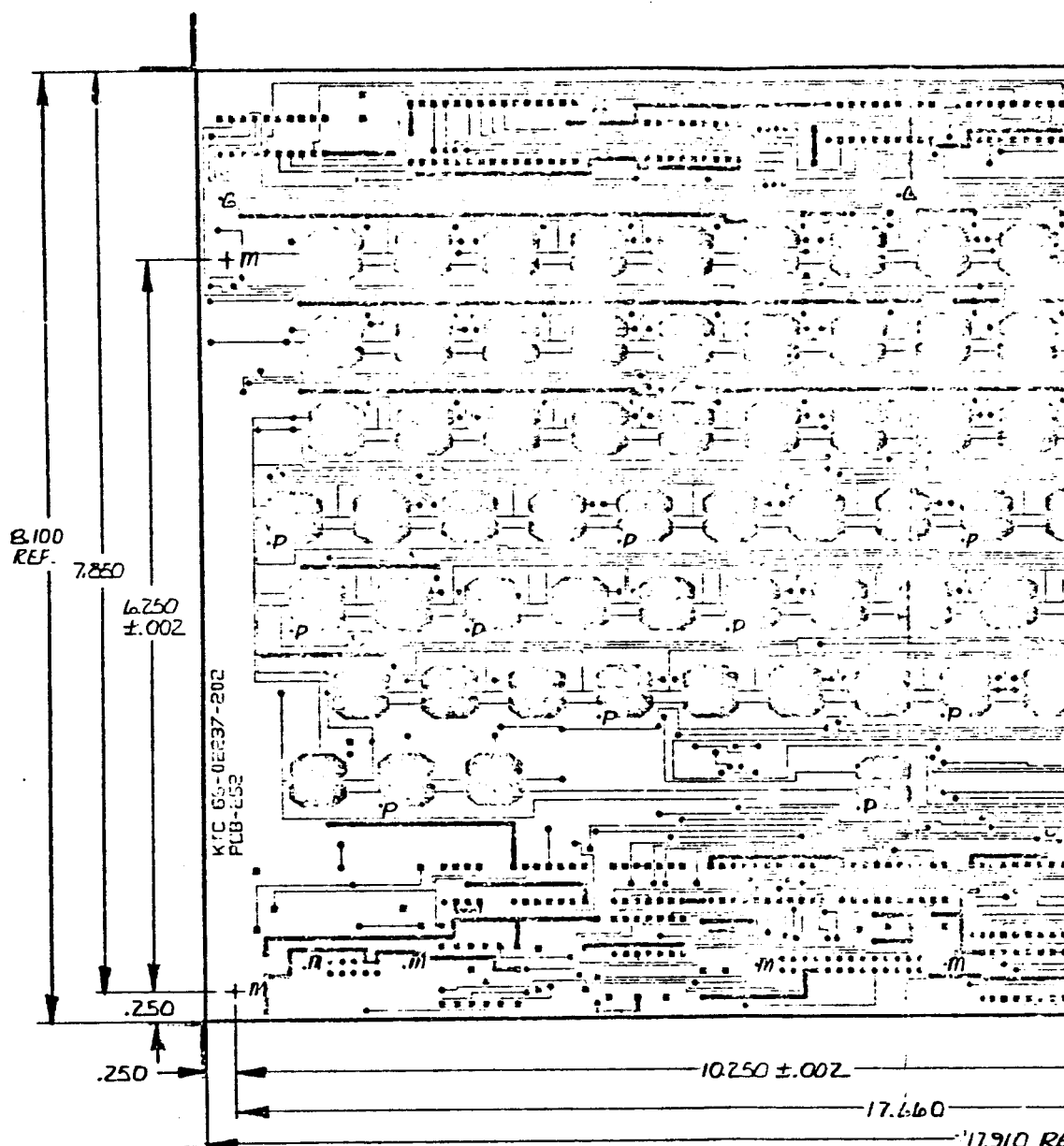


39-00576-000 HDR

48-00300-006 XTAL
INSULATE WITH
48-00312-005 TAPE
DO NOT FLOW SOLDER OR DEGREASE

-002, -052 ASSY

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES		TOL EXCEPT AS NOTED	ITEM	PART NO	DESCRIPTION
MANUFACTURE PARTS AND OR ASSY S PER P.T.C DOCUMENT	XXX DIMENSION NOT TO SCALE	HOLE D/A FRACT = 1/64" AX = 01 YX = 005 ANG = 1°	SCALE	TITLE	KEYBOARD ASSY. (ELECT. ASSY)
M006 M007	USED ON RELEASED REBUCEENTR-122 APR 1975 CH DR INT 10-28-80			key tronic corporation	DWG NO 65-0223 SHEET 5 OF
				SPRINGFIELD, WASH., U.S.A.	



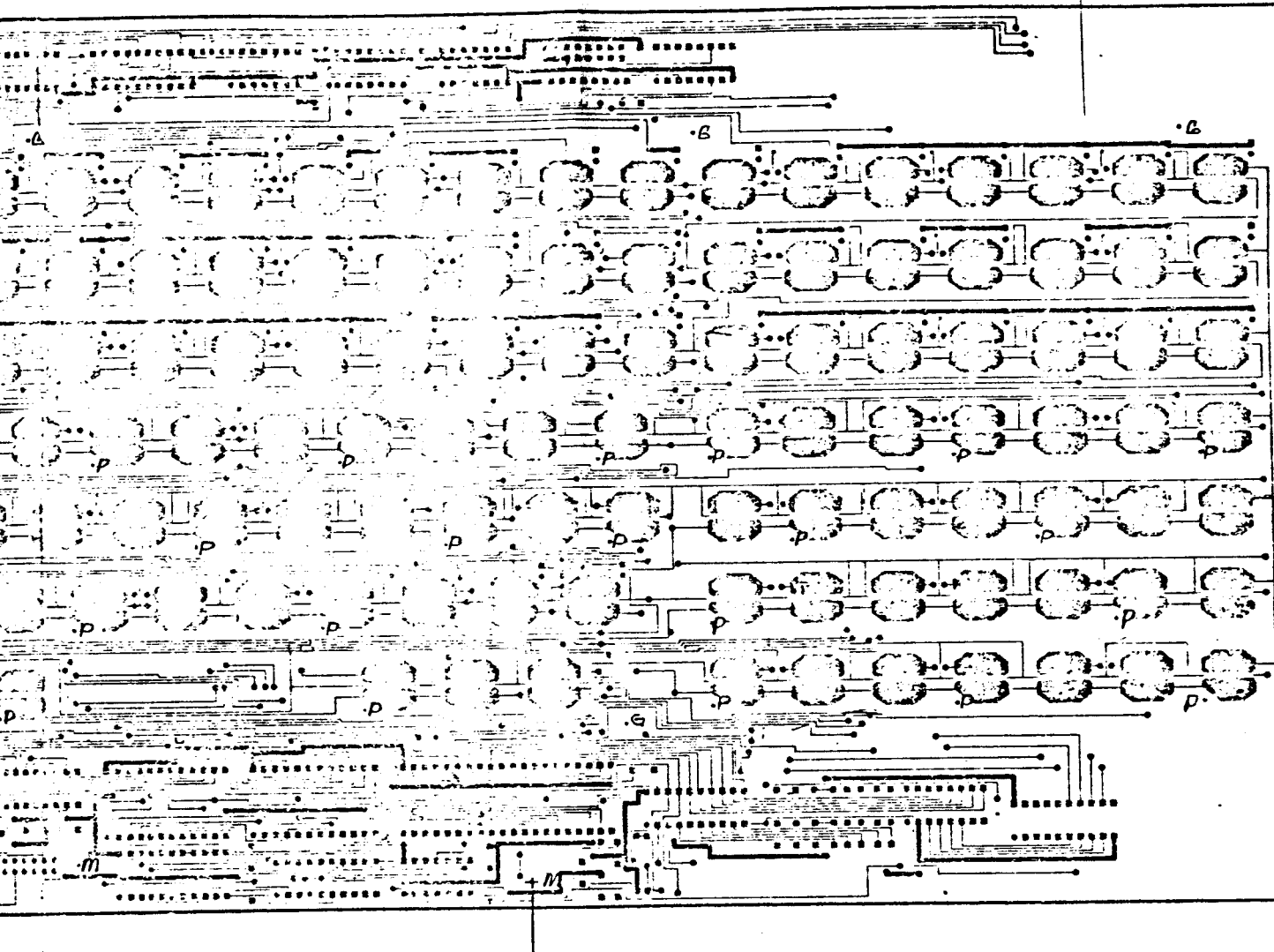
HOLE SIZE AFTER PLATING	CODE
.037	UN-MARKED
.042 ± .002	A
.062	B
.089	C
.127	D
.153	E
.187	F
.191 ± .002	G
.201	H
.234	J
.250	K
.175	L
.129	U
.122	N
.129	P
.150	R
	S
126 HOLE	T
	U
	V

2.

5. APPLY APPROPRIATE DASH NUMBER AFTER KTC PART NUMBER; PER MFR.
4. SOLDER MASK CKT SIDE OF PCB USING 65-12237-XXX
3. BREAK ALL SHARP EDGES.
2. PLATE THROUGH ALL UNMARKED, HOLES
1. USE 10Z. DOUBLE-CLAD G10-FR4 (1/16") THK. FABRICATE USING KTC UL APPROVED PROCESS "A".

NOTES:

EFF	REV	ECO	BY	DESCRIPTION	APP	DATE
N	N	N	WJM	PRSTO REL	NCK	10/24/80



-17.660
-17.910 REF

- 252 PCB
- 202 PCB
(COMPONENT SIDE)

PART NUMBER ;
XXX

.261	A
.250	
.201	MIP
.085	UNMARKED
SOLDER MASK HOLE CODE	

ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED EXCEPT WHERE SHOWN OTHERWISE

MANUFACTURE PART AND OR ASSY'S PER KTC DOCUMENT MO15	UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES		TOL EXCEPT AS NOTED HOLE .003" G.A. FRACT = 1/64 XX = .03 XXX = .015 ANG ± 1°	ITEM	PART NO.	DESCRIPTION	GT
	XXX DIMENSION NOT TO SCALE	SCALE		NONE	TITLE	KEYBOARD ASSY. (PCB HOLE CODE)	
USED ON	RELEASED	AP NCK 10/29/80	DR NCK 10/24/80	keytronic corporation SPOKANE, WASH. U.S.A.		DR NO 65-02237	CHEET 4 OF

A

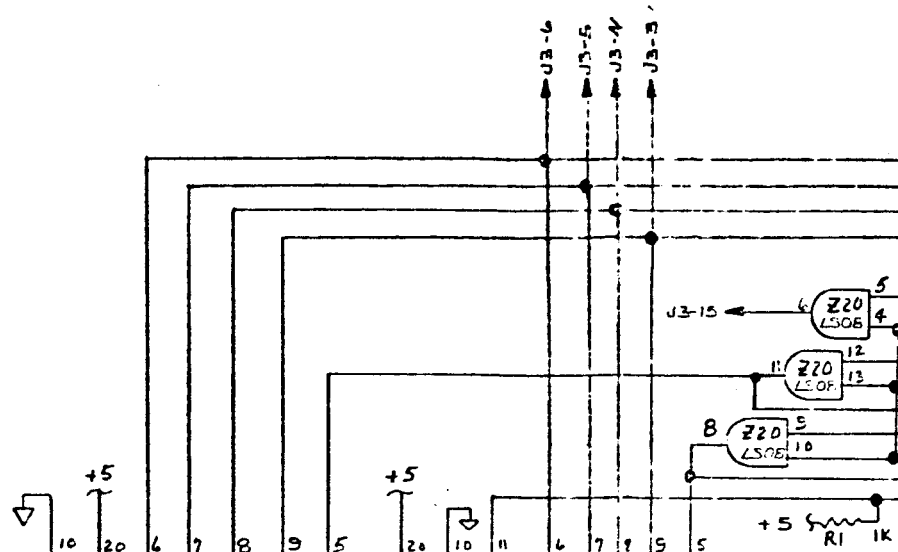
B

1

2

3

4



Z22
22-00950-003

	A	B	C	D	STB	
X4	X5	X4	X3	X2	X1	X0
118	117	116	115	114	113	112
125	124	123	122	121	120	119
146	145	144	143	142	141	140
135	138	137	136	135	134	133
132	131	130	129	128	127	126
119	117	116	115	114	113	112
111	110	109	108	107	106	105
104	103	102	101	100	99	98

Z1
22-00950-003

	A	B	C	D	STB						
YB	XA	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
4	3	2	1	19	18	17	16	15	14	13	
13	14	15	26	29	30	43	44	45	58	59	
95	94	73	74	75	83	83	56	93	92	91	
87	86	85	84	83	82	81	80	79	78	77	
72	71	70	69	68	67	66	65	64	63	62	
57	56	55	54	53	52	51	50	49	48	47	
42	41	40	39	38	37	36	35	34	33	32	
27	26	25	24	23	22	21	20	19	18	17	
12	11	10	9	8	7	6	5	4	3	2	

28-00220-0

+5V
R1
B

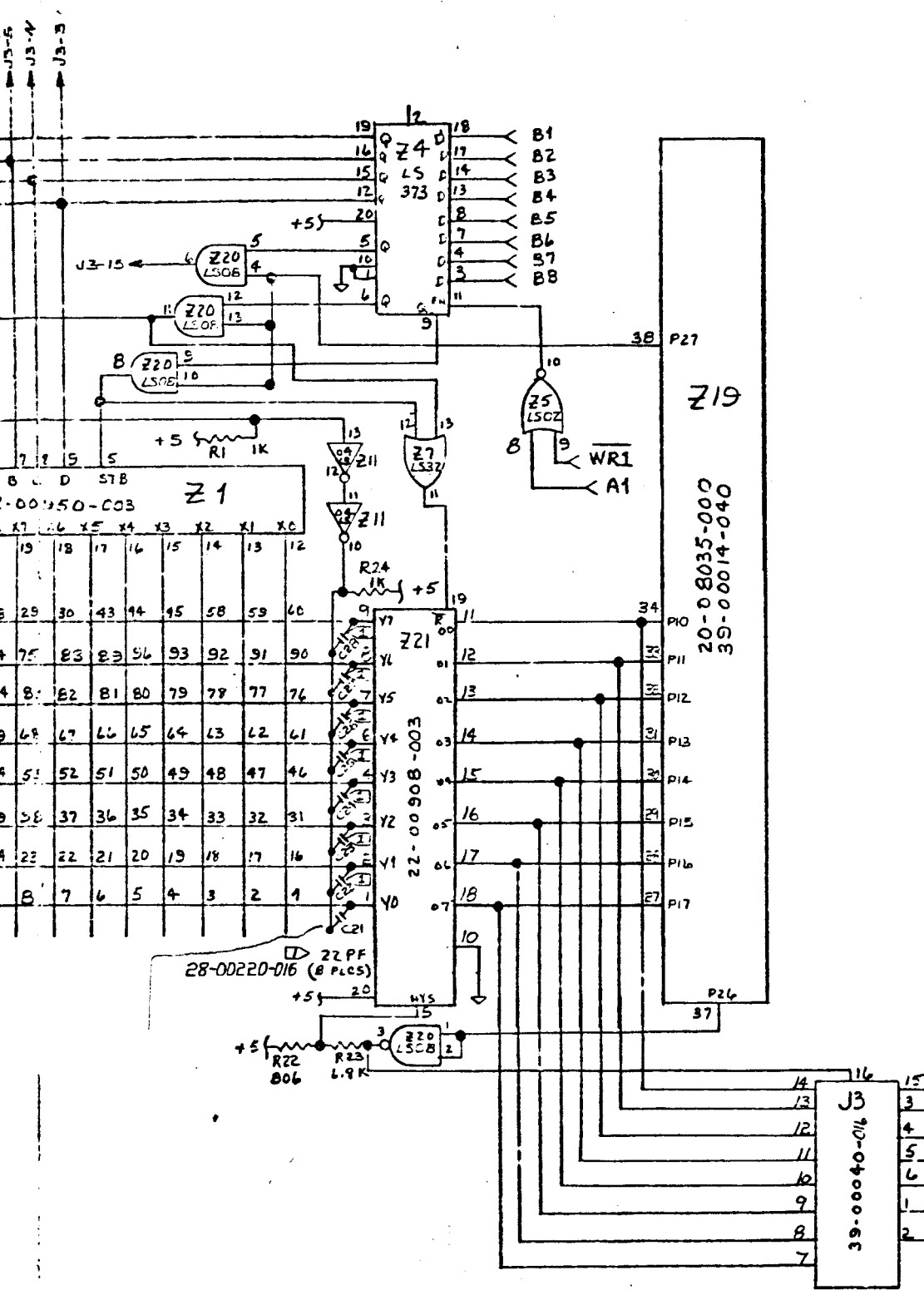
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A

B

EFF.	REV.	ECO	BY	DESCRIPTION	APP.
~	~	~	BB	PROTO	JR
~	A	~	RL	MFG RELEASE	JR



LED NUMBERING TABLE

RESISTOR	RX	FEEDS	LEDS	CRX
R2	1, 9, 16, 24, 31, 39			
R3	2, 10, 17, 25, 32, 40			
R4	3, 11, 18, 26, 33, 41			
R5	4, 12, 19, 27, 34, 42			
R6	5, 13, 20, 28, 35, 43			
R7	6, 14, 21, 29, 36, 44			
R8	7, 15, 22, 30, 37, 45			
R9	8, 23, 38			

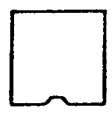
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 AND/OR ASSY'S PER
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XXX	DIMENSION NOT TO SCALE	MOLE DIA.
USED ON	RELEASED	FRACT. = 1/64"
REC: AUCENTRALITY	APP: NCA 11/2/75	XX = .01"
	CH: JRM 11-2-0	XXX = .005"
	DR: BB 10/24/75	ANG = 1°

ITEM	PART NO.	DESCRIPTION
SCALE	TITLE	SCHMATIC
keytronic corporation		DWG. NO. 35-02237
SPOKANE, WASH., U.S.A.		SHEET 1 OF 2

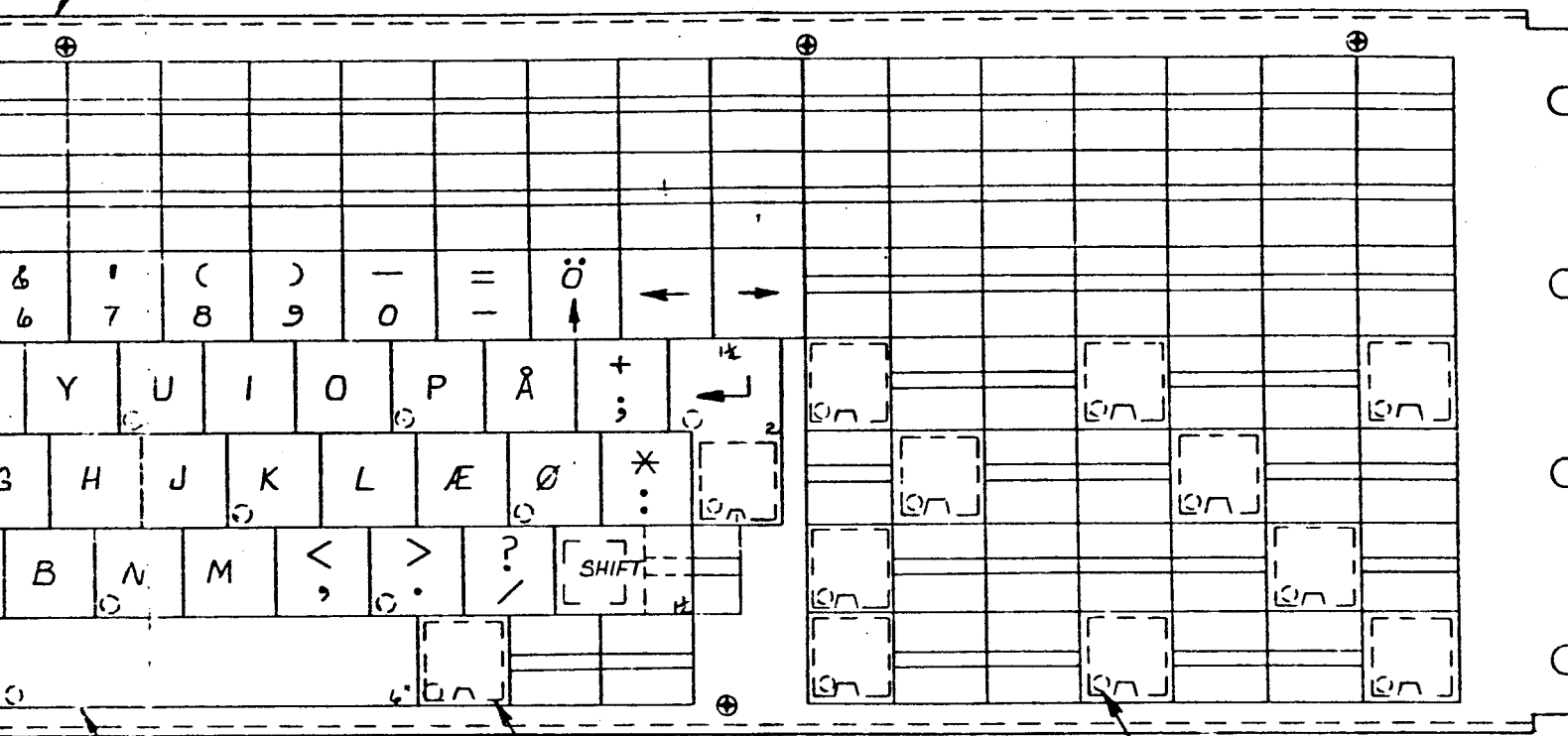
REV.	ECO	BY	DESCRIPTION
N	N	WJM	PROTO REL



61-04001-001 SWI (57PLCS)
45-00021-020 SPRNG (57PLCS)

SWI ORIENTATION
(57PLCS)

49-00977-000
MTB. PCT.



44-00104-001 BAR
44-00103-000 LEG (2PLCS)
44-00102-000 MNT (2PLCS)
CACA-12P1-1090-2601

44-00083-000
PNL. PLG (3PLCS)

47-00192-000
SCRNI (27PLCS)

-002 ,052 ASSY

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DATE 10-28-80 BY 1028/SP/STP

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AND/OR ASSY'S PER
K.T.C. DOCUMENT:

MEDI

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES	
XXX	DIMENSION NOT TO SCALE
USED ON	RELEASED
REGUCENTRALEN	APP. NCR. 1/27/81
	CH.
	DR/TIT 10-28-80

TOL. EXCEPT
AS NOTED
HOLE
DIA.
FRACT = 1/64"
XX = .03"
XXX = .010"
ANG = 1°

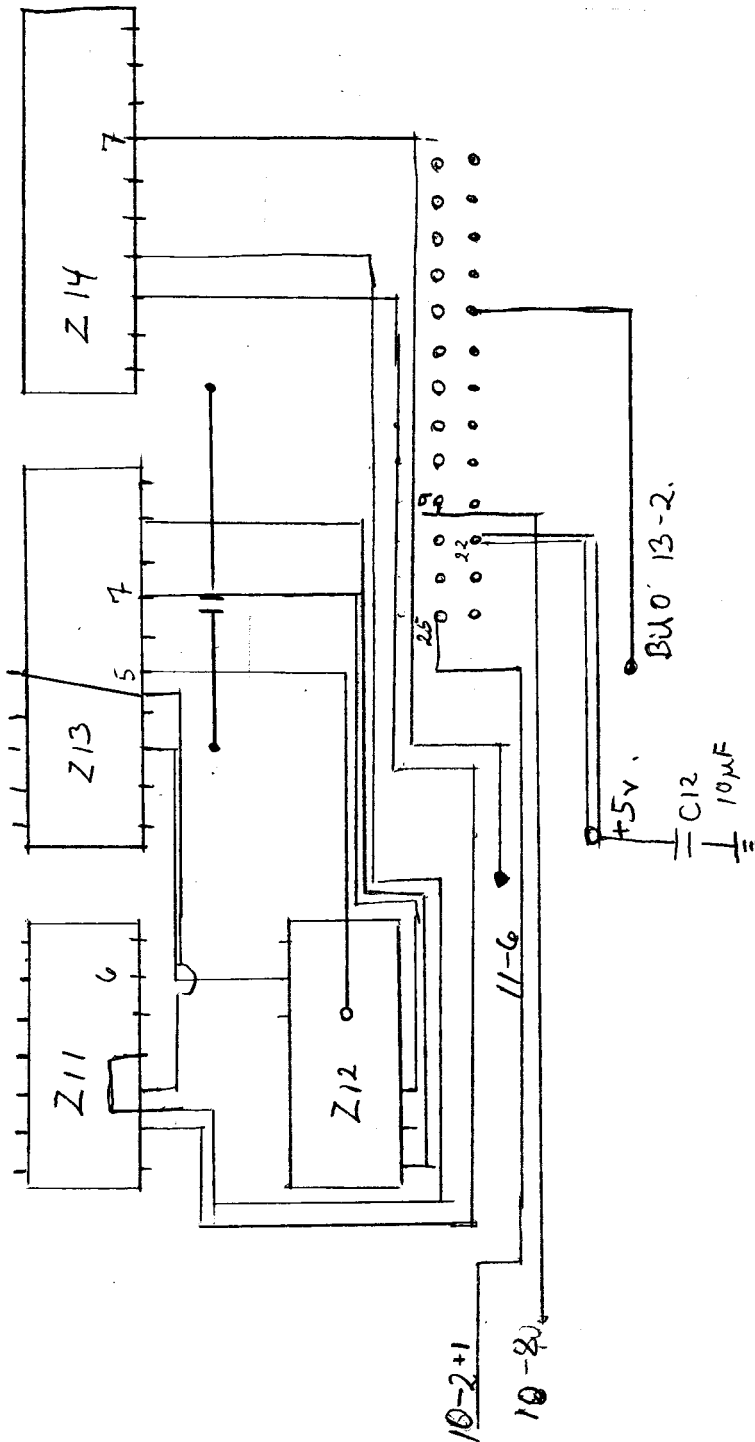
QTY.	PART NO.	DESCRIPTION
SCALE	TITLE	
NONE	KEYTOP & MECH. AS	
key tronic corporation		DWG NO
SPOKANE, WASH. U.S.A.		65-022
		SHEET

Z 12.

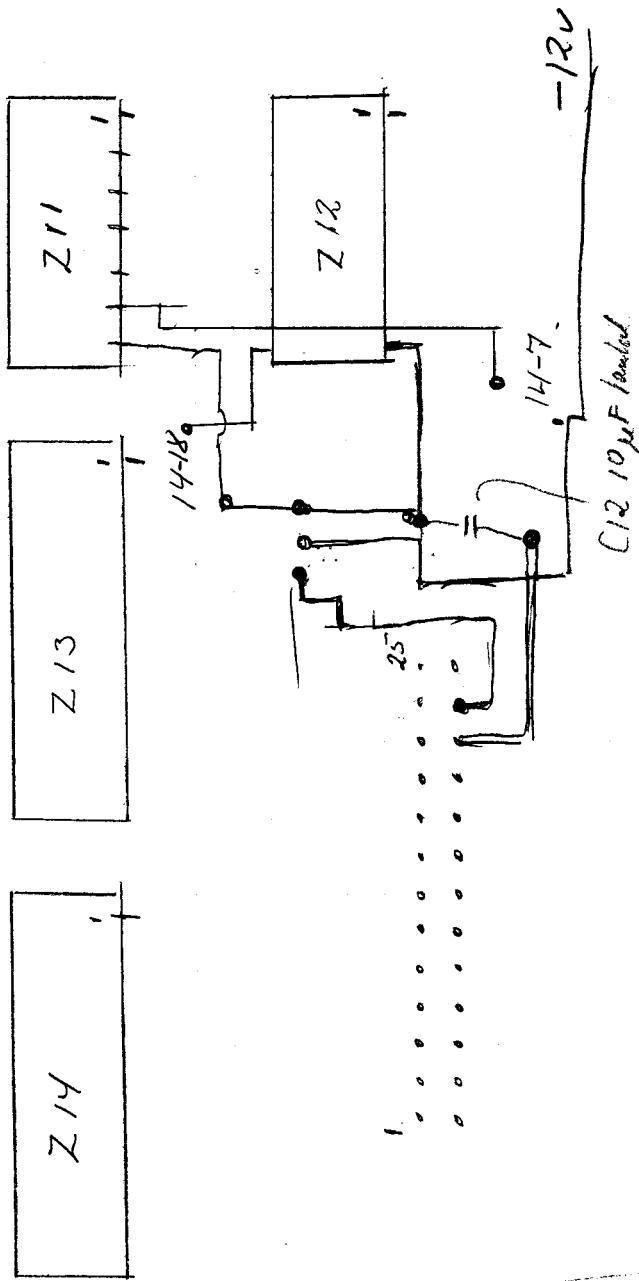
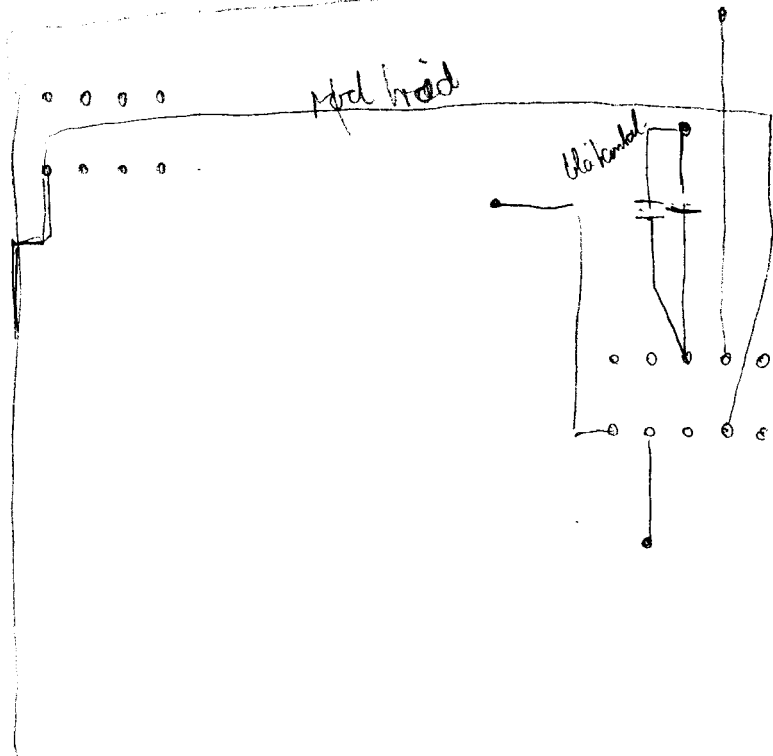
C5 > 1 Z12 2 Z 3-13 Z 14-13 Z 2-13, B 5.
C6 > 6 Z12 4 Z 14-14 Z 3-14 Z 2-14, B 6.
C7 > 5 Z12 6 Z 3-17 Z 14-17 Z 2-17, B 7.
C8 > 9 Z12 8 Z 14-18 Z 3-18 Z 2-18, B 9

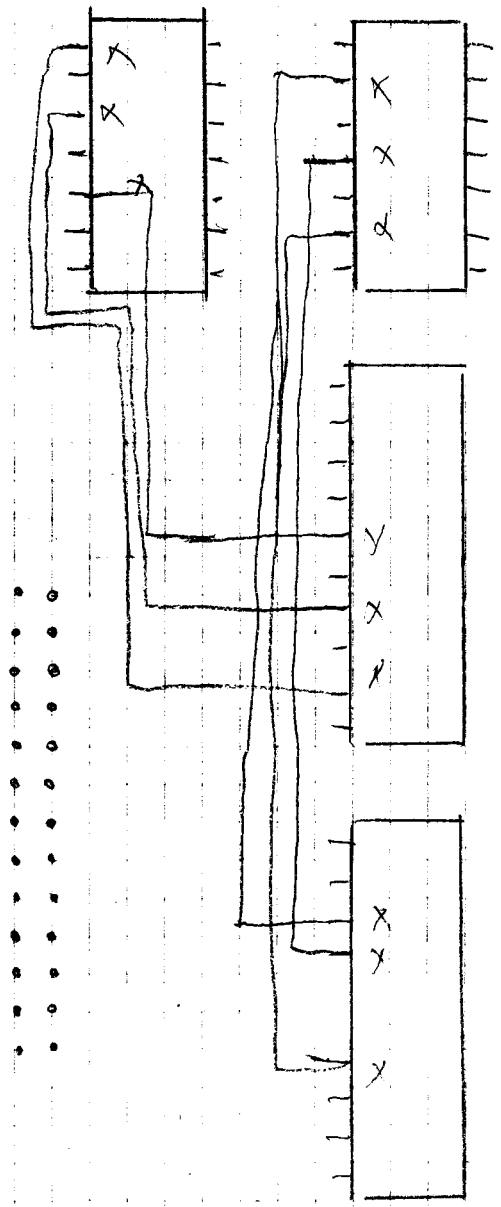
742504

sel fra komponent sidten,



Sel fra loddeside





KH386N-3 7425132 742504 7425240 7425373

742504

22-908-3
8037.

P2101
803DHP

7425373

742508

22-950-3
8036

(((((

RCSL No: 44-RT1981

Edition: March 1981

Author: Mogens V. Pedersen

Title:

RC752 Video Display Monitor
Technical Manual

Keywords:

RC700, RC702, RC752, VDU752, Video Display.

Abstract:

This manual contains the technical manual for RC752 Video Display Monitor used in the RC700 system.

(32 printed pages)

<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
1. GENERAL DESCRIPTION	1
2. OPERATIONS	2
2.1 POWER Switch	2
2.2 BRIGHTNESS Control Knob	2
2.3 CONTRAST Control Knob	2
2.4 H. HOLD Control Knob	2
2.5 V. HOLD Control Knob	2
3. ADJUSTMENT	3
4. CONNECTION TO RC702	5
5. SPECIFICATIONS	6
6. CIRCUIT DESCRIPTION	7

1. GENERAL DESCRIPTION

1.

RC752 Video Display Monitor is normally used in connection with the RC702 Microcomputer system, but may also be used by other computer systems. The RC752 is designed by:

Nippon Electric Co., Ltd.
Tokyo,
Japan.

This manual is based on the service manual for NEC (Nippon Electric Co., Ltd.), Model JB-1201M(A). The RC752 is a special version of JB-1201M(A) and the corrections to this service manual are made by NEC and by RC Computer.

The technical name for RC752 is VDU752.

2. OPERATIONS

2.

In sections 2.1 to 2.3 the switches and controls on the front of the video monitor are explained. Sections 2.4 to 2.5 explain the switches and controls on the back of the video monitor.

2.1 POWER Switch

2.1

The picture will appear after approximately 10 seconds, when the power switch is turned to the right, and will disappear when the switch is turned to the left.

2.2 BRIGHTNESS Control Knob

2.2

The further to the right the knob is turned, the brighter the picture becomes. Adjustment needed is depending on ambient lighting conditions.

2.3 CONTRAST Control Knob

2.3

The further to the right the knob is turned, the more emphasized is the contrast between black and white. Do not overemphasize the contrast; it may strain your eyes.

2.4 H. HOLD Control Knob

2.4

If stripes appear on the screen, turn the knob slowly until the stripes disappear and a normal picture appears.

2.5 V. HOLD Control Knob

2.5

If the picture moves upward or downward, turn this knob slowly until a normal picture appears.

3. ADJUSTMENT

3.

The locations of the main part on the circuit board are shown in fig. 1.

The following adjustment may be done:

+B Adjustment: VR601 (+B ADJ)

Connect a DC voltmeter (range: 15 to 20V) to TP91 on the printed circuit board and the ground, and adjust VR601 until the voltmeter reads +12V.

Horizontal Width Adjustment: L503 (H. width coil)

- (1) Display a character signal (e.g. for the letter H) fully on the CRT screen, and adjust the brightness and contrast to the best.
- (2) Turn the hexagonal core of L503 until the optimum horizontal amplitude is obtained.

Vertical Height Adjustment (VR401 V. HEIGHT).Vertical Linearity Adjustment (VR402 V. LIN)

- (1) Display a character signal (e.g. the letter H) fully on the CRT screen, and adjust the brightness and contrast to the best.
- (2) Turn VR401 and VR402 until the optimum vertical amplitude and linearity are obtained.

Focus Adjustment (VR901)

Bring the picture to the best focus by adjusting VR901.

LOCATIONS OF MAIN PARTS

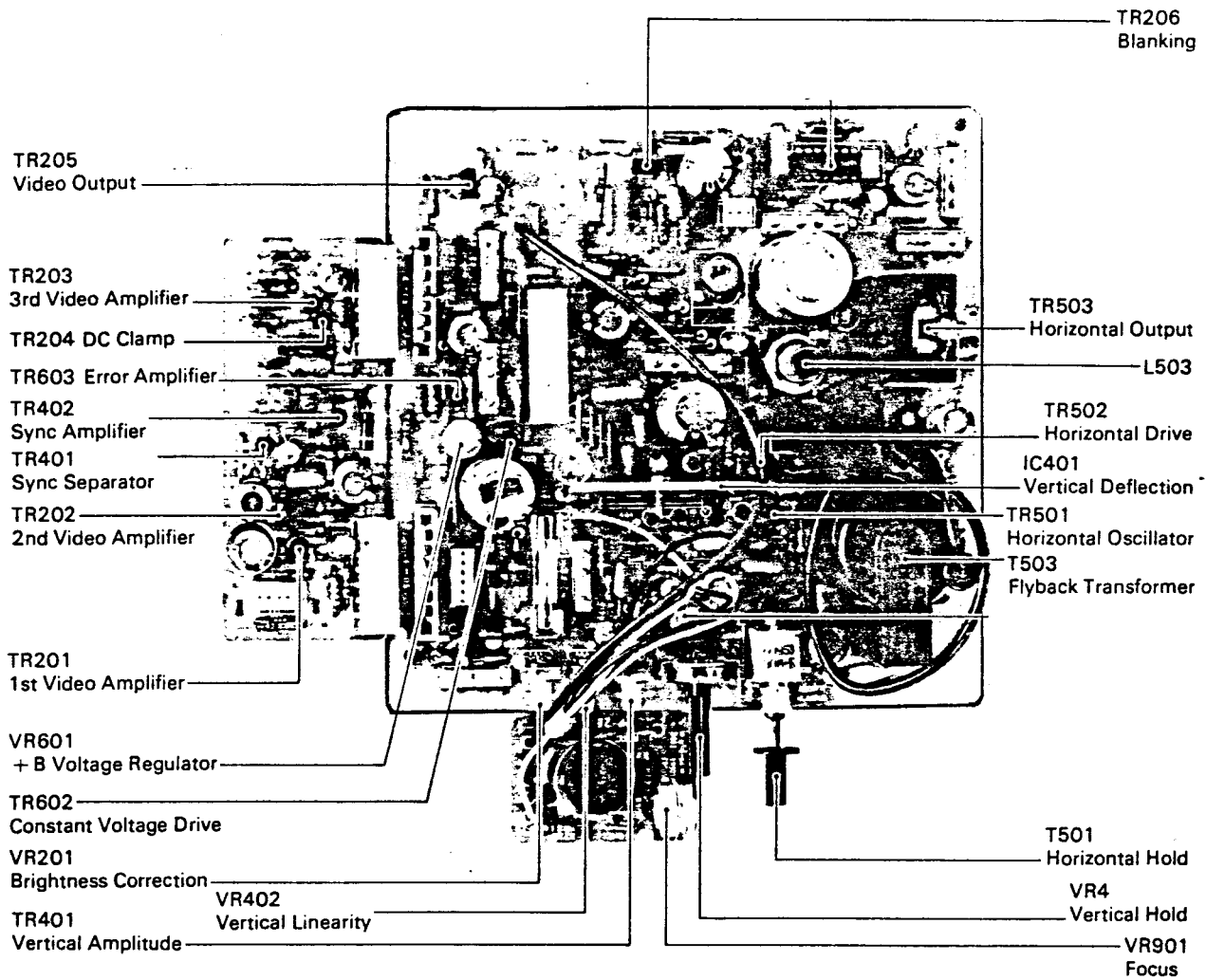


Figure 1: Location of main parts on PCBA.

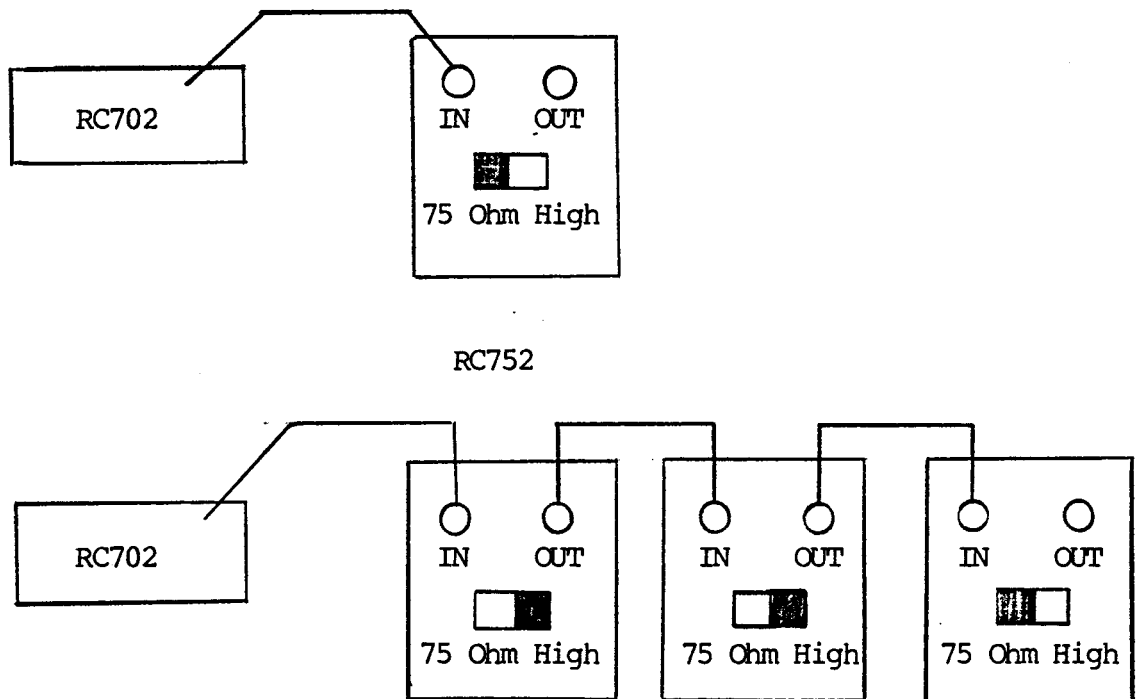
4. CONNECTION TO RC702

4.

The power cable from RC752 is connected to RC702 to the Monitor Power Jack, which can only supply one RC752.

The signal from RC702 is supplied to RC752 using a coax cable and more than one monitor may be connected to the same signal.

The connections are made the following way:



The signal cable supplied together with RC752 is named CBL919.

5. SPECIFICATIONS

5.

Picture Tube	: C1270P4Y ARU 12" diagonal and 90° deflection
Phosphor	: Yellow (P4Y)
Video Input Signal	: Composite Video signal
Polarity	: Negative sync.
Level	: 1.0 V p-p
Impedance	: 75 Ohm (switchable to higher impedance)
Input Terminal	: BNC jacks
Active Display Area	: 230 (W) x 165 (H) mm
Scanning Frequency	
Horizontal	: 15.4 KHz (64.9 μ S)
Vertical	: 50 Hz (20 μ S)
Active Video Period	
Horizontal	: 48.1 μ S
Vertical	: 17.9 mS
Video Bandwidth	: 30 Hz - 20 MHz (\pm 3 dB)
Display Characters	: 80 characters with 25 lines 5 x 7 dot matrix (7 x 11 dot/cell)
Controls	
Inside	: H. width, V. height, V. lin., focus, Sub bright- ness
Outside	: Brightness, Contrast, H. hold, V. hold
Operating Ambient Temperature	: 0°C - +40°C
Power Supply	: 15 V DC
Power Consumption	: 15 W
Dimensions	: 360 (W) x 296 (H) x 330 (D) mm
Weight	: 5 kg

Note: The above specifications are subject to change without further notice.

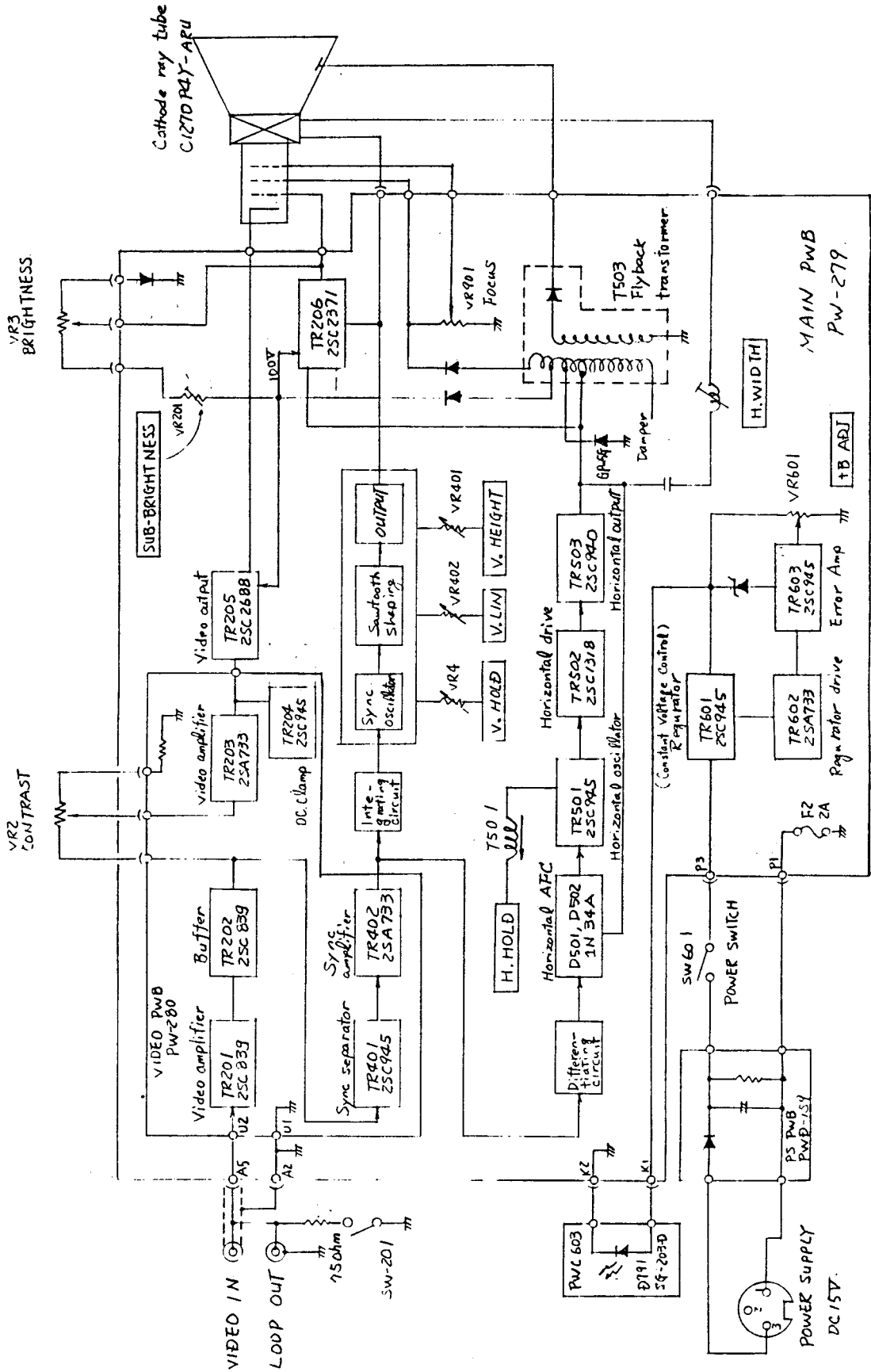
6. CIRCUIT DESCRIPTION

6.

The rest of the manual is a part of the original NEC manual and contains the following parts:

- A. Block Diagram
- B. Circuit Explanation, 6 pages
- C. Circuit Diagram, 21 pages
- D. Drawings of Printed Circuit Boards
- E. Troubleshooting

BLOCK DIAGRAM



2. Explanation of VIDEO PWB

The VIDEO INPUT of 1 Vpp is added from the A5 terminal of PW-279 of the main PWB, then added to the base of TR201 of 1st VIDEO AMP via the U₂ terminal of VIDEO PWB PW-280

Subsequently, it is amplified to about 2.7 Vpp by TR201 and TR202.

Between the output side of TR202 and the amplifier of the next stage, VR is installed, and the input to TR203 of the next stage is increased or decreased by the changes in this division ratio, and the adjustment of the picture contrast is made.

Each stage of the image portion is connected with capacitors, so the direct current portion will be eliminated, and the average brightness of the picture will be reduced. On the other hand, to the base of TR204, pulses of the synchronous pulses of TR402, which have been delayed by L201, C206, are input and only during this pulse period TR204 will maintain continuity.

This period is equivalent to the back porch of the composite video signal, and when continuity is made for TR204, the back porch of the video signal on the collector side will be clamped to the electric potential of the emitter side of TR204.

In this way, VIDEO signal of which the direct current portion has been regenerated by TR204 will be sufficiently amplified by TR205, and impressed on the cathode of the CRT.

On the other hand, the output of TR202 will appear at test point TP31, and be synchronously separated at SYNC SEP of TR401. The synchronous signal which has been amplified by TR402 will pass through integration circuit composed of R408, R409, C405 and C408 via terminal W2, and only the vertical synchronous ones will be separated and added to pin 5 of IC401.

Furthermore, the synchronous signals which passed through the differentiating circuits C501 and R501 via terminal W3 will be added to the unbalanced type AFC Circuit.

3. Sound Output Circuit

The sound signal which enters from the SOUND IN terminal will be input to pin 7 of IC301 via S1 terminal of the main PWB and the Sound Adjustment control, VR1.

At this IC, it is amplified to about 40 dB and output to pin 8. To pin 9, voltage to drive this IC is added from C603. C308 and R306 of pin 6 raises the S characteristics. C305 between pin 8 and pin 10 is a capacitor for bootstrap, and R302 is resistance for bias of the output.

4. Vertical Deflection Circuit

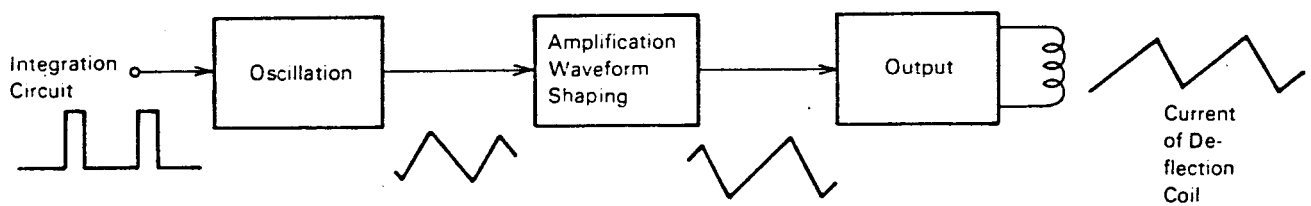


Fig. 4 Composition of Vertical Deflection Circuit

As shown in the block diagram, the base circuit of the vertical deflection circuit is composed of vertical oscillation circuit which generates saw tooth wave voltage, amplification waveform shaping, and output circuit.

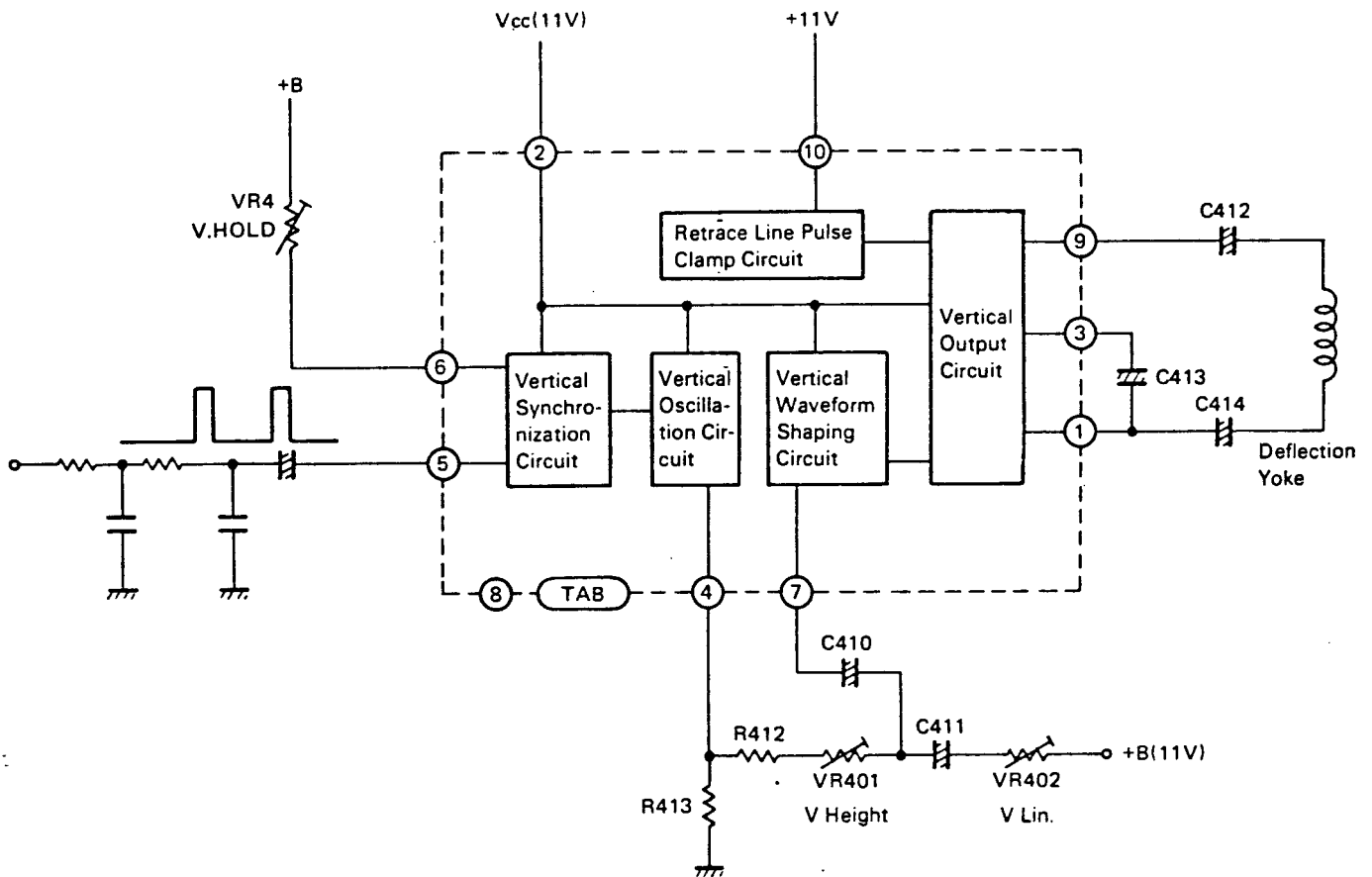


Fig. 5

The vertical synchronous signal that has been synchronously separated and which has passed through the integration circuit is added to the vertical synchronous circuit by pin 5 of IC401.

The saw tooth wave of 50 Hz which has been generated by the vertical oscillation circuit is taken from pin 4, and after passing through R412, VR401 and C410, it is added to pin 7, then after the waveform shaping, it is amplified, and added to the vertical output.

R413 and C409 are time constants which determine the oscillation.

The vertical output waveform is a waveform in which pulse is superposed with sawtooth wave as it is clear from TP82. This is designed so that high voltage is added to retrace line period, and low voltage is added to scanning period in order to decrease the power consumption of vertical deflection circuit by retrace line pulse clamp circuit.

In the above mentioned way, the circuit power consumption is reduced and the operation is done efficiently.

VR401 is VR for adjustment of V Height and VR402 is VR for adjustment of V. Lin, and they are connected to pin 4 and pin 7, respectively.

Furthermore, vertical synchronization is done by VR4 connected to pin 6.

5. Blanking Circuit

During the retrace line period, if the television picture tube is operating, white slantwise lines vertical retrace (flyback) lines will appear on the tube and become obstacle to the picture, so they must be eliminated.

Such a phenomenon occurs when the black label adjusted to the cut-off and below of the picture tube moves, and the scanning lines in the vertical retrace (flyback) line period appears in the picture.

In order to prevent this, it will be sufficient if the television picture tube does not operate during the retrace (flyback) line period.

As an actual circuit operation, positive polarity pulse generated during the retrace (flyback) period is added to the base of the Blanking Transistor TR206 from IC401 pin 1 and the collector of horizontal output transistor TR503, and negative polarity pulse is taken out to the collector of TR206, and this is added to the control grid G1 of CRT via C211.

During the retrace (flyback) line period, the bias of CRT is made deeper, and cut off.

6. Horizontal Deflection Circuit

As shown in Fig. 6, the horizontal deflection circuit is composed of AFC Circuit, Oscillation Circuit, and Output Circuit, and its function is to pass sawtooth wave current synchronized with the horizontal synchronization signal to the deflection coil.

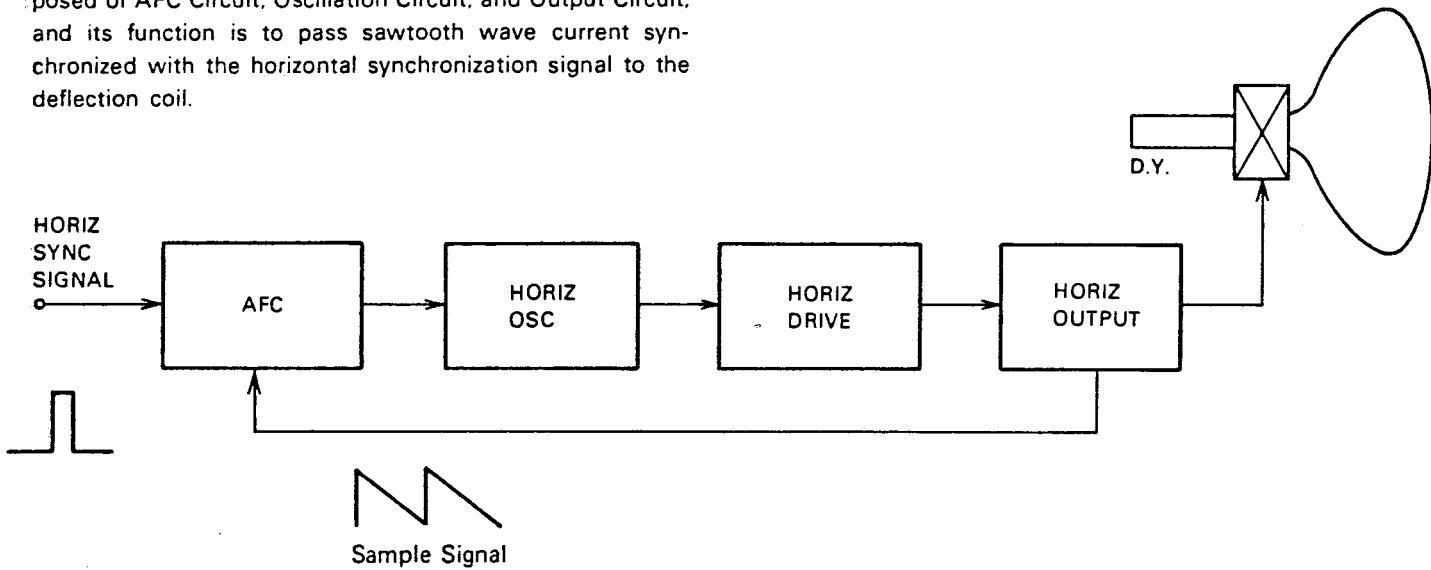


Fig. 6 Horizontal Deflection Circuit

Function of AFC Circuit

The vertical synchronous signals which control the vertical oscillation current pass through 2 or 3 stages of integration circuit which is a kind of lowpass filter, so the horizontal synchronous signals and pulsing noises are leveled off and do not appear in the output.

Therefore, the oscillation circuit can be directly controlled by the synchronous signals. However, horizontal synchronous signals are taken out by passing them through a kind of high-pass filter, so pulsing noises will be mixed, and in the same way as the vertical circuit, if direct control is done, the synchronization will be disturbed, and a stable picture can not be obtained.

Consequently, for the control of horizontal oscillation frequency, AFC circuits are used.

The AFC circuits will compare the phase of the oscillation circuit and the phase of the synchronous signal, then generate direct current output voltage proportionate to the phase difference. This voltage is added to the oscillation circuit, and the oscillation frequency and its phase will be coincided with the horizontal synchronous signal.

The horizontal oscillation signal fed back to the AFC circuit is normally done by changing the pulse generated in the horizontal output circuit into sawtooth wave (This is called comparative waveform signal).

7. Horizontal Oscillation Circuit

The horizontal oscillation circuit generates frequency of 15.625 kHz, and just like in case of the vertical oscillation circuit, blocking oscillation circuit which employs the oscillation transformer is often used.

The oscillation time constant becomes rather small time constant than that in case of the vertical oscillation circuit at R510, C507 and C508.

The Oscillation Transformer is designed so that positive feedback and oscillation will be made at T501.

In case the base voltage of the oscillation transistor becomes high, the oscillation frequency also becomes high, and in case the base voltage becomes low, the oscillation frequency becomes low.

Therefore, the frequency control will function as follows. If the oscillation frequency begins to get low (The phase is delayed) the output of AFC increases.

Since this voltage is added to the base of the horizontal oscillation, it will function as raising the oscillation frequency (The phase is advanced.).

Contrary to this, if the oscillation frequency begins to get high (The phase advances), the output of AFC will become low, and this will be added to the oscillation circuit. Consequently, it will function as lowering the oscillation frequency (The phase is delayed). In the above mentioned way, the horizontal oscillation frequency and its phase will always coincide with the horizontal synchronous signal.

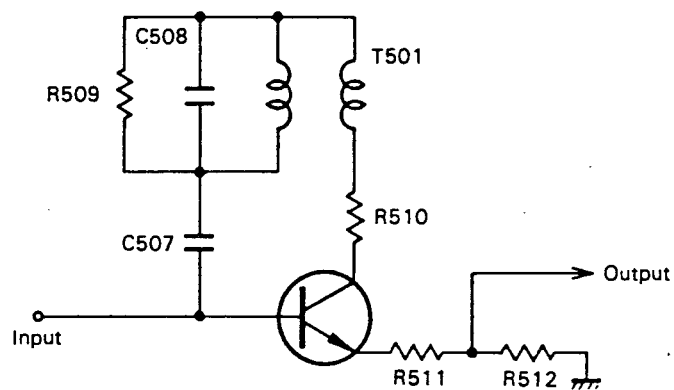


Fig. 7 Horizontal Oscillation Circuit

8. Horizontal Drive Circuit

The horizontal oscillation drive circuit is located between the oscillation circuit and the output circuit, and its function is to amplify the oscillation output and drive the output circuit. In Fig. 8, its circuit is shown.

The waveform which is amplified is a waveform like rectangular waves. Since transformers are used, sharp pulses generate when the transistors become ON or OFF. C510 and R513 are inserted to absorb such pulses.

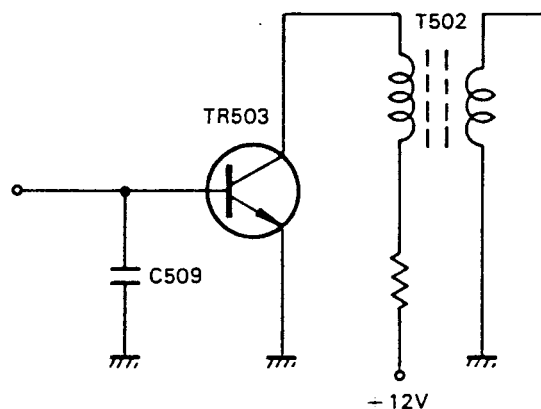


Fig. 8 Horizontal Drive Circuit

9. Horizontal Output Circuit

The horizontal output circuit has the function of sending sawtooth wave current of 15.625 kHz to the horizontal deflection coil. However, unlike the vertical output circuit,

this is done by the switch operation of the transistors. Fig. 9 shows the horizontal output circuit.

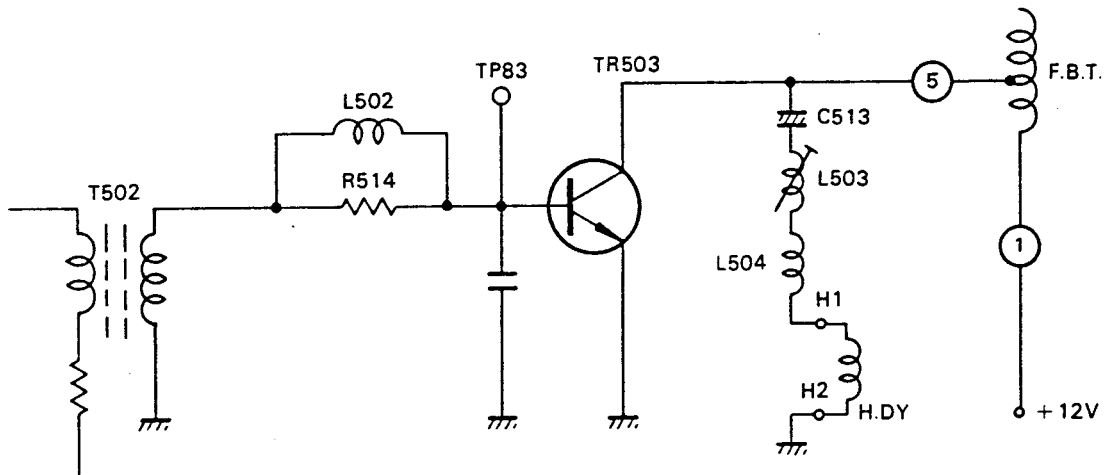
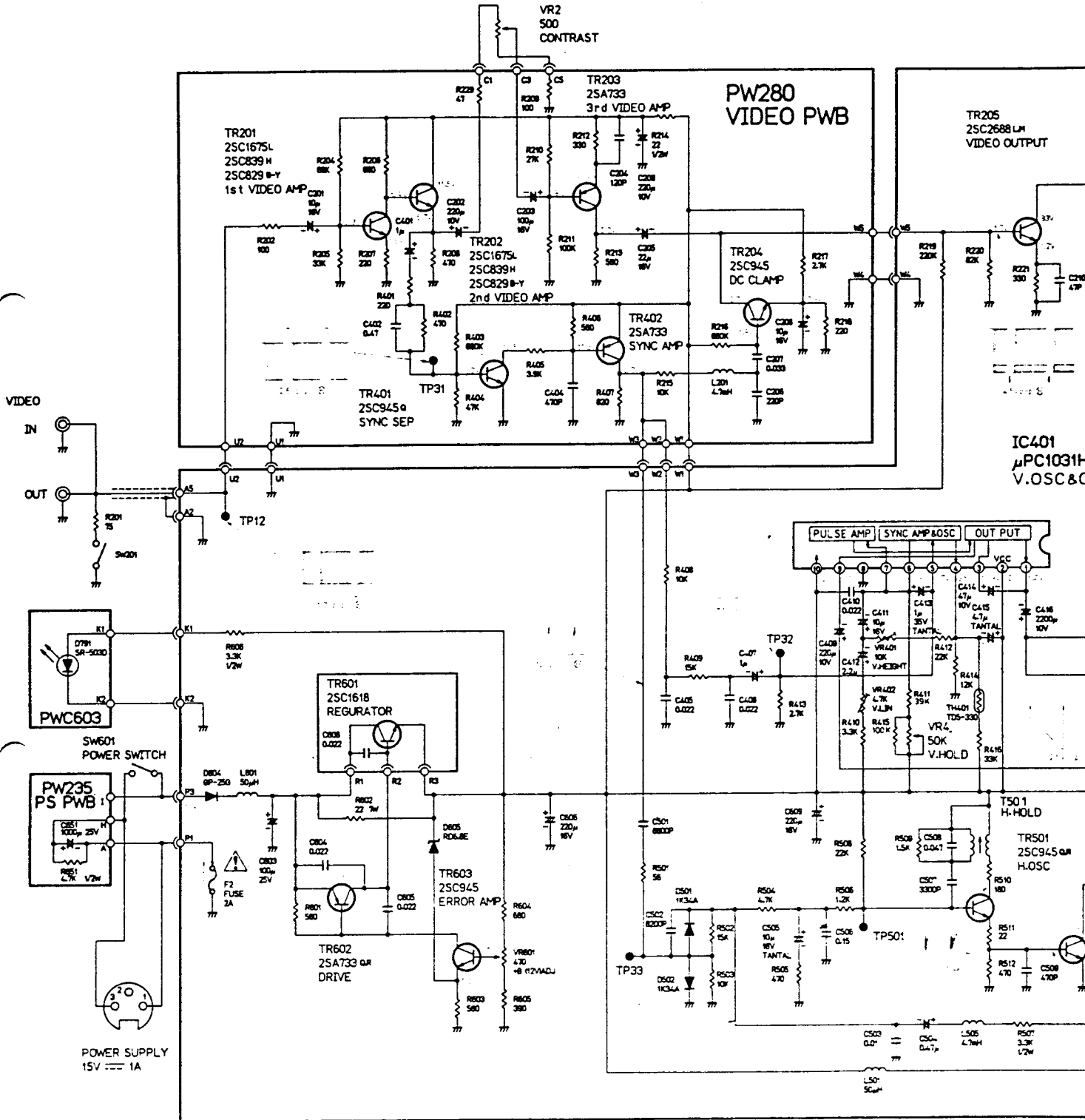
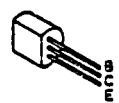
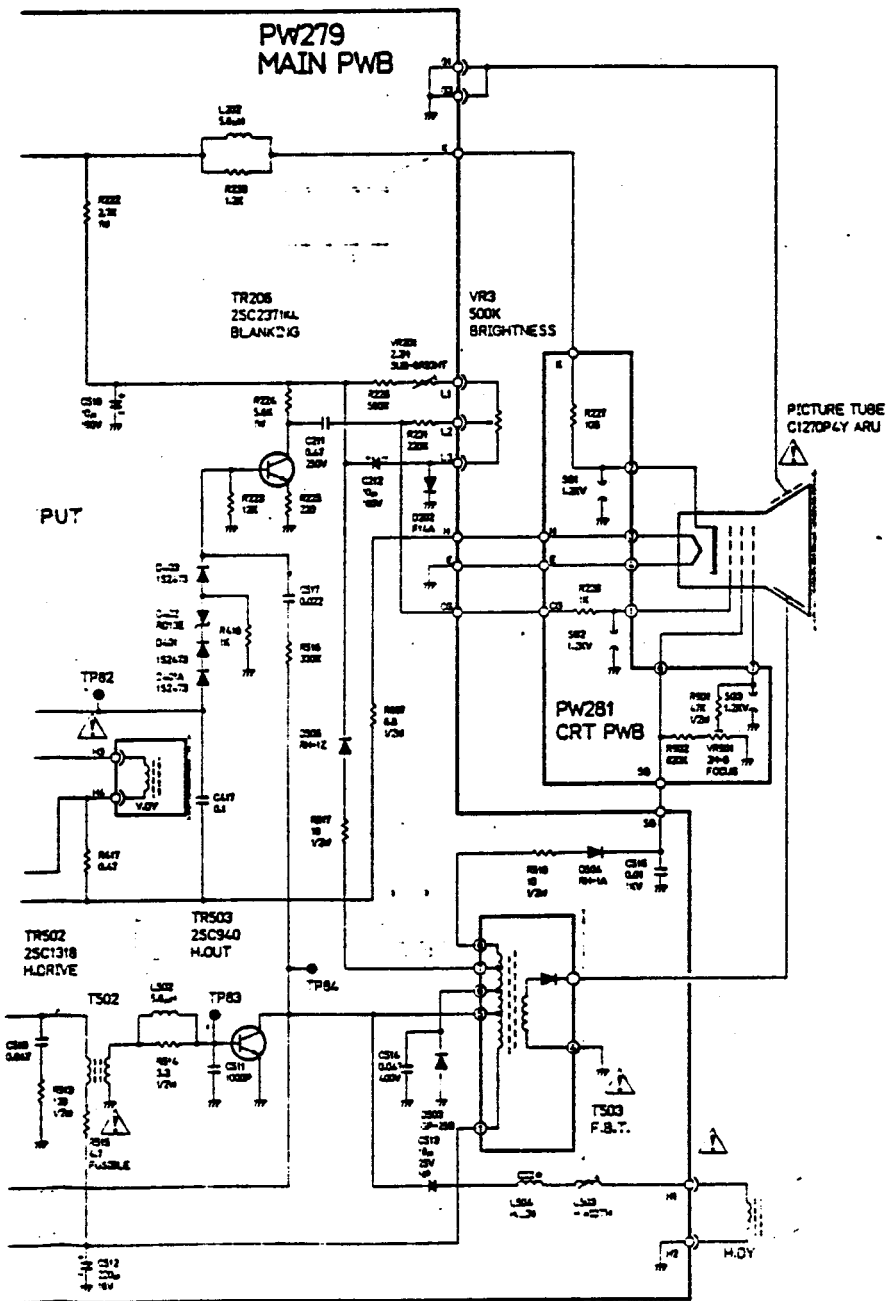


Fig. 9 Horizontal Output Circuit

MODEL RC 752 SCHEMATIC DIAGRAM





- 25A733
- 25C1318
- 25C3002
- 25C945
- 25C826829
- 25C836839
- 25C1684



- 25C2371
- 25C2568



- 25C940
- 25C1618

E: EMITTER
B: BASE
C: COLLECTOR

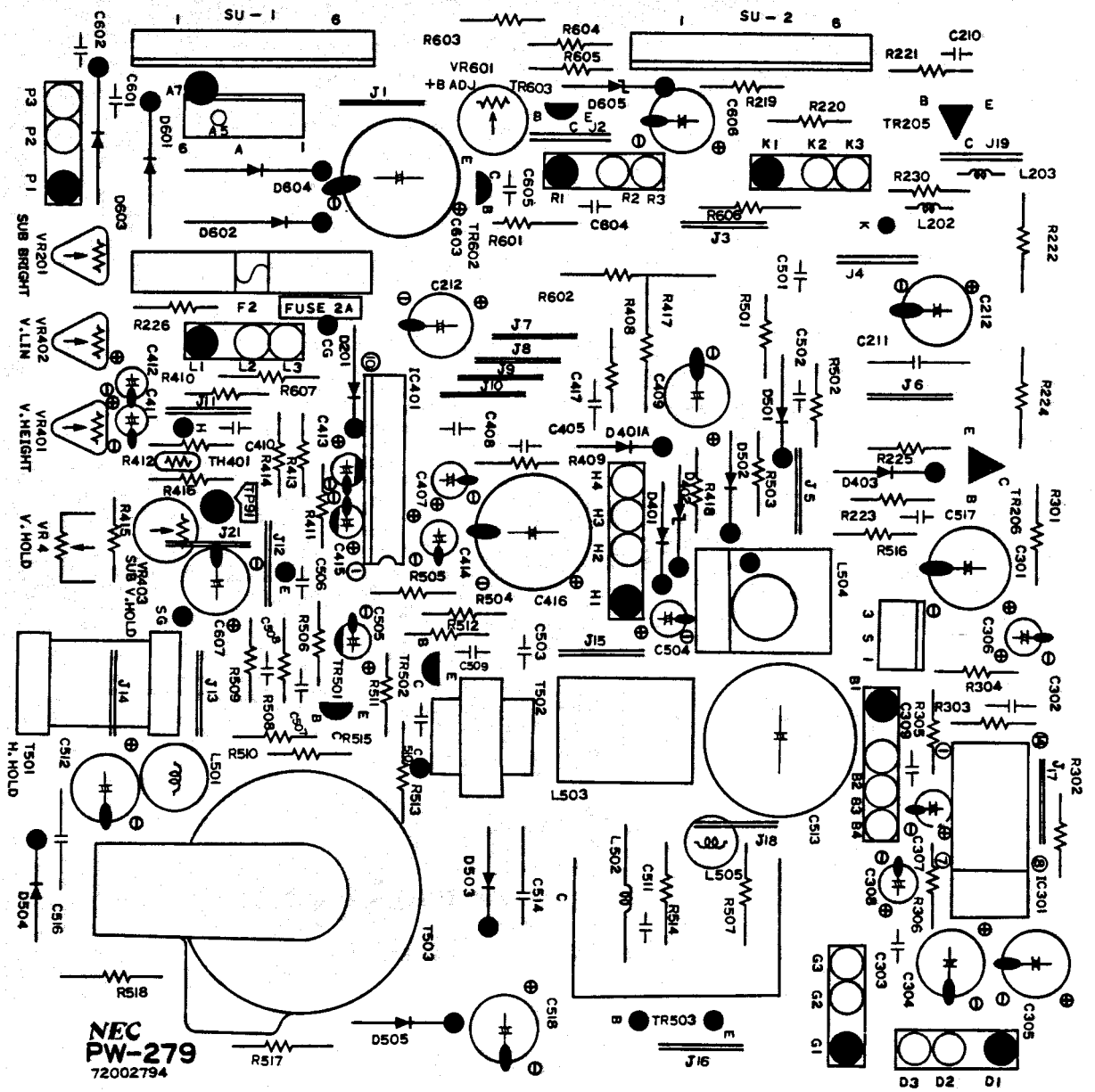
NOTES

1. RESISTOR VALUES ARE IN OHMS K=1000 M=1000000
2. ALL RESISTORS ARE 1/4WATT, EXCEPT WHERE OTHERWISE INDICATED.
3. CAPACITOR VALUES ARE IN μF UNLESS OTHERWISE INDICATED. P =
4. ALL CAPACITORS ARE 50VOLTS EXCEPT WHERE OTHERWISE INDICATE
5. VOLTAGES AND WAVEFORMS ARE MEASURED UNDER THE CHARACTER
- SIGNALS IN THE CONDITIONS OF CONTRAST AND BRIGHTNESS CONTR
- ARE MAXIMUM AND ALL OTHER CONTROLS ARE NORMAL OPERATION.
6. Ⓜ----- HORIZONTAL RATE. Ⓜ----- VERTICAL RATE.

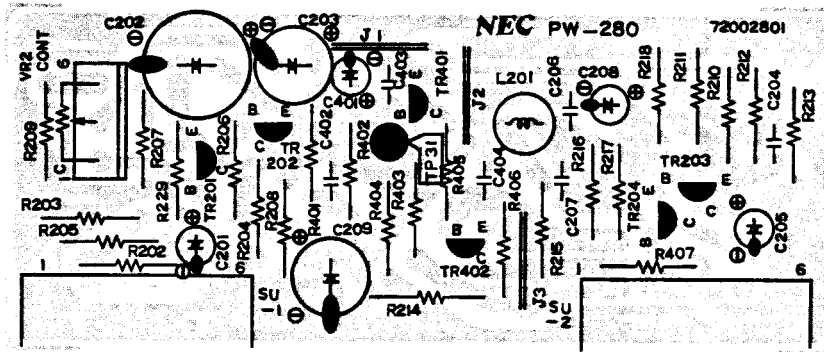
WARNING

REPLACEMENT PARTS WHICH HAVE SPECIAL SAFETY CHARACTERISTICS ARE IDENTIFIED BY A SHADING ON THE SCHEMATIC. REPLACE THESE CRITICAL COMPONENTS WITH RECOMMENDED REPLACEMENT PARTS. DON'T DEGRADE THE SAFETY OF THE SET THROUGH IMPROPER SERVICING.

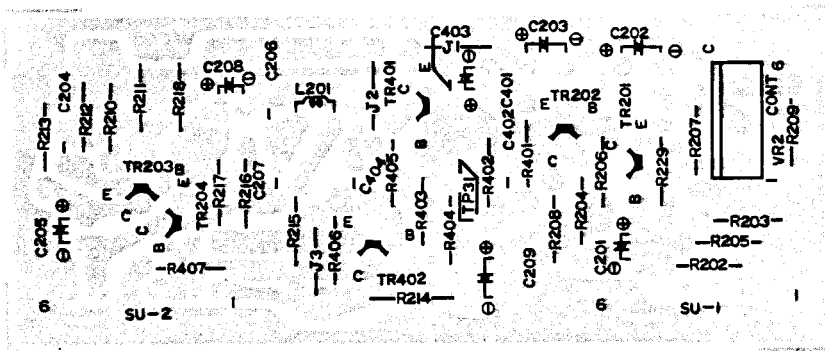
MAIN PWB ASS'Y (PW-279) (Component Side)



VIDEO PWB ASS'Y (PW-280) (Component Side)

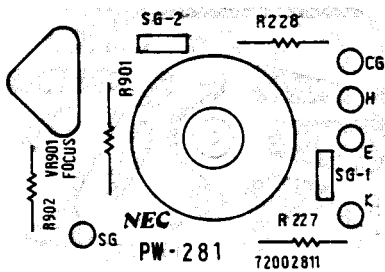


(Solder Side)

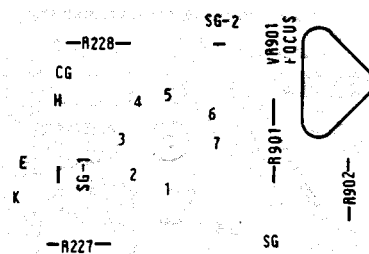


CRT PWB ASS'Y (PW-281)

(Component Side)

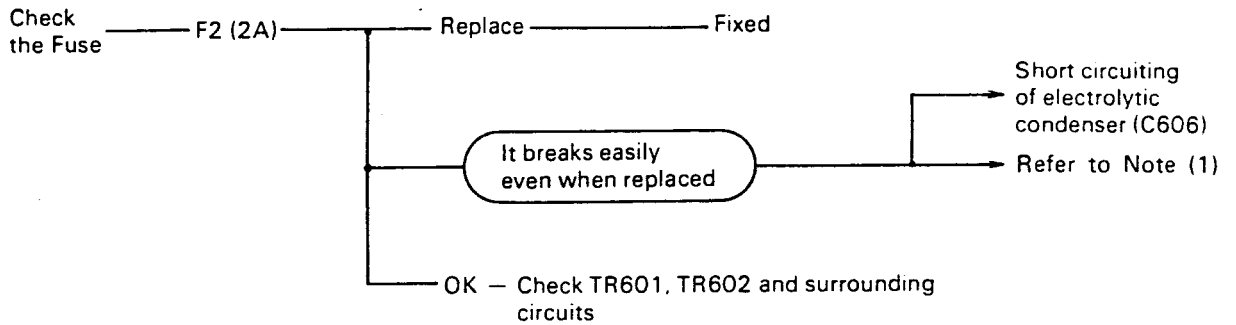


(Solder Side)

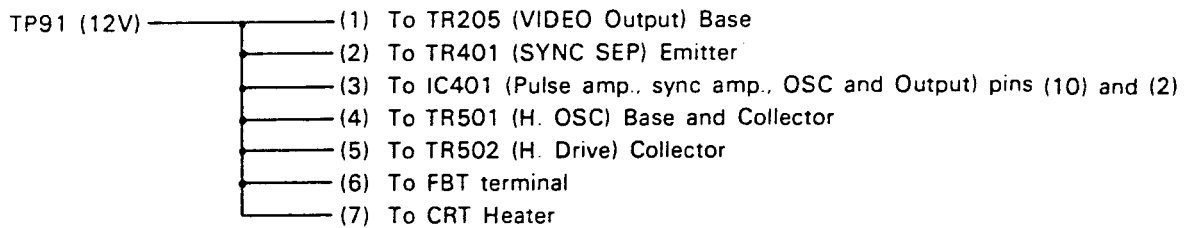


TROUBLESHOOTING

1.



Note (1): Supply source of DC voltage (12V)

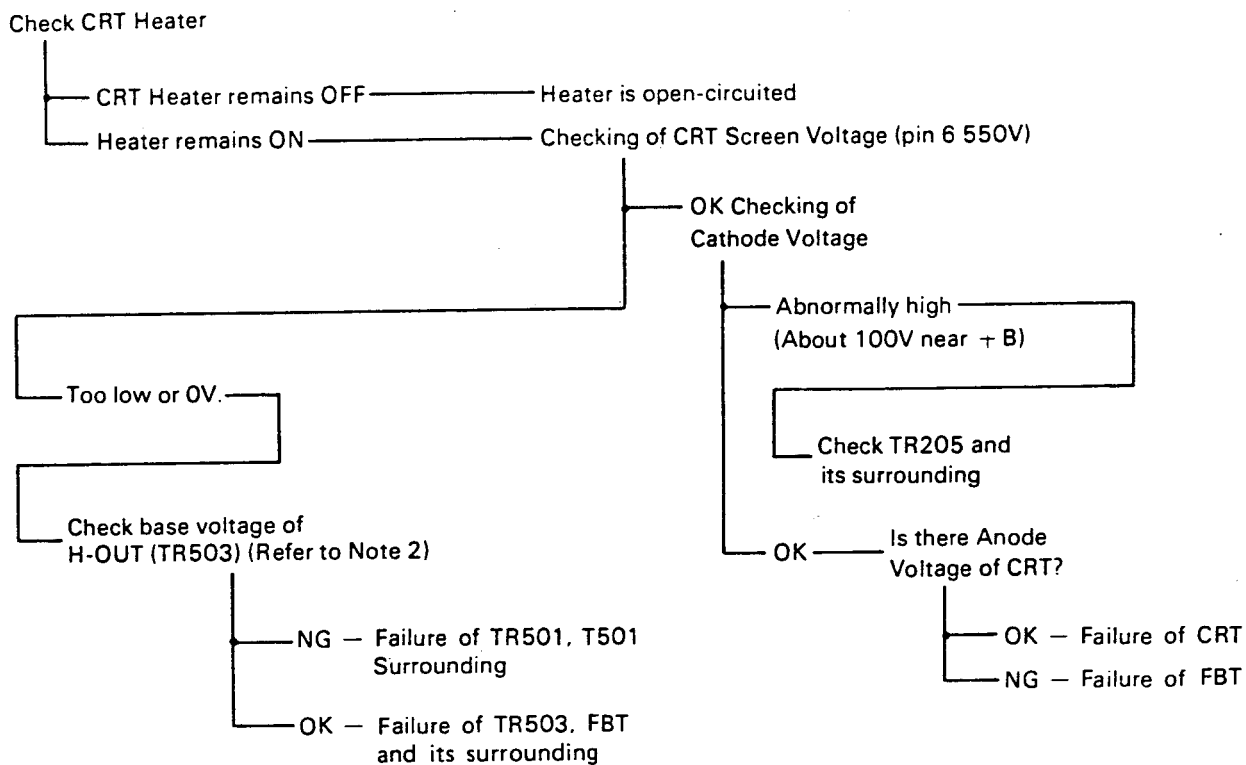


12

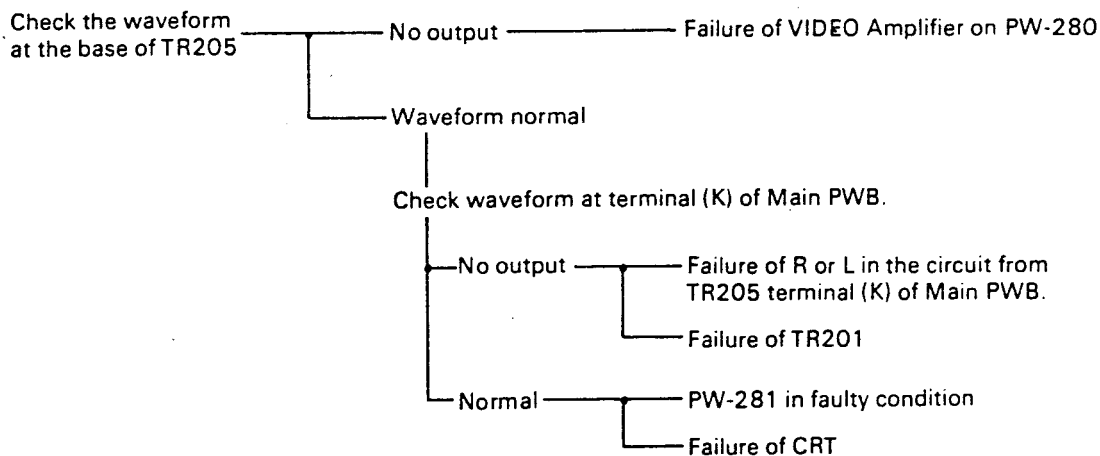
As described above, DC ~~12~~¹²V is supplied to various circuits from TP91. Therefore, in order to find what the cause is, it is necessary to divide the circuits into separate circuits, and judge where the trouble lies.

12

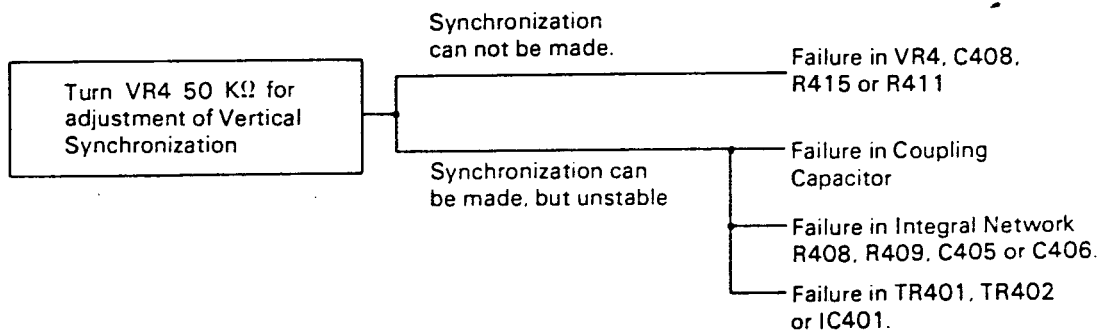
Note (2): In case AC ~~10~~¹²V range tester is connected to the base of TR503, the meter will deflect when the horizontal oscillating circuit is oscillating, so it can be judged whether the trouble exists before the oscillating circuit or after the oscillating circuit.



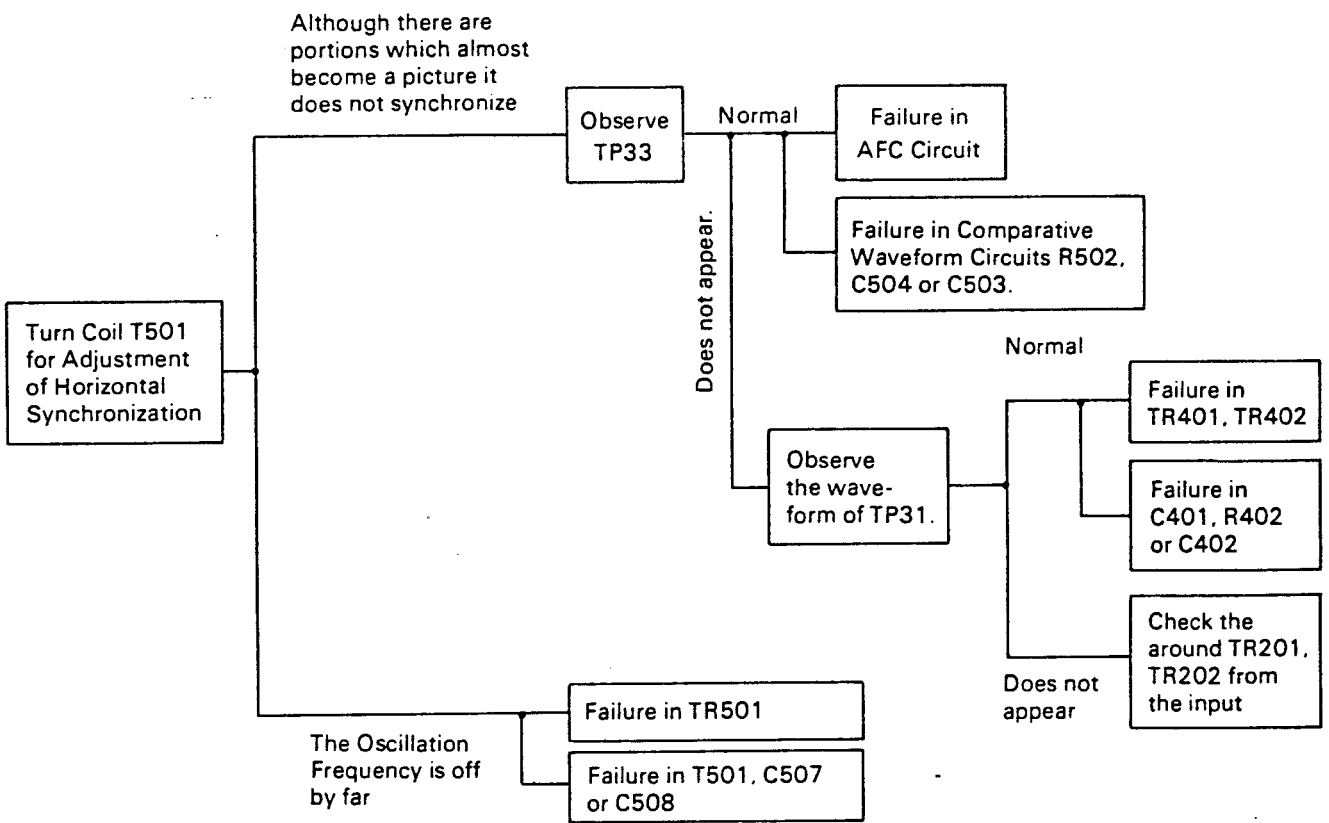
2. ~~Sound and raster~~ are normal, but picture does not show up.



3. ~~Vertical Synchronization~~ can not be made.



4. Horizontal Synchronization can not be made.



RETURN LETTER

Title: RC752 Video Display Monitor
Technical Manual

RCSL No.: 44-RT1981

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: _____ Title: _____

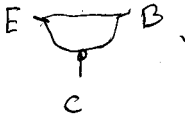
Company: _____

Address: _____

Date: _____

Thank you

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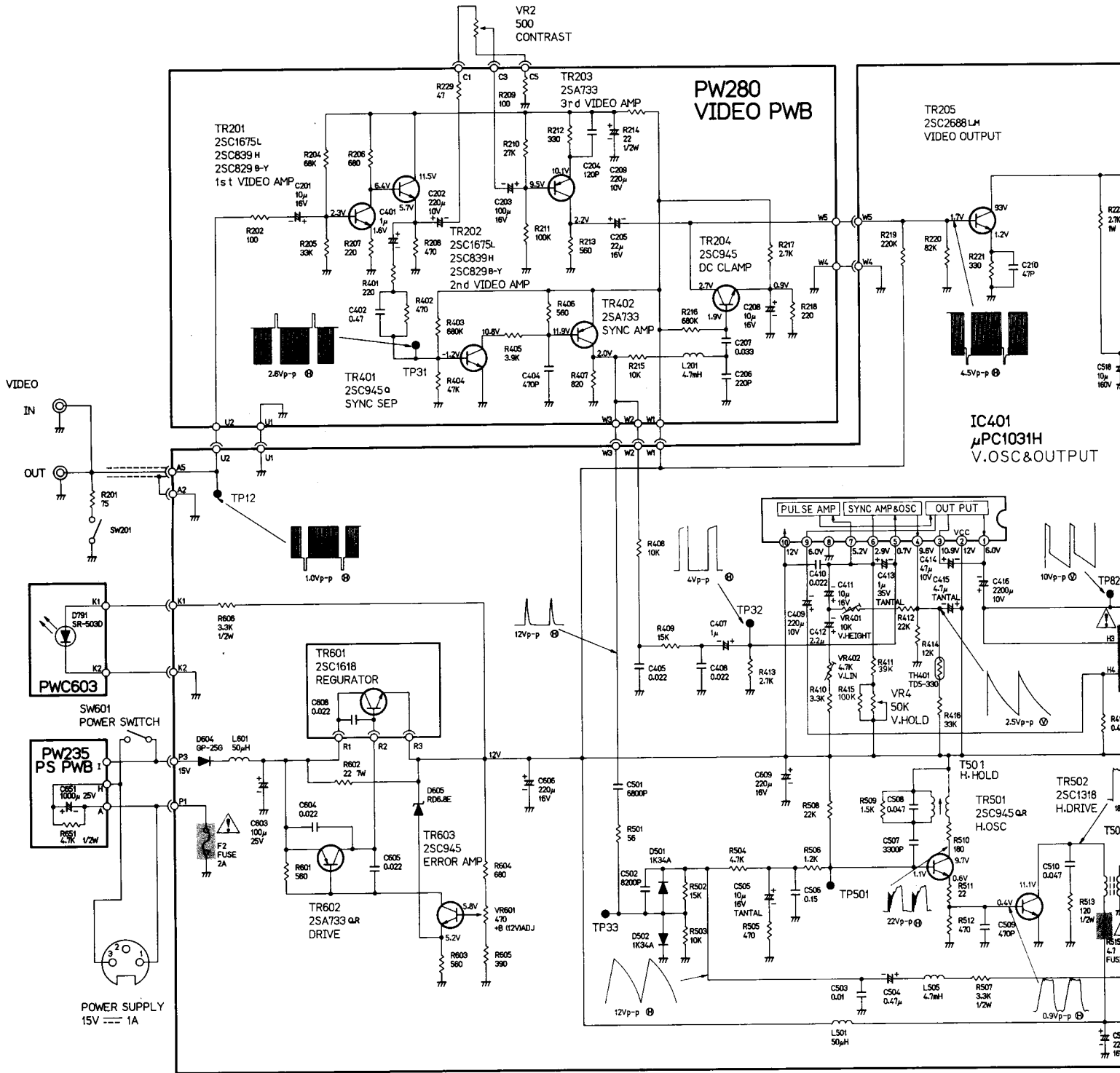
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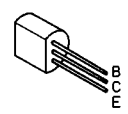
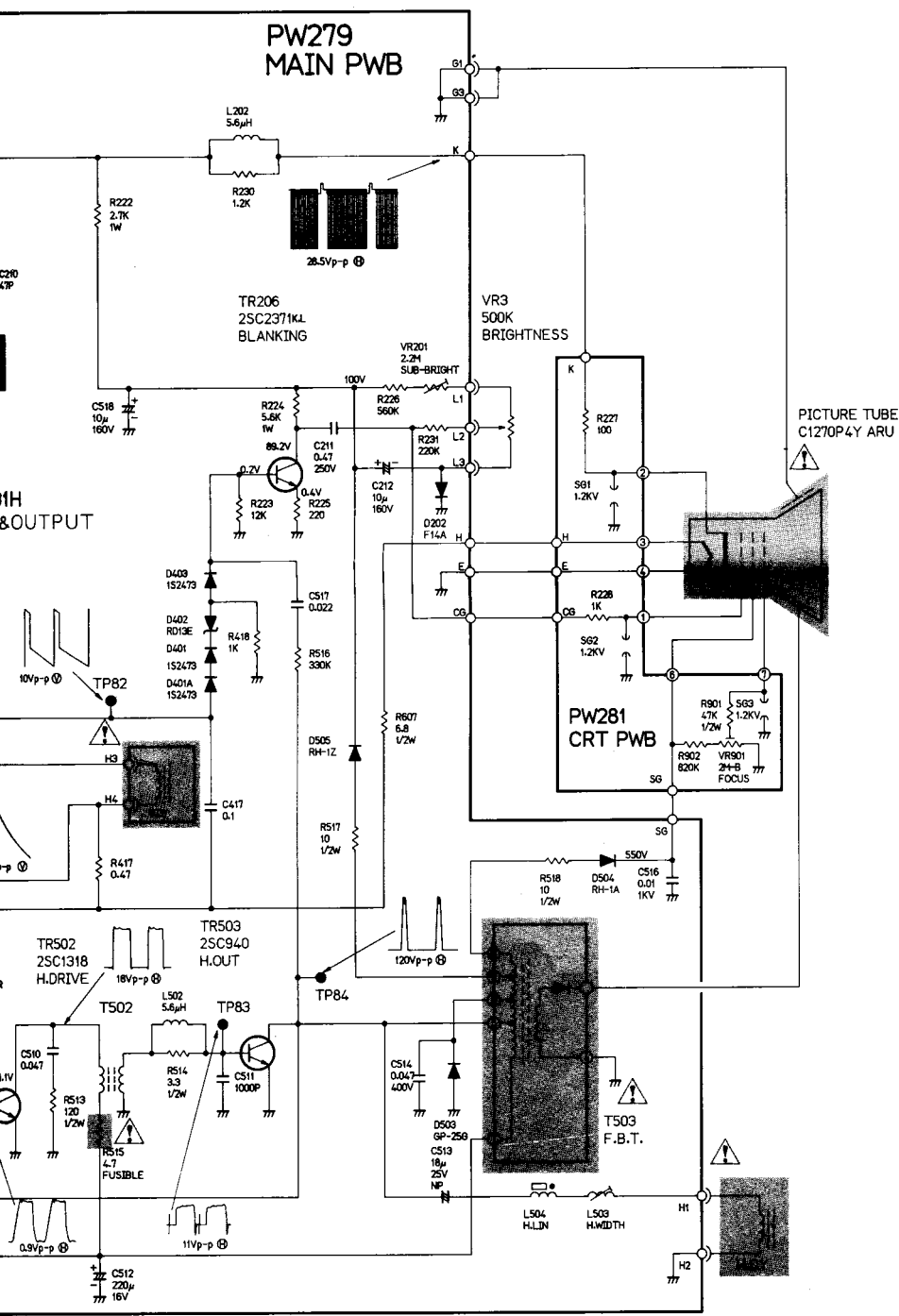
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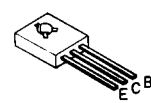
Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark

MODEL RC 752 SCHEMATIC DIAGRAM

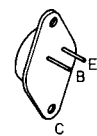




- 25A733
- 25C1318
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- 25C945
- 25C828.829
- 25C838.839
- 25C1684



- 25C2371
- 25C2688



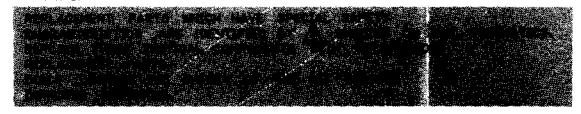
- 25C940
- 25C1618

E: EMITTER
B: BASE
C: COLLECTOR

NOTES

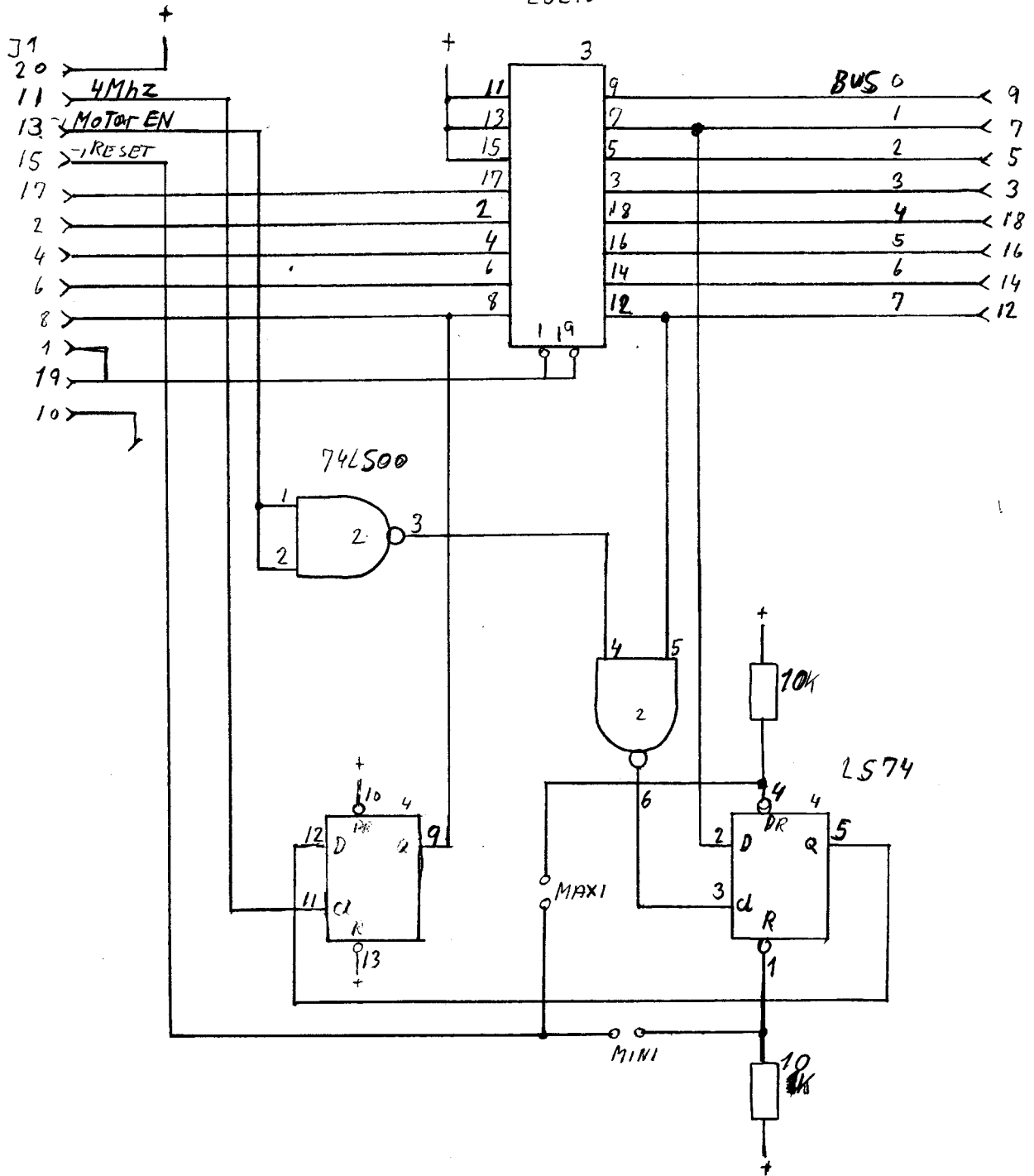
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2. ALL RESISTORS ARE 1/4WATT, EXCEPT WHERE OTHERWISE INDICATED.
3. CAPACITOR VALUES ARE IN μ F UNLESS OTHERWISE INDICATED. P=PF
4. ALL CAPACITORS ARE 50VOLTS EXCEPT WHERE OTHERWISE INDICATED.
5. VOLTAGES AND WAVEFORMS ARE MEASURED UNDER THE CHARACTER SIGNALS IN THE CONDITIONS OF CONTRAST AND BRIGHTNESS CONTROLS ARE MAXIMUM AND ALL OTHER CONTROLS ARE NORMAL OPERATION.
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WARNING



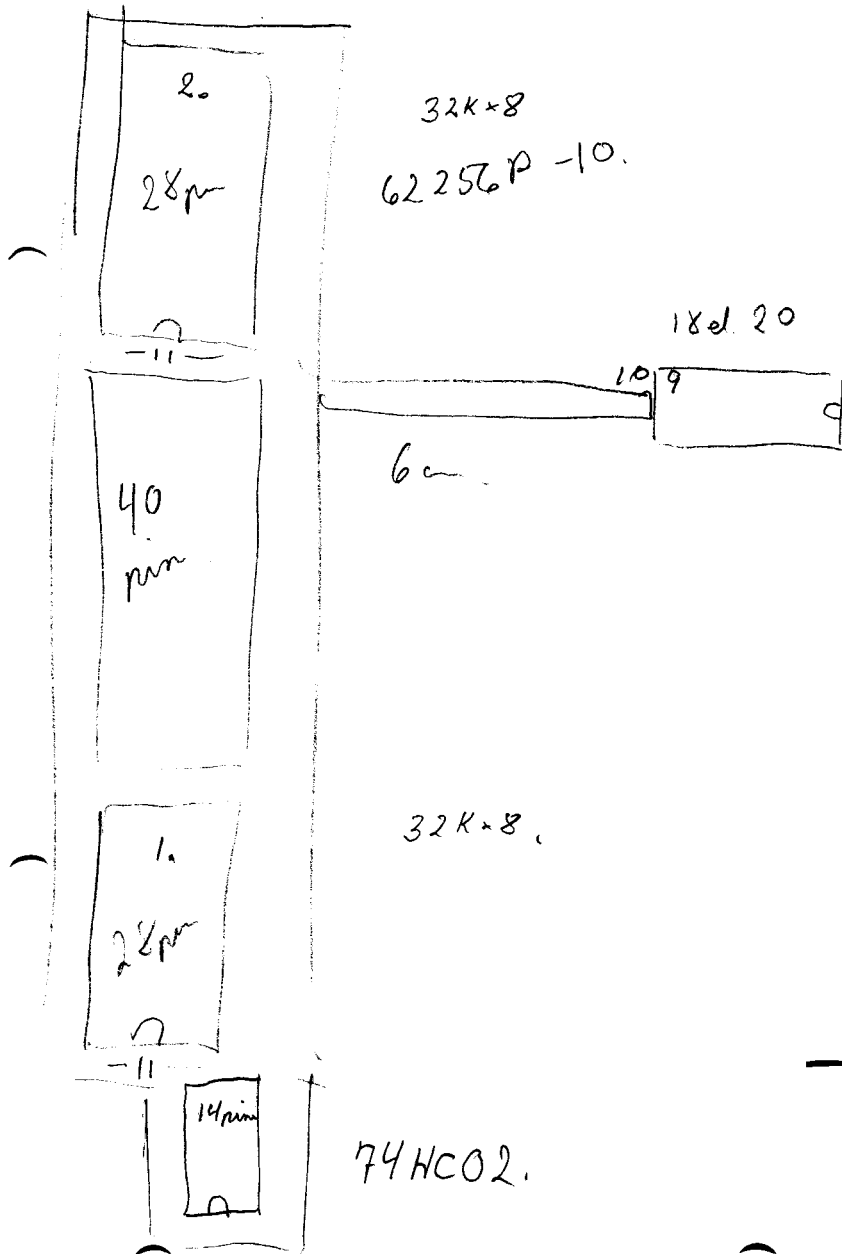
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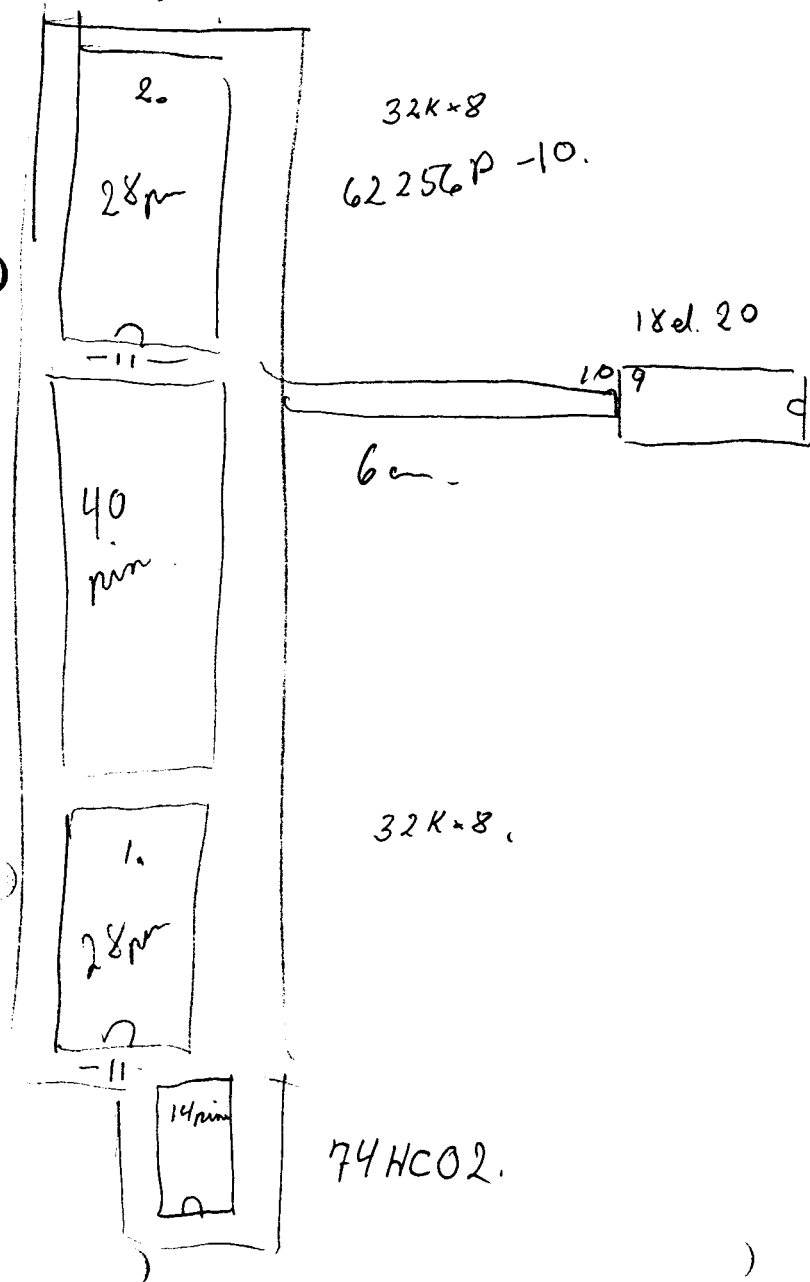


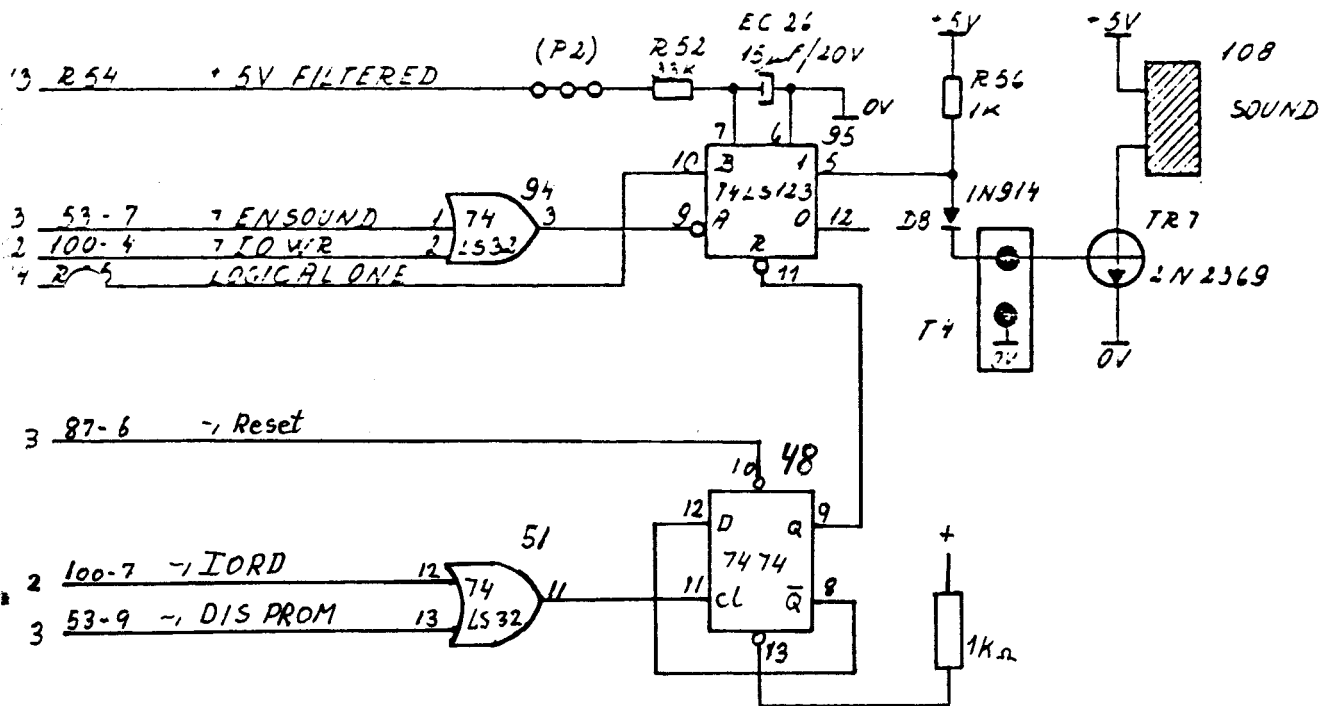
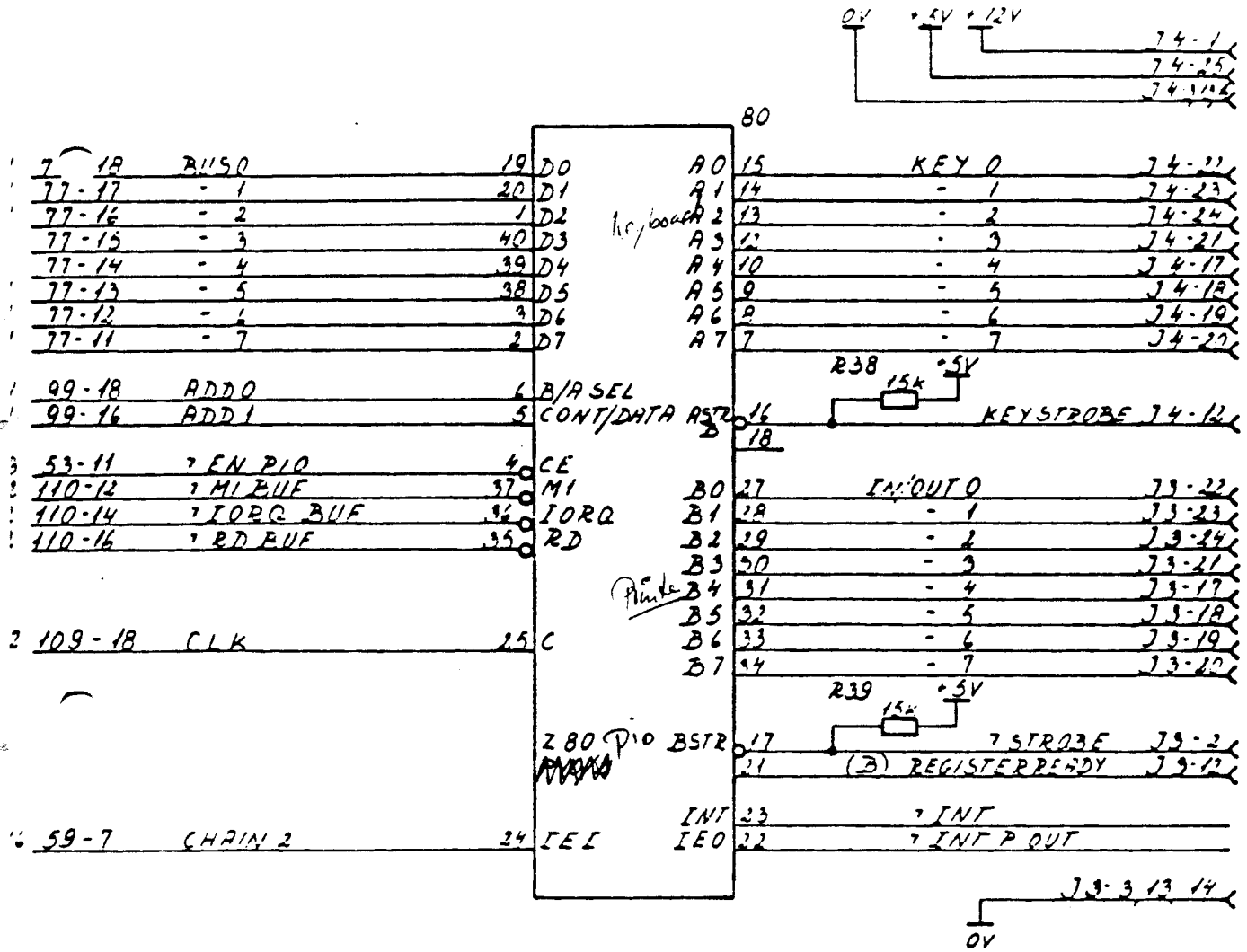
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74 HC 02





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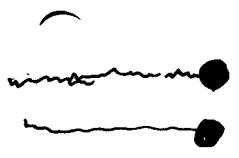
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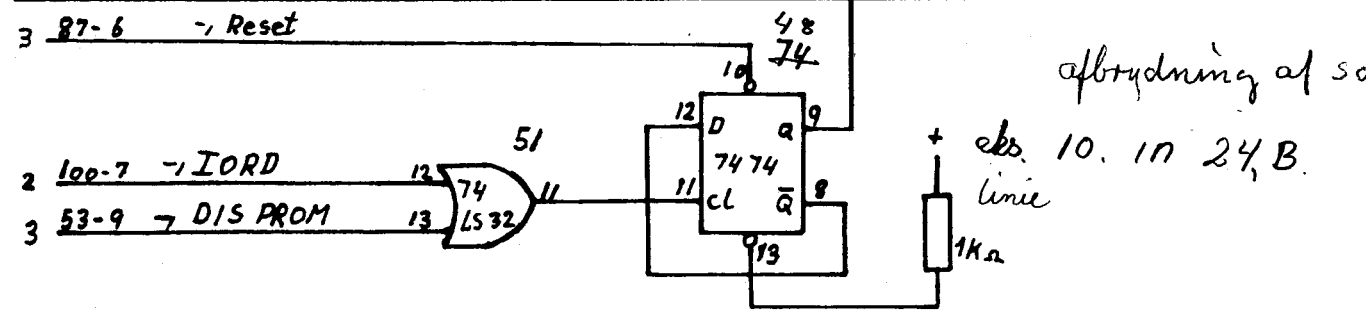
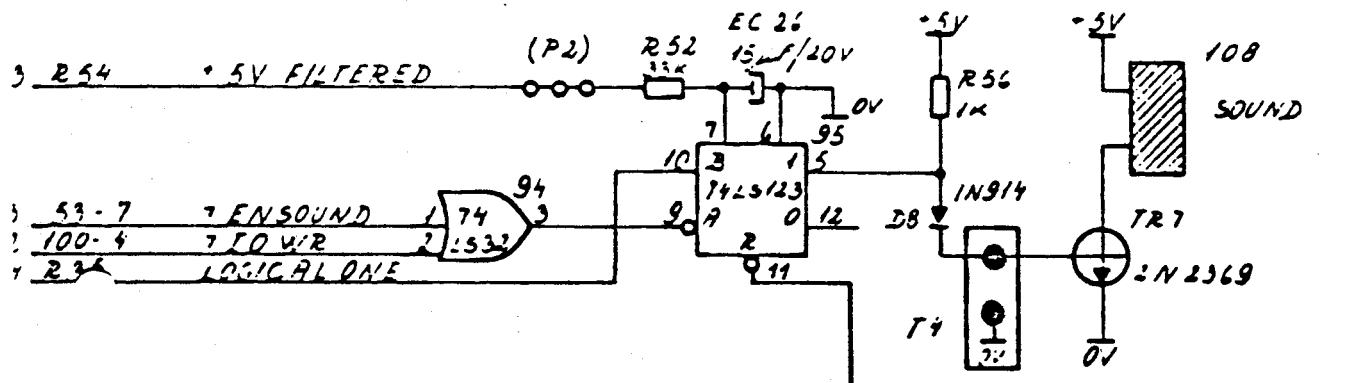
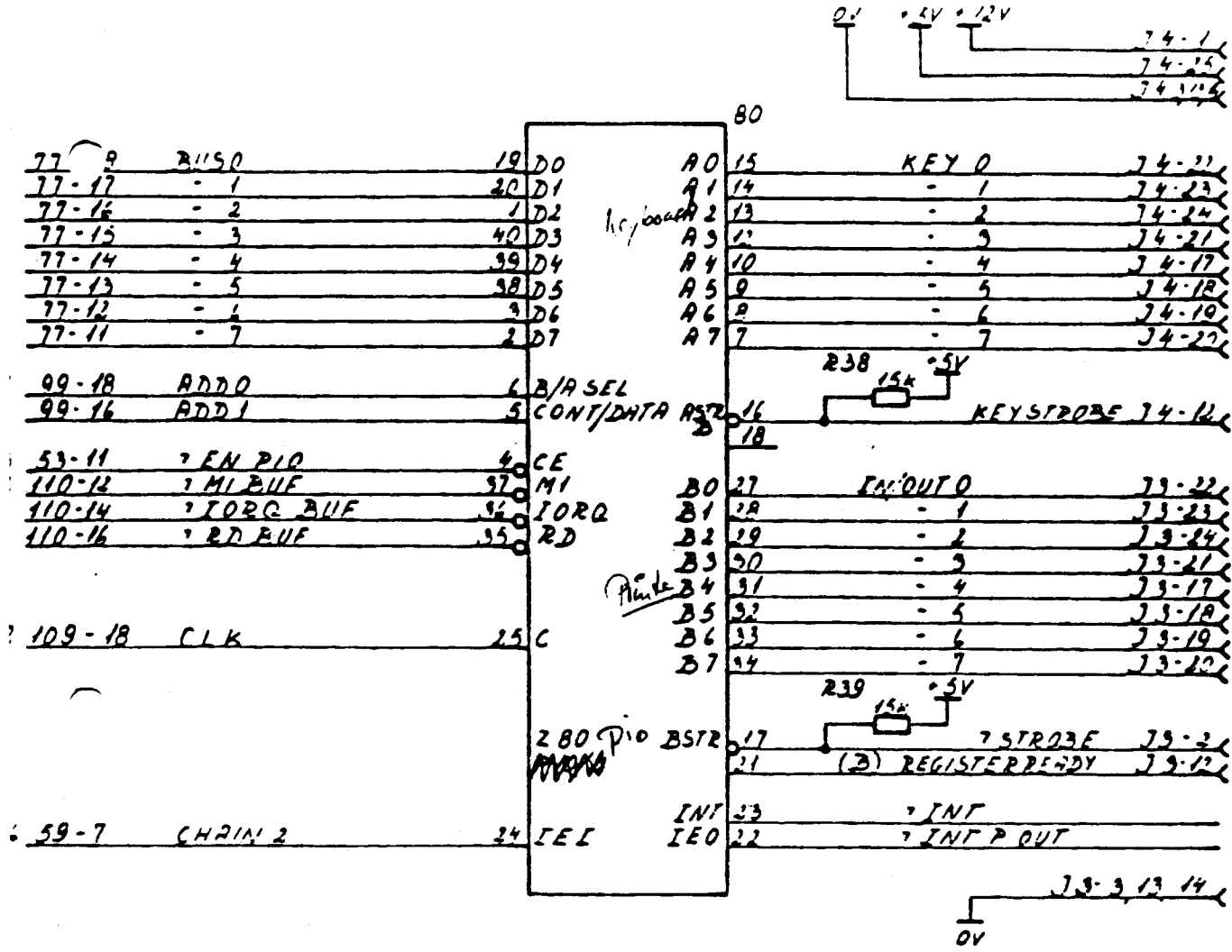
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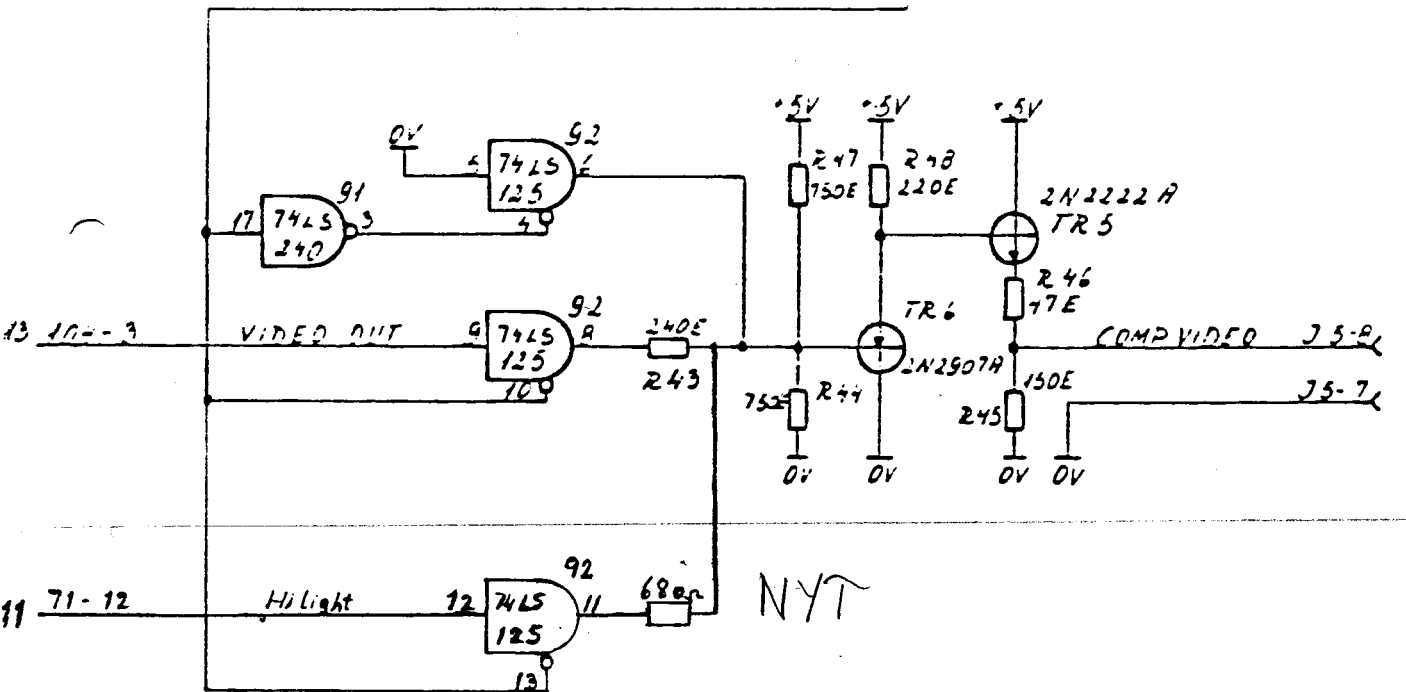
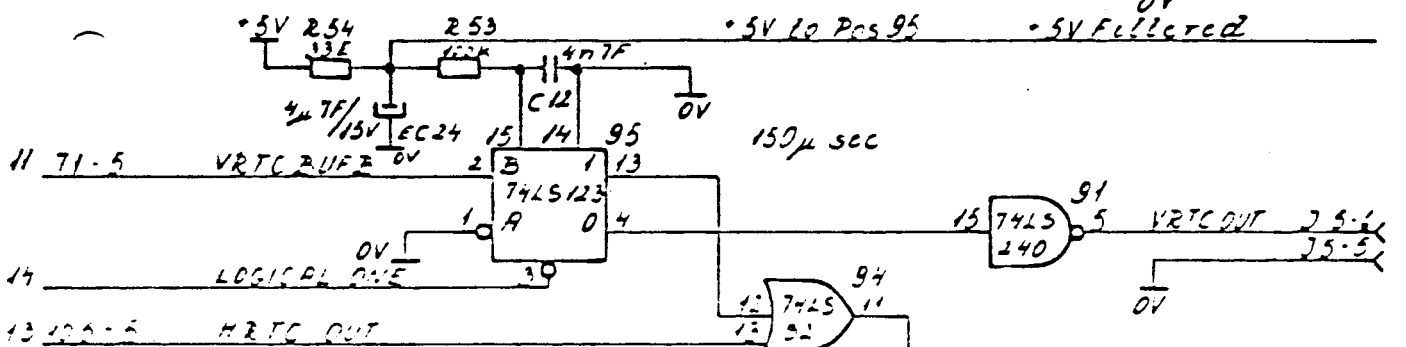
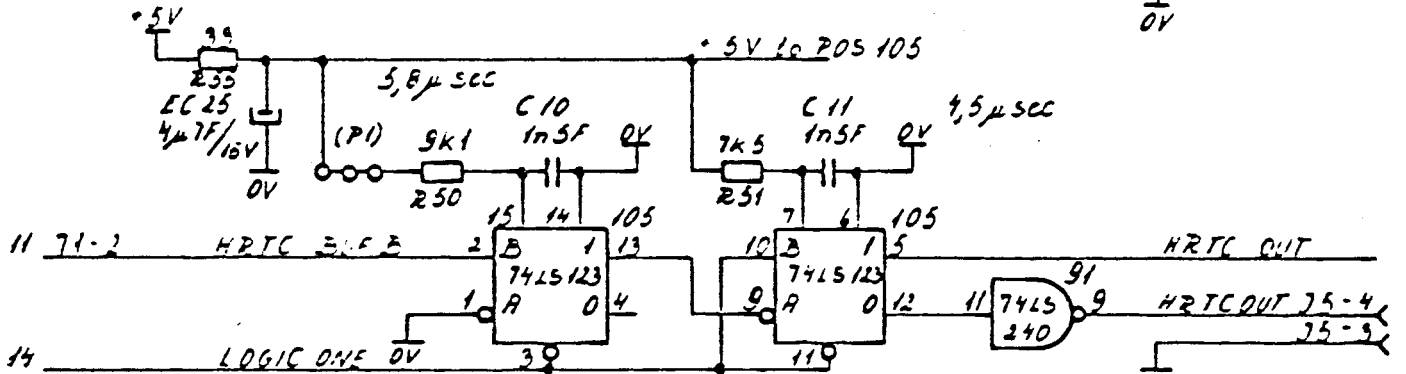
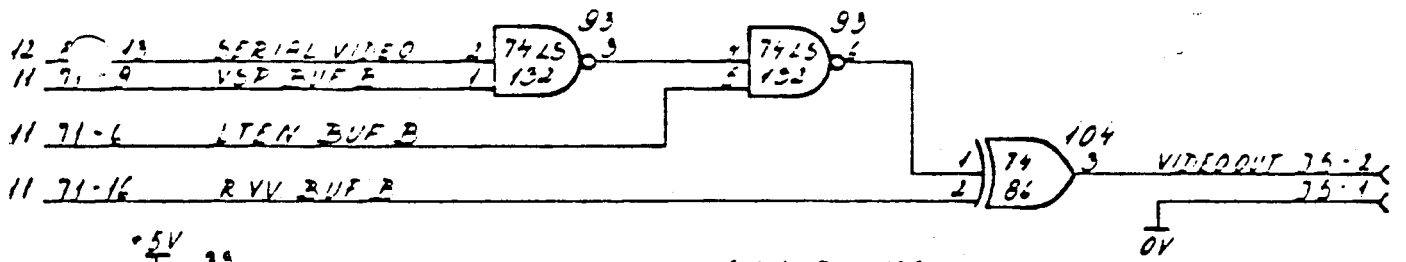
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*MR strap gate ready (closed)

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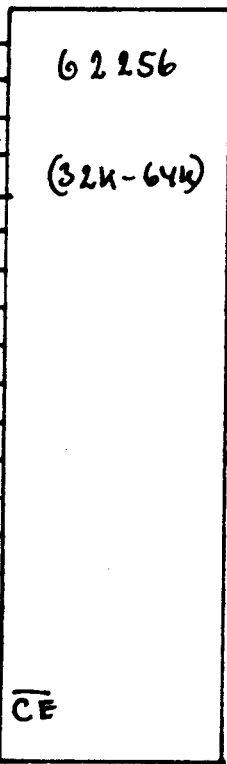
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	6		15	BUS 2
	9	36	14	BUS 3
	12	36	13	BUS 4
	15	36	12	BUS 5
	16	36	11	BUS 6
	19	36	10	BUS 7



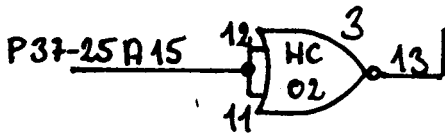


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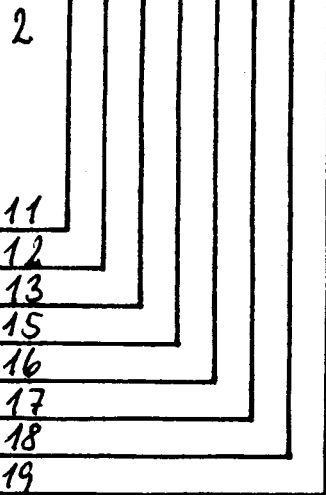
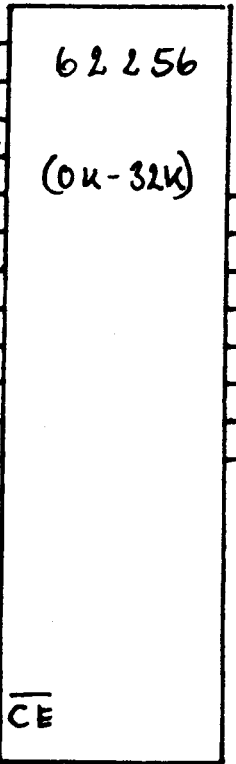
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P37-8	ADD 1	9
P37-10	ADD 2	8
P37-12	ADD 3	7
P37-14	ADD 4	6
P37-16	ADD 5	5
P37-18	ADD 6	4
P37-5	ADD 7	3
P37-4	ADD 8	25
P37-3	ADD 9	24
P37-2	ADD 10	21
P37-1	ADD 11	23
P37-39	ADD 12	2
P37-38	ADD 13	26
P37-24	ADD 14	1
P37-31	MEM WR	27
1-3-1	RAM RD	22



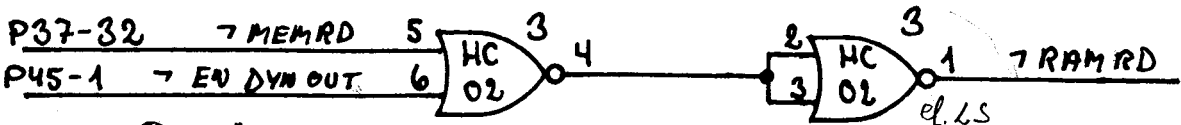
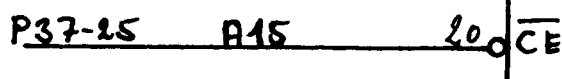
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12	- 1	P45-5
13	- 2	P45-6
15	- 3	P45-9
16	- 4	P45-12
17	- 5	P45-15
18	- 6	P45-16
19	- 7	P45-19



P37-6	ADD 0	10
P37-8	ADD 1	9
P37-10	ADD 2	8
P37-12	ADD 3	7
P37-14	ADD 4	6
P37-16	ADD 5	5
P37-18	ADD 6	4
P37-5	ADD 7	3
P37-4	ADD 8	25
P37-3	ADD 9	24
P37-2	ADD 10	21
P37-1	ADD 11	23
P37-39	ADD 12	2
P37-38	ADD 13	26
P37-24	ADD 14	1
P37-31	MEM WR	27
1-3-1	RAM RD	22



28 VCC
14 GND



P37-30 SACK pin 30 på org logercontroller skal jordes

STATIC RAM FOR PC700

RC * INFO

RC-NYHEDSBORGANET FOR RC-BRUGERE



Micro i system.

PROGRAMMERBAR TENGGENERATOR

Der foregår hele tiden en spændende og vigtig udvikling omkring RC700 - PICCOLO, og megen af den foregår i Århus.

Det sidste, som har set dagens lys, er en programmerbar tegngenerator.

Idéen er simpel, udførelsen enkel - og det virker ...

Initiativet til tegngeneratoren kom, som så mange andre gode initiativer, fra Århus Tandlægehøjskole, og selve "faderen" til RC700 var inddraget i implementationen af den prototype, som man bl. a. kunne se på U'81 i Herning.

Den programmerbare tegngenerator er et lille printkort på ca. 6 x 10 cm med nogle få integrerede kredse. Fra printkortet er der en lille stump kabel, der ender i et stik, som passer til data-bussens stik. På undersiden af printkortet sidder der stik, som svarer til benene på en PROM.

Installationen er meget simpel: man fjerner semigrafik-PROM'nen og placerer printkortet i dens sokkel og forbinder kablet til data-bussen.

Når maskinen tændes, vil de programmerbare tegn have et tilfældigt udseende. Men via et program, kan man sende de ønskede tegn ud over kablet til printkortet, og så vil man kunne bruge disse specielle, selvvalgte tegn også fra andre programmer. De forsvinder først igen, når maskinen slukkes og spændingen forsvinder.



På RC700-PICCOLO er hvert tegn opbygget i et felt på 7 x 11 punkter, og disse punkter kan "tændes" og "slukkes" individuelt, når man opbygger et tegn. Felterne for tegnene når helt sammen, og i princippet får man så en opløselighed på 560 x 254. I praksis kan man dog stadig kun anvende grafikken tegnovis, og det sætter visse begrænsninger, specielt for kurvetegning. Men der er andre områder, hvor denne "tegn for tegn grafik" er glimrende, og i visse tilfælde også normal grafik overlegen m. h. t. hastighed.

Med den programmerbare tegngenerator kan man også lave sine egne nye bogstaver. Har man f. eks. brug for russiske eller græske bogstaver klares det i en håndvending. Man kan selvfølgelig også danne sine egne symboler til f. eks. elektroniske diagrammer, som man bl. a. kunne se i Herning.

Det vil også være muligt at lave tal og bogstaver i overstørrelse til mindre børn, der skal have staveøvelser eller regneøvelser.

Endelig kan man, hvis man har kunstneriske evner (eller evt. erfaringer fra korsstingsbroderi) lave sine egne tegninger af forskellige ting, og så bruge disse tegninger til at sætte liv på undervisningsprogrammer.

Programmerbar tegngenerator

til

RC700 PICCOLO

SEM702

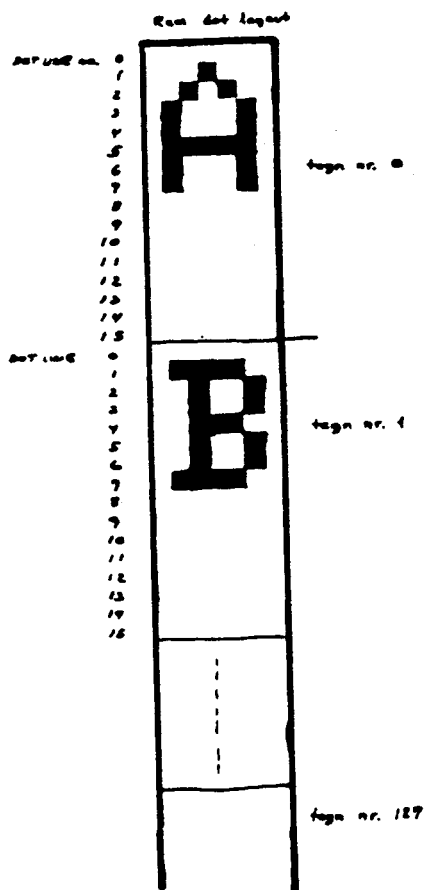
FUNKTIONSBESKRIVELSE

RC702 ("PICCOLO") leveres standard med et fast semigrafisk karakter-sæt, som giver kunden visse grafiske muligheder, men har den ulempe, at den ikke er udskiftbar, d.v.s. den kan ikke kundetilpasses. Det er her, at SEM702 (Semigrafik Memory) kommer ind i billedet.

SEM702 består af et RAM-memory (random access memory), der installeres i stedet for den i RC702 siddende ROM-semigrafik tegngenerator. Indholdet af dette ram memory skrives fra RC702 programmet.

Efter skrivning af semigrafik karakterram, benyttes den som beskrevet i RC702 dokumentation.

Fra programmet har SEM702 følgende layout:



SEM702 programmeres ved hjælp af programmerbare I/O instruktioner fra RC702 programmel (OUT-instruktion i COMAL).

SEM702 benytter 3 I/O adresser:

D1 _H (209 ₁₀)	set tegn værdi (range 0-127)
D2 _H (210 ₁₀)	set dot linie (range 0-15)
D3 _H (211 ₁₀)	ram data

For hvert tegn, der skal programmeres, skrives indholdet ind i RAM'en, én dot linie ad gangen.

Følgende COMAL program eksempel sætter tegnværdi 32-38:

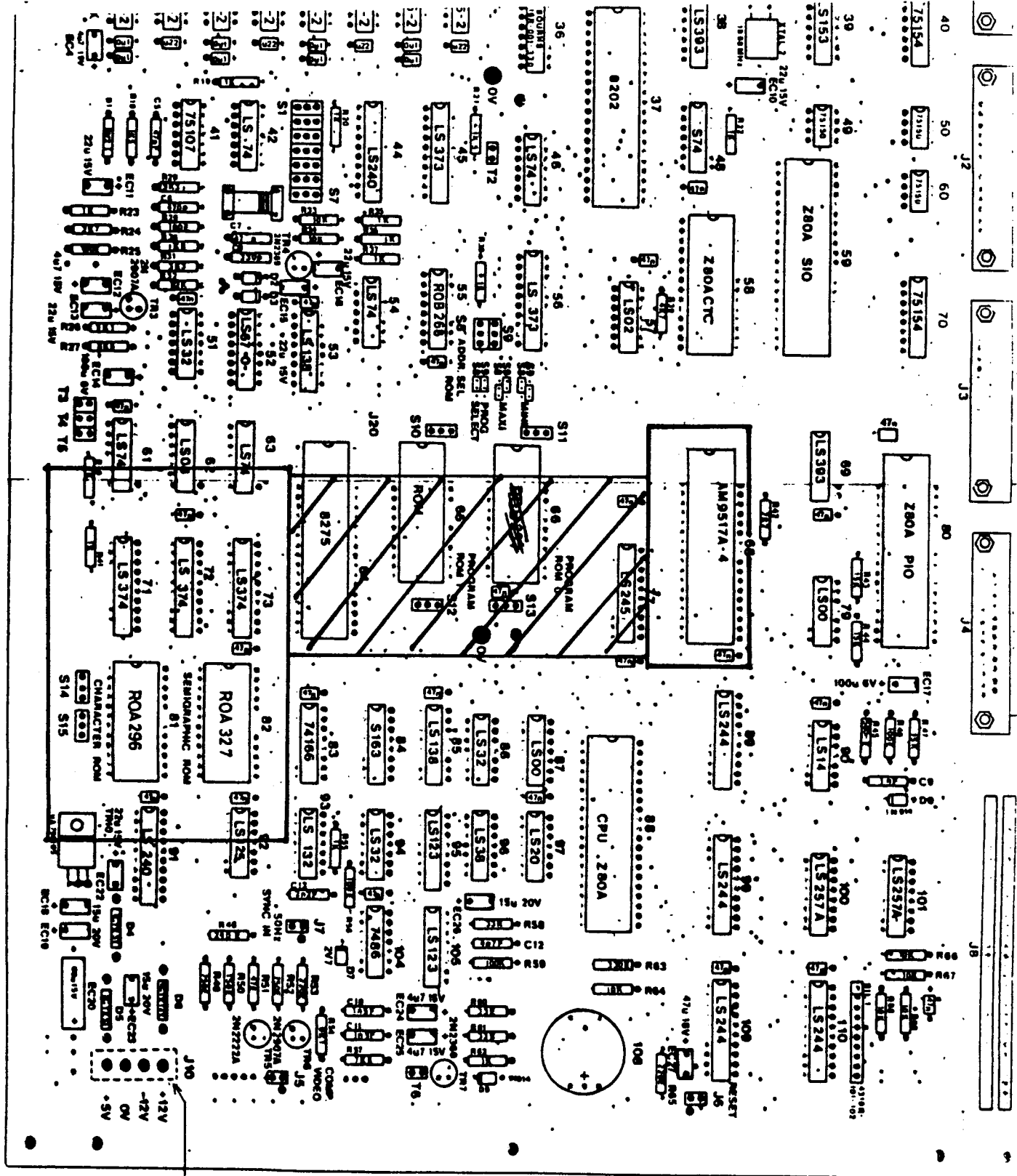
```

REM    SEM702 eksempel
10  ACHAR = 209; ALINE = 210; AWR = 211
20  restore
30  for char = 32 to 38
40      out achar, char
50      for line = 0 to 10
60          out aline, line
70          read val
80          out awr, val
90          next line
100 next char
110 end
120 data 0,0,0,0,0,0,0,0,0,0,0
130 data 0,8,8,8,8,8,0,8,0,0,0
140 data 0,20,20,20,0,0,0,0,0,0,0
150 data 0,20,20,54,0,54,20,20,0,0,0
160 data 0,8,28,10,28,40,30,8,0,0,0
170 data 0,38,38,16,8,4,50,50,0,0,0
180 data 0,4,10,10,4,42,18,44,0,0,0

```

INSTALLATIONVEDLEDNING TIL SEM7o2

-
1. Fjern topdæksel på rc7o2.
 2. Fjern ic68(AM9517-4). Dette gøres forsigtigt ved at løfte ic'en med en skruetrækker fra hver side. På fig 1 er vist placeringen af ic68.
 3. Fjern ic82(roa327). Der benyttes samme fremgangsmåde som under punkt 2.
 4. Sem7o2 består af 2 printkort, som vist på fig2.
 5. Det store print orienteres som vist på fig2, og trykkes ned i ic82. Vær omhyggelig med at pindene kommer ordentlig ned i ic82.
 6. Det lille print isættes ic68. Bemærk orienteringen af printet.
 7. Den under punkt 2 afmonterede ic sættes ned over det lille print...

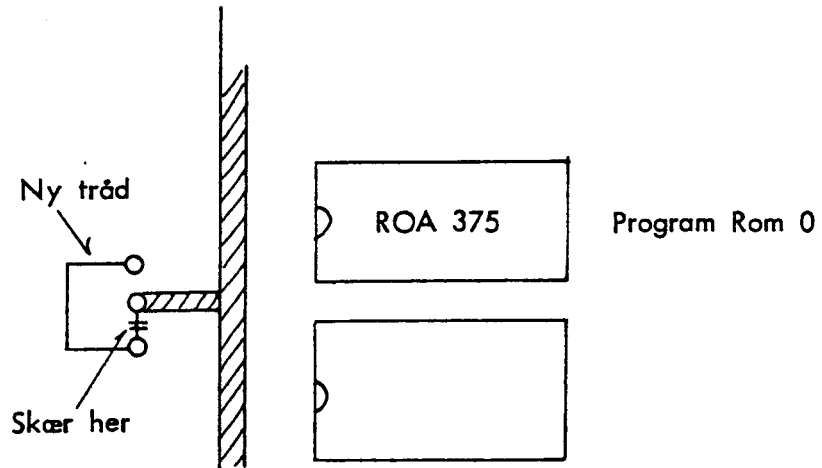


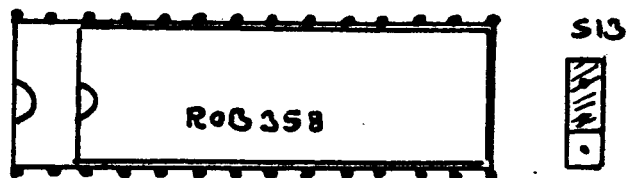
310
 MONTAGES FRA
 LODDESIDEN
 FIG 2.

BETEGNELSE		UDGAVE	
MONTINGSTEGNING PCB 595		02	820818HC
		03	820903HC
PA PART NR	PA TEKN PART NR	04	
DESIGN HC		05	
01 UDGAVE 820623	MONTAGE	06	
		TEKN NR.	
		MIC 704-00	

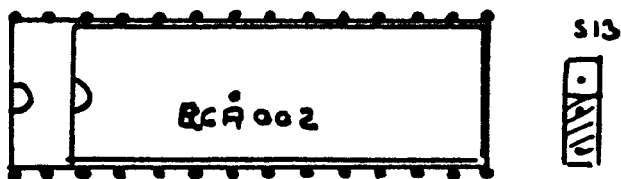
INSTALLATION AF NY BOOTER ROM I RC702.

1. Udskift ROA 375 (IC66) med RGÅ001.
2. Skær printbane som vist neden for.
3. Læg ny tråd som vist neden for.



Installation of booter-rom EGA002 i RC702 (m. nyt MIC-print)

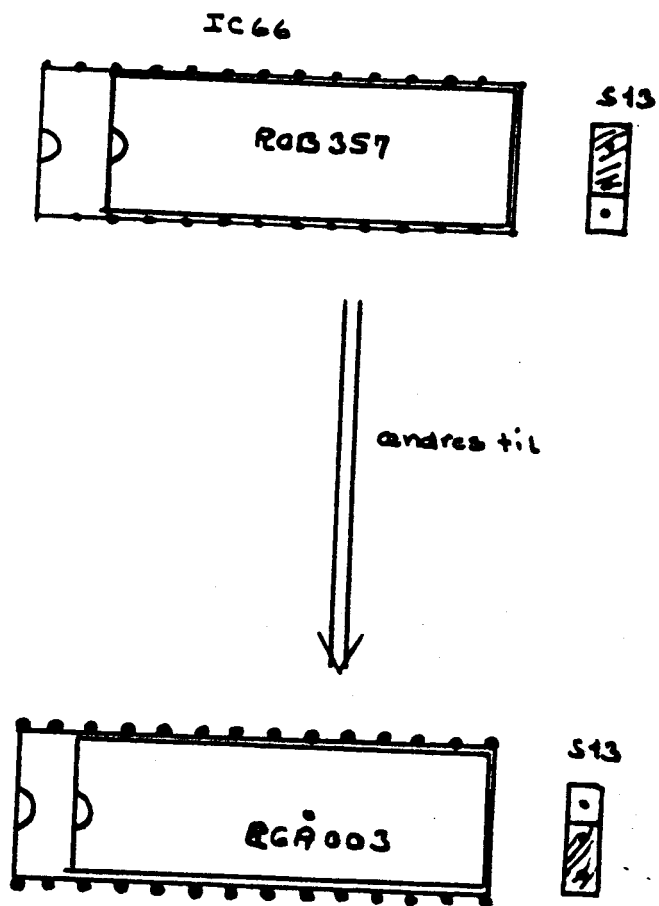
ändres til



1. ROB 358 erstattes med EGA002.
2. S13 flyttes som vist.

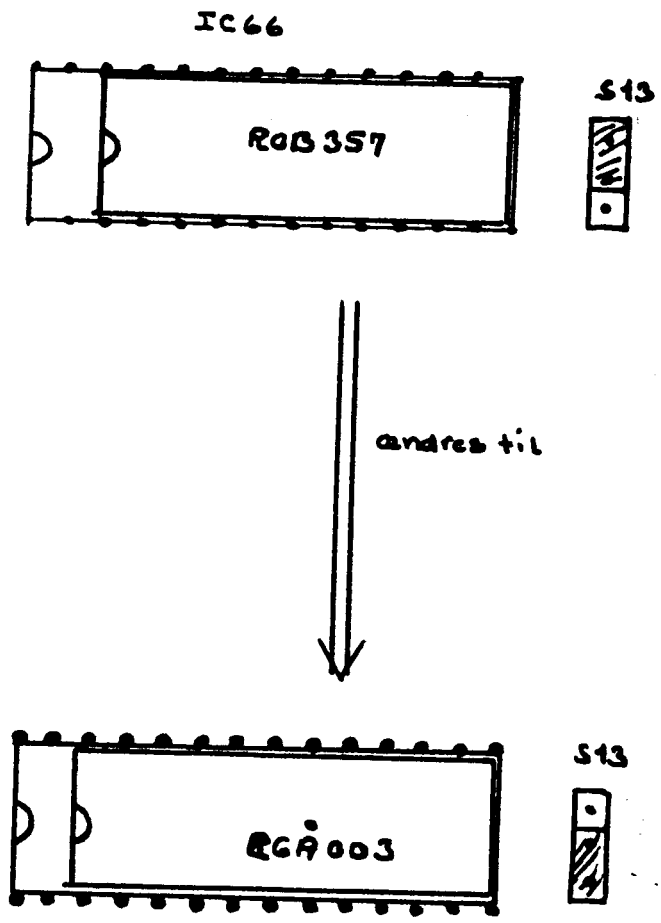
1983.12.05

INSTALLATION af booter-rom EGA003 i RC703



1. ROB357 erstattes med EGA003.
2. S13 flyttes som vist.

INSTALLATION af booter-rom RGA003 i RC703



1. ROB357 erstattes med RGA003.
2. S13 flyttes som vist.

RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input checked="" type="checkbox"/>	NON WARRANTY	<input type="checkbox"/>

PAGE	1	OF	1
RE: ECN NO:	19-002		

SERIAL EFFECTIVITY MIC 702/ 453 and upwards.	EQUIPMENT AFFECTED RC 700 RC 702 / MIC 702 Microprocessor.
NOTE	

REASON FOR CHANGE

To be shure that the drivers, between the floppy disc controller and the floppydisc driv are able to supply enough current to drive the the receivers effectively, the drivers are changed from SN 74LS240 to SN 74S240. And to ensure a correct clock pulse to the floppy disc controller the IC in pos. 27 is changed from SN 74LS157N to SN 74157N.

DESCRIPTION OF CHANGE

1. Change the SN 74LS240 in pos. 8 and pos. 18 to SN74S240.
2. Change the SN 74LS157 in pos. 27 to SN 74157.
3. Code the FCO-label: 19-002.

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: _____
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE	YES <input type="checkbox"/>	NO <input checked="" type="checkbox"/>
---------------------	------------------------------	--

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
2	SN 74S240	
1	SN 74157	

DOCUMENTATION ENCLOSED

None

ESTIMATED INSTALLATION TIME: 1.0 hour.

PROJECT ENGINEER SIGN. <i>M. B. Pedersen</i>	DATE <i>5/10/81</i>	DEVELOPMENT MANAGER SIGN. <i>Henrik Rouse</i>	DATE <i>5/13/81</i>	SYS. PRODUCTION MANAGER SIGN. <i>[Signature]</i>	DATE <i>4/28/81</i>	TECH. SERVICE MANAGER SIGN. <i>[Signature]</i>	DATE <i>[Signature]</i>
--	---------------------	---	---------------------	--	---------------------	--	-------------------------

RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input type="checkbox"/>	NON WARRANTY	<input checked="" type="checkbox"/>

PAGE	1	OF	2
RE: ECN NO:	19-003		

SERIAL EFFECTIVITY	EQUIPMENT AFFECTED
MIC 702/ 453 and upwards.	RC 700 RC 702 / MIC 702 Microprocessor.
NOTE	

REASON FOR CHANGE

To be shure that write data from the floppy disc controller, are clocked correctly into the preformatting register, the clock input to this register is changed from the signal " 8 MHz to "78MHz ".

DESCRIPTION OF CHANGE

- Cut the wire on the komponent side of the MIC 702 or MIC 703 PCBA, as shown on page 2.
- Insert a wire from pos. 28 pin 4 to pos. 5 pin 9. The wire is soldered on komponent side near pos. 5, and routed through a hole in the board near pos. 28, as shown on page 2.
- Code the FCO-label: 19-003.

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: _____
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE YES NO

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
0.1m	Mini Wrap Wire	4-4910

DOCUMENTATION ENCLOSED

None

ESTIMATED INSTALLATION TIME: 0.5 hour

PROJECT ENGINEER		DEVELOPMENT MANAGER		SYS. PRODUCTION MANAGER		TECH. SERVICE MANAGER	
SIGN.	DATE	SIGN.	DATE	SIGN.	DATE	SIGN.	DATE
M. Pedersen	30/4 81	[Signature]	1/5-81	[Signature]	31.05.81	[Signature]	AS/S

RCSL: 44 - RT 1911

MANDATORY <input type="checkbox"/>	RETROFIT ON FAILURE <input checked="" type="checkbox"/>
WARRANTY <input type="checkbox"/>	NON WARRANTY <input checked="" type="checkbox"/>

PAGE 1	OF 2
RE: ECN NO: 19-004	

SERIAL EFFECTIVITY

MIC 703/1001 and upwards

EQUIPMENT AFFECTED

RC 700
RC 702 / MIC 702 and MIC 703
Microprocessor.

NOTE

REASON FOR CHANGE

The MEM CLOCK oscillator has caused problems in the production, which has been solved by changing the transistor or the Xtal. In case of such problem change of two capacitors is the correct solution.

DESCRIPTION OF CHANGE

- Change C 3 from 4.7 pF to 33 pF. (see page 2)
- Change C 1 from 68 pF to 330 pF. (see page 2)
- Code the FCO-label: 19-004.

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: _____
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE YES NO

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
1	Capacitor 33pF	0802018
1	Capacitor 330pF	08102033

DOCUMENTATION ENCLOSED

None

ESTIMATED INSTALLATION TIME: 1.0 hour.

PROJECT ENGINEER SIGN. <i>M. G. Pedersen</i>	DATE 3/14 81	DEVELOPMENT MANAGER SIGN. <i>[Signature]</i>	DATE 1/581	SYS. PRODUCTION MANAGER SIGN. <i>[Signature]</i>	DATE 1/581	TECH. SERVICE MANAGER SIGN. <i>[Signature]</i>	DATE 1/581
---	-----------------	---	---------------	---	---------------	---	---------------

RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input type="checkbox"/>	NON WARRANTY	<input checked="" type="checkbox"/>

PAGE	1	OF	2
RE: ECN NO:	11-069		

SERIAL EFFECTIVITY

UNITS SHIPPED AFTER 10-12-1980

NOTE

EQUIPMENT AFFECTED

RC700

RC 702/MIC 702

MICROPROCESSOR

REASON FOR CHANGE

CURRENT IN THE 0 VOLT WIRE FOR THE "SYNC" SIGNAL FROM REC 701 to MIC 702, CAN INTRODUCE NOISE IN SECOND MINI FLOPPY DRIVE IN RC 702.

DESCRIPTION OF CHANGE

1. DISCONNECT THE 0 VOLT WIRE BY CUTTING 10 MM OUT AS SHOWN ON PAGE 2.
2. ISOLATE WITH FLEX.
3. CODE THE FCO LABEL 19-005.

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: _____ ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE YES NO

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
20 MM	FLEX, CRIMP	

DOCUMENTATION ENCLOSED

NONE

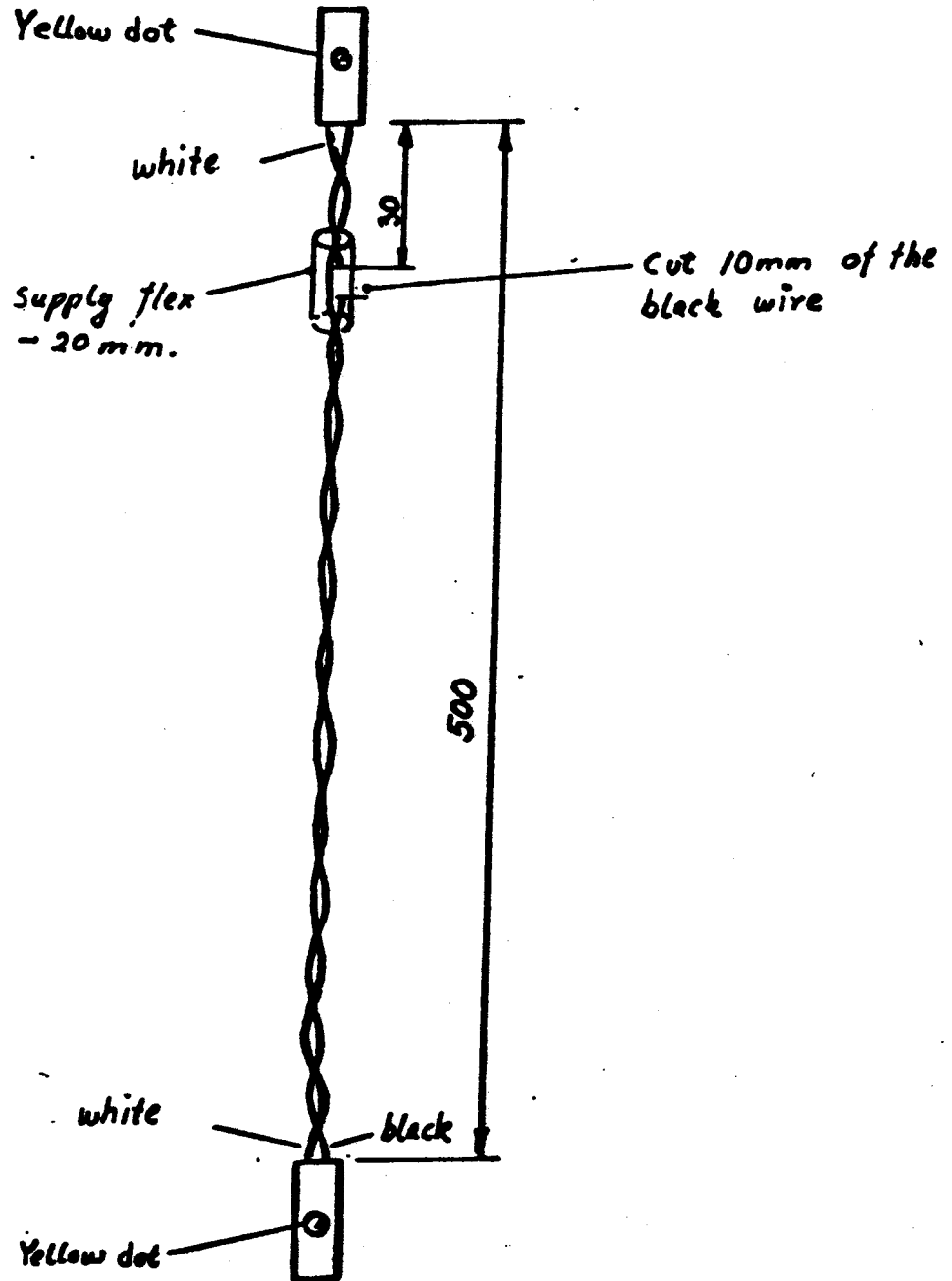
ESTIMATED INSTALLATION TIME: 0,5 HOURS

PROJECT ENGINEER SIGN. <i>MVPedersen</i> DATE <i>25/5-81</i>	DEVELOPMENT MANAGER SIGN. <i>[Signature]</i> DATE <i>25/5-81</i>	SYS. PRODUCTION MANAGER SIGN. <i>[Signature]</i> DATE <i>2/6-81</i>	TECH. SERVICE MANAGER SIGN. <i>[Signature]</i> DATE <i>2/6-81</i>
---	---	--	--

FIELD CHANGE ORDER

NO. 19-005

PAGE 2 OF 2



HEA, APL

TOPIC: C-024

YOUR REF.

OUR REF. LEB/GBA

DATE 21st December, 1981

Dear Sirs,

"Bad Sectors" on Floppy Discs in the RC 700-System

Lately we have found that the use of "Dual Density" on the Mini - as well as the Maxi Floppy Discs in the RC 700-Systems may cause "Bad Sectors".

To ensure a safe operation in Dual Density a New Field Change Order (FCO 19-008) will be released. The implementation of this FCO together with FCO 19-009 will ensure a safe operation.

The kit for FCO 19-008 consists of a "Satellite print", DSP 701, a small cable, CBL 980, and some tape. The "satellite print" is to be installed in IC Pos. 7 and Pos. 17 (see fig. 1). The Print consists of a new Data Separator Circuit for the Floppy Disc Controller (see fig. 2 and 3).

The production of the FCO-kits is rather expensive, for which reason we kindly ask you to inform us of the number of kits needed in your area as soon as possible.

A limited number of the FCO-kits will be available in January 1982.

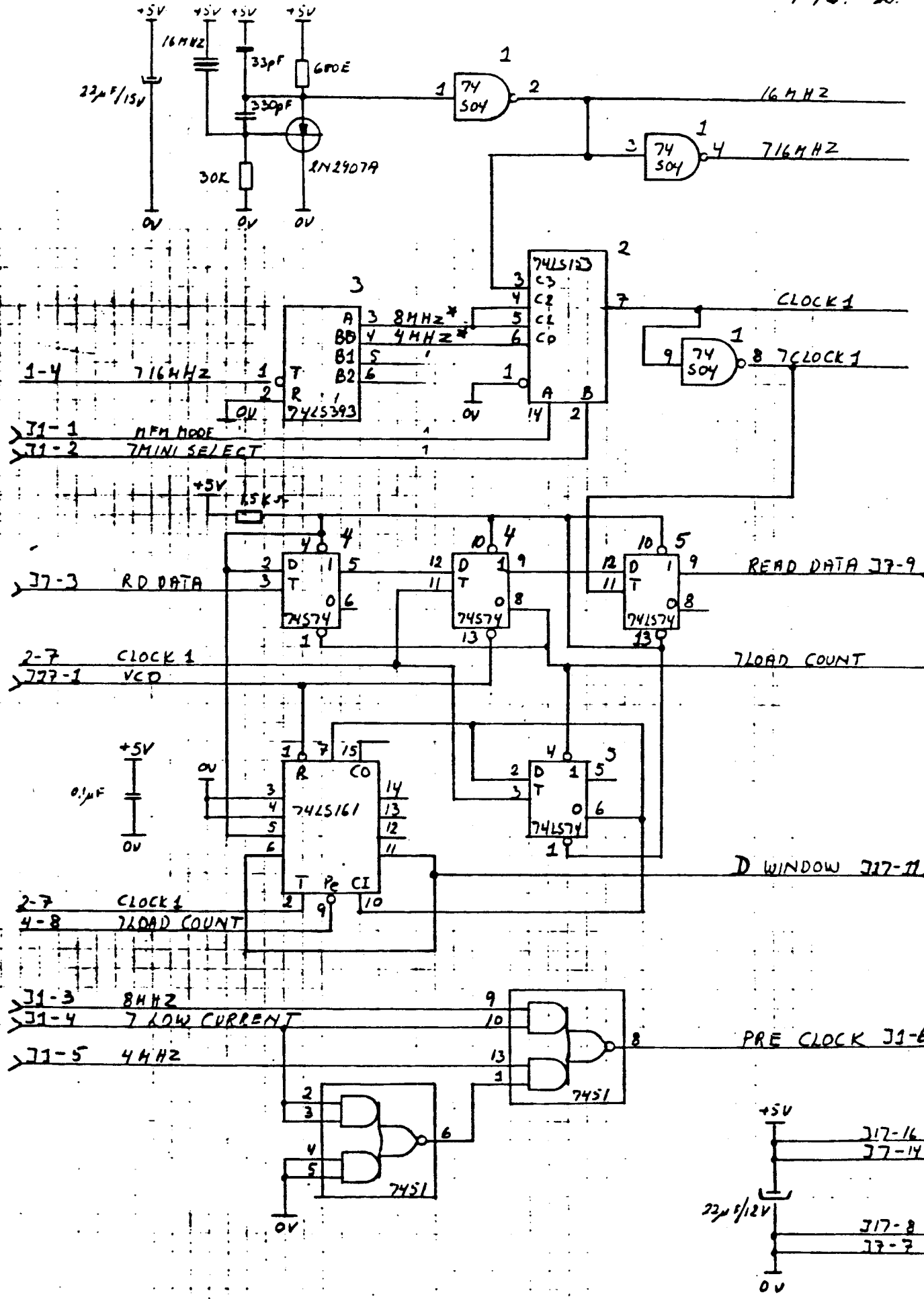
Best regards,
RC COMPUTER A/S



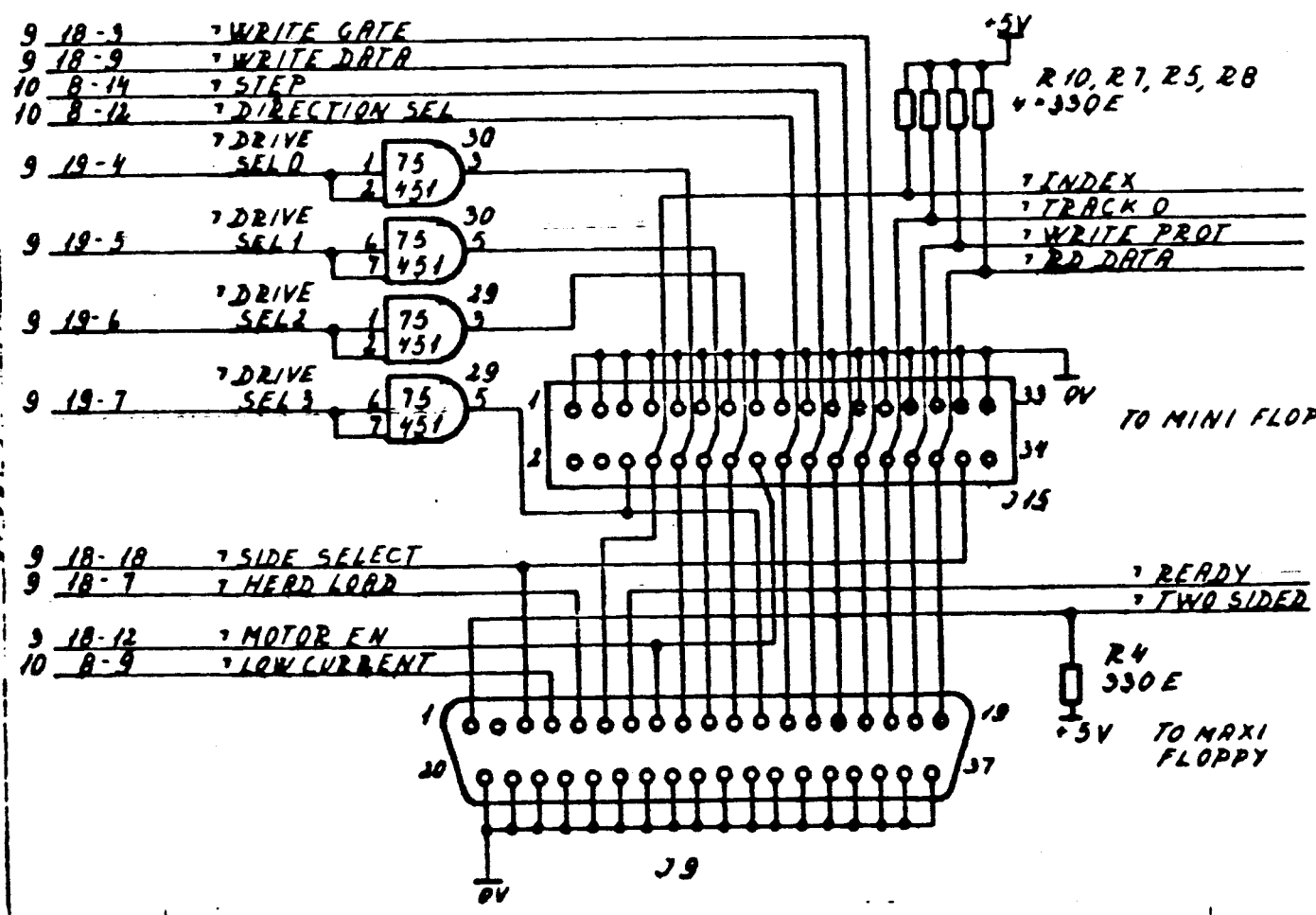
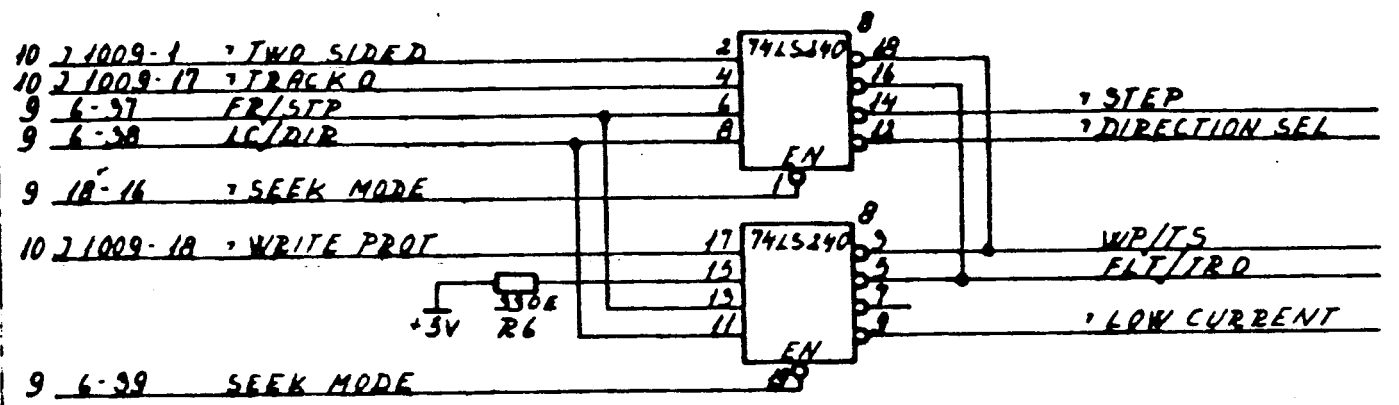
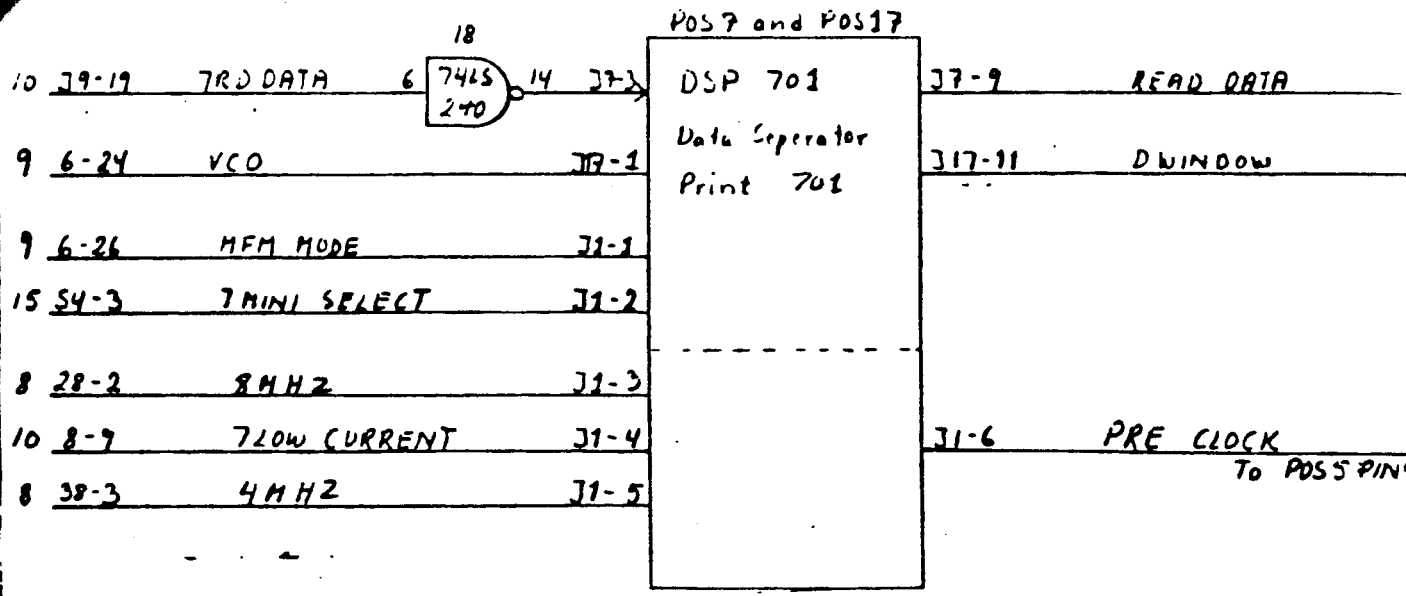
Leif Braae
International Technical Service

Encl.: fig. 1, DSP 701 Mounted on MIC 703,
fig. 2, Data Separator Print DSP 701,
fig. 3, Floppy Disc Read & Select Circuit

FIG. 2.



Approved by Desig. No. _____
 due to ECN _____
 Replaces Desig. No. _____
 Design-Check _____
 Drawn by _____
 Designed by _____
A/S RECENTRALEN



MVP RGA 80.08.14

MIC 702
R.19086

FLOPPY DISK READ & SELECT CIRCUIT

MIC 10

RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input checked="" type="checkbox"/>	NON WARRANTY	<input type="checkbox"/>

PAGE	1	OF	3
RE: ECN NO:			

SERIAL EFFECTIVITY MIC 703, SN 1305 and upwards	EQUIPMENT AFFECTED RC700 RC702/MIC 703 Micro Processor
--	---

NOTE

REASON FOR CHANGE

Due to electromagnetic interference from the power supply, an unacceptable high frequency of soft-errors is experienced, when utilizing double density mode on mini floppy drive in pos. 2.

The object of this FCO is to improve the data recovery circuit, thus reducing the failure rate.

DESCRIPTION OF CHANGE

1. Remove the IC's in POS 7 and POS 17.
2. Mount the PCBA DSP701 as showed on FIG 1.
3. Mount the signal cable CBL 980 as described page 2.
4. Code the FCO label 19-008.

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK UNDER RC-PARTNUMBER: 8-0908
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE YES NO

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
1	PCBA DSP 701	
1	CABLE CBL 980	
2,5CM	"SKILTETAPE"	3810010

DOCUMENTATION ENCLOSED

2 pages of preliminary diagrams

ESTIMATED INSTALLATION TIME: 2,0 h

PROJECT ENGINEER SIGN.	DATE	DEVELOPMENT MANAGER SIGN.	DATE	SYS. PRODUCTION MANAGER SIGN.	DATE	TECH. SERVICE MANAGER SIGN.	DATE
<i>[Signature]</i>	8/2/82	<i>[Signature]</i>		<i>[Signature]</i>	27/1/82	<i>[Signature]</i>	27/1/82



FIELD CHANGE ORDER

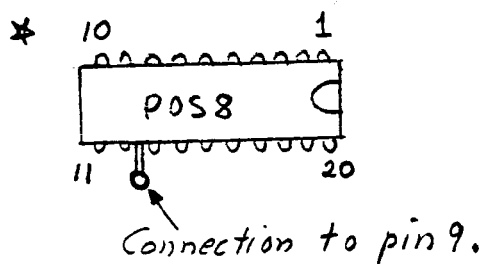
NO. 19-008

PAGE 2 OF

Remove the wire from POS 28 PIN 4 to POS 5 PIN 9.

CONNECT CBL 980 AS FOLLOWS:

1. J1 - PIN 1 TO POS 26 PIN 1
2. J1 - PIN 2 TO POS 27 PIN 1
3. J1 - PIN 3 TO POS 27 PIN 13
4. J1 - PIN 4 TO POS 8 PIN 9 *
5. J1 - PIN 5 TO POS 27 PIN 10
6. J1 - PIN 6 TO POS 5 PIN 9





FIELD CHANGE ORDER

NO. 19-008

PAGE 3 OF

Fixed with double stick tape

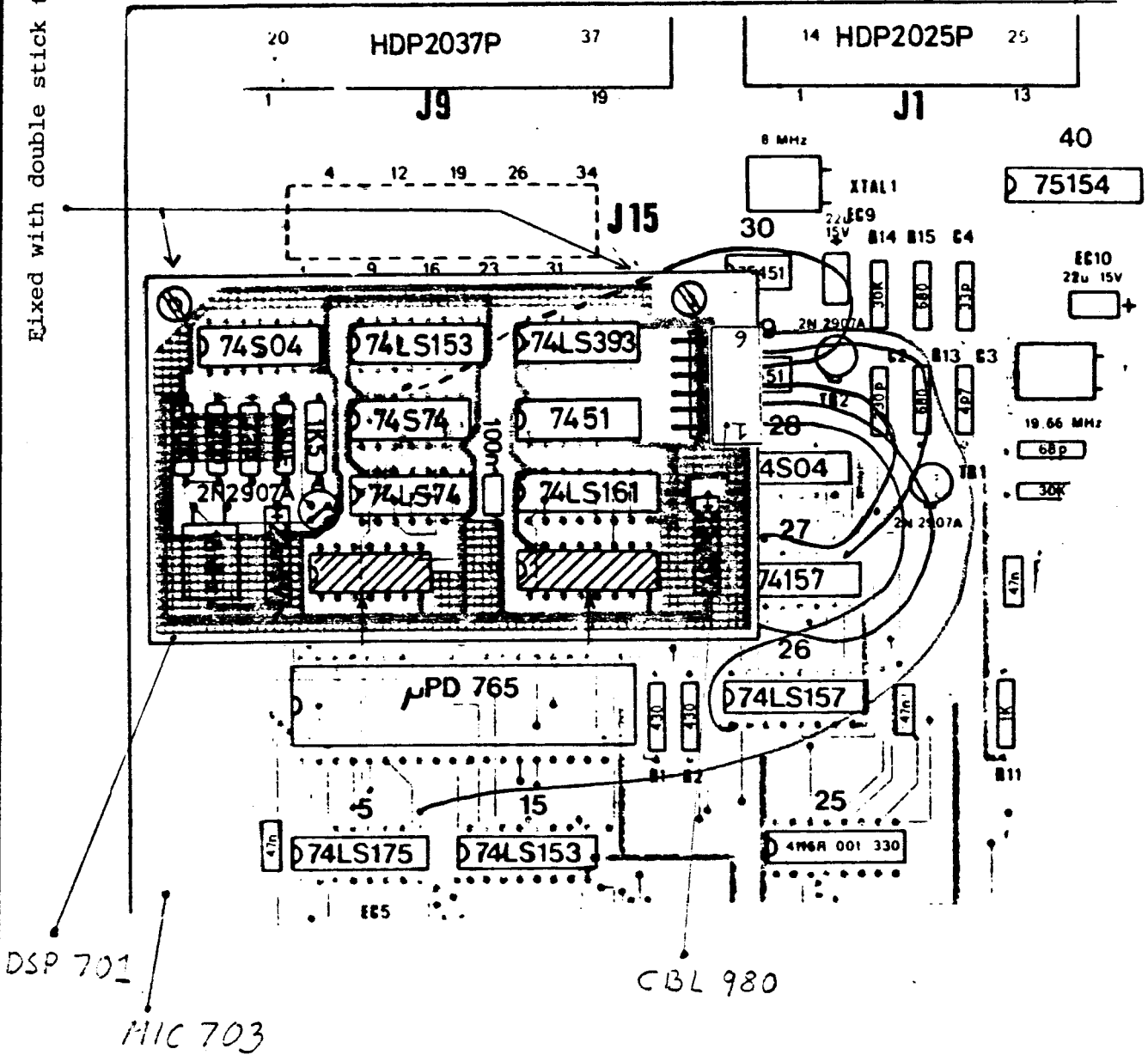
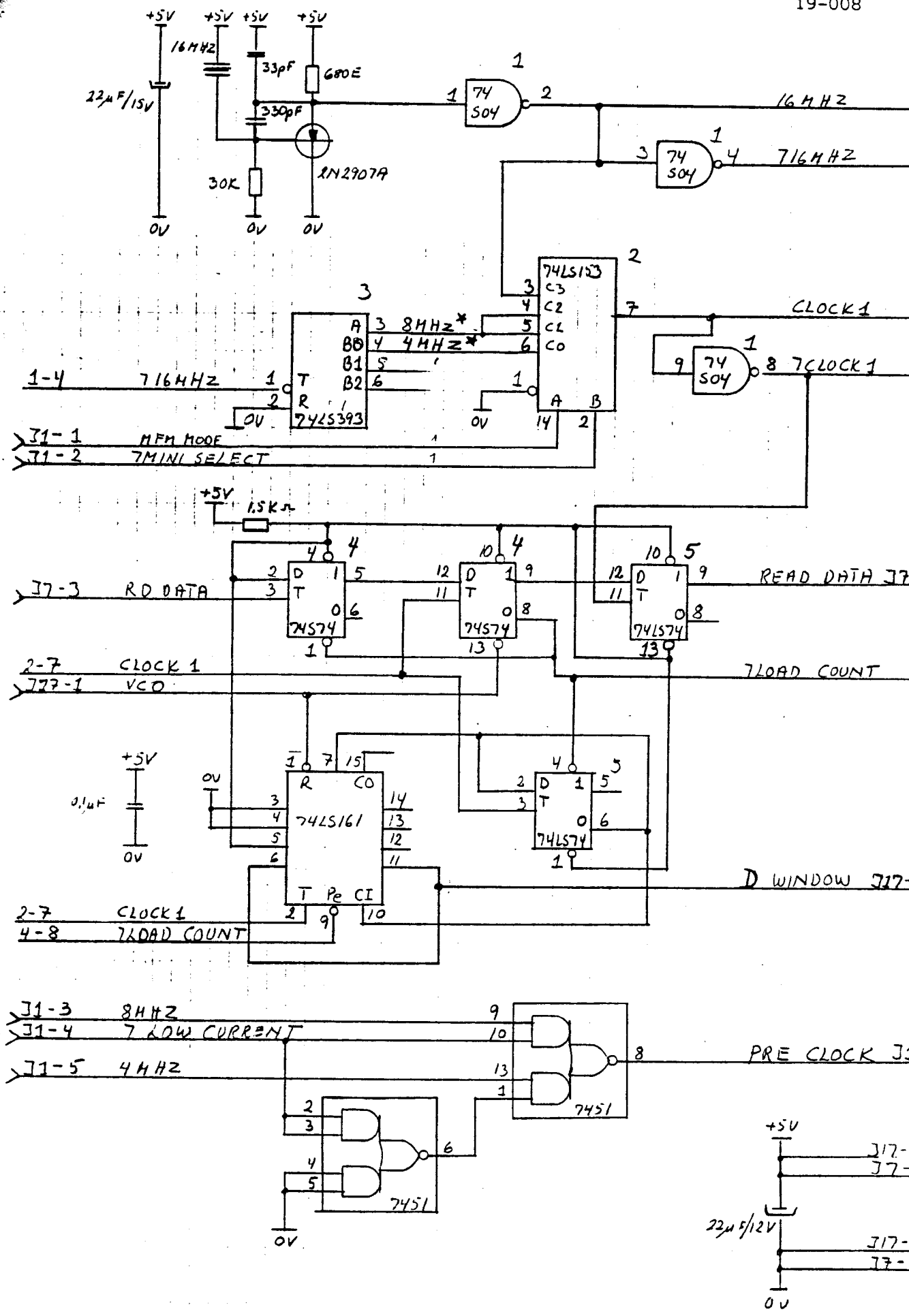


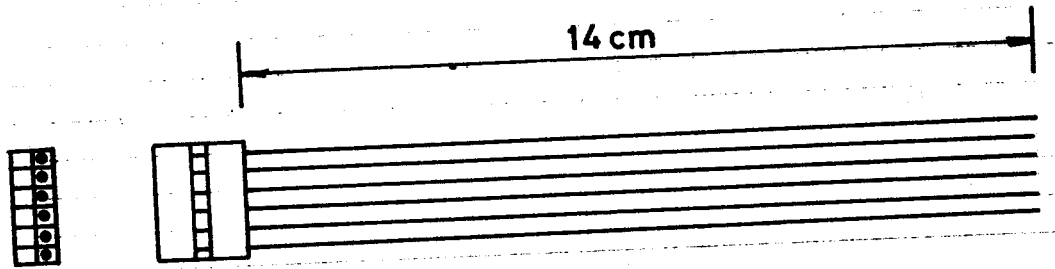
Fig. 1. DSP 701 Mounted on MIC 703.



by Dwg. No. _____
 Replaces Dwg. No. _____
 Design Check _____
 Dwg. Off. _____
 Drawn by _____
 Designed by _____
NTRALEN
A/S REG

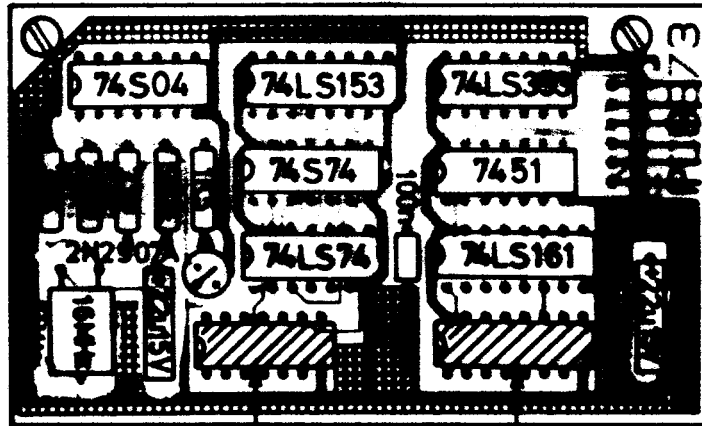
Unit	DATA SEPERATOR PRINT DSP701	
Dwg. No.		

AC: 008 VB 14C

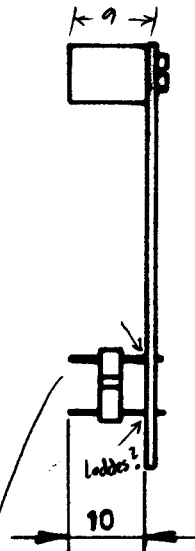


BETEGNELSE		UDGAVE	
SIGNAL CABLE FOR DSP701		02	07
		03	08
		04	09
		05	10
		06	11
PA PART NR.	PA TEKN. PART NR.	TEGN NR.	
DESIGN	HC	E	CBL 980-
01 UDGAVE	811209		
MONTAGE			

AFSTANDSSTYKKE
DSP701-001



14 PINS ADAPTER & 16 PINS ADAPTER
MONTERES FRA LODDESIDEN.



max. 0.46

BETEGNELSE		UDGAVE	
MONTERINGSTEGNING PCB 573		02	07
		03	08
		04	09
PA PART NR.		05	10
PA TEGN PART NR		06	11
DESIGN	HC	TEGN NR	
01 UDGAVE	811204	DSP 701-002	
MONTAGE			

ANTAL	ENHED	MODUL NR.	PA PART NR.	DOK. / TEGN. NR.	BETEGNELSE
1					UHONTERET PRINTKORT PCB 573
1			1010107		IC: 7451
1			125003		IC: 74504
1			125013		IC: 74574
1			128027		IC: 74LS74
1			128038		IC: 74LS153
1			128046		IC: 74LS161
1			128088		IC: 74LS393
4			203015		TRANSISTOR 2N2907A
2			1001004		TANTAL 22MF 15V
1			2701030		KRYSTAL 16 MHz
1			802018		KONDENSATOR 33PF
1			802033		" 330PF
1			855001		" 0,1MF
1			1103061		MODSTAND 1K5 1/8W
1			1103092		" 30K 1/8W
1			1103053		" 680E 1/8W
1			1330047		VINKELBØJET WRAP-PIW 1x6 POL
1			1319037		14 PINS ADAPTER
1			1319038		16 PINS ADAPTER
2			27104002		SKRUE M3x6 CHJ
2				DSP701-001	AFSTANDSSTYKKE

BETEGNELSE		UDGAVE	
DATA SEPARATOR PRINT		02	07
PA PART NR.		03	08
PA TEGN. PART NR.		04	09
DESIGN HC		05	10
01 UDGAVE 811125		06	11
STYKLISTE		MODUL NR. DSP701	
		BLAD 1/1	

RCSL: 44 - RT 1911

MANDATORY	<input type="checkbox"/>	RETROFIT ON FAILURE	<input checked="" type="checkbox"/>
WARRANTY	<input checked="" type="checkbox"/>	NON WARRANTY	<input type="checkbox"/>

PAGE	1	OF	1
RE: ECN NO:			

SERIAL EFFECTIVITY MIC 703, S/N 1534	EQUIPMENT AFFECTED RC700 RC702/DSP 701 Data Separator Print
---	--

NOTE
This FCO is irrelevant if FCO 19-008 is not implemented

REASON FOR CHANGE

The IC SN74LS153 may not be fast enough in maxi floppy disc applications.
In this case the computer may not read the floppy.

DESCRIPTION OF CHANGE

- Change the SN74LS153 to a SN74S153
- Code the FCO label: 19-011

ADDITIONAL COMMENTS

THE FCO-KIT CAN BE ORDERED AT THE SPARE PART STOCK
UNDER RC-PARTNUMBER: 8-0911
ADDRESS: HOVEDVEJEN 9, DK-2600 GLOSTRUP DENMARK

KITS FREE OF CHARGE YES NO

THE FCO-KIT INCLUDES:

QTY	DESCRIPTION	RC P/N
1	SN74S153	125026

DOCUMENTATION ENCLOSED

None

ESTIMATED INSTALLATION TIME: 0,5 h

PROJECT ENGINEER SIGN. <i>MVP Pedersen</i>	DATE 26/4 82	DEVELOPMENT MANAGER SIGN. <i>[Signature]</i>	DATE 29/4 82	SYSTEM PRODUCTION MANAGER SIGN. <i>[Signature]</i>	DATE 29/4 82	TECH. SERVICE MANAGER SIGN. <i>[Signature]</i>	DATE 28/4 82
---	-----------------	---	-----------------	---	-----------------	---	-----------------

Title:

Technical Manual for
POW 735 Power Supply

 **REGNECENTRALEN**

RC SYSTEM LIBRARY: FALKONERALLE 1 DK-2000 COPENHAGEN F

RCSL No: 44-RT 1788

Edition: November 1978

Author: Karsten Friis

Keywords:

POW 735, RC3600, RC3751.

Abstract:

This paper contains technical information on the
POW 735 power supply.

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1. DESCRIPTION.

1.

The POW 735 is designed to supply two FDD705 Flexible Disk Drives with AC and DC power.

The DC power supply section of the POW 735 consists of a transformer with three secondary windings, each supplying a separate rectifier and series regulator. These regulators produces the three output voltages: +24V, +5V and - 5V.

The POW 735 also contains timing logic and solid state relays to switch off the spindle drive motor of the FDD705 Diskette Drives if no disk access is made within half a minute.

2. SPECIFICATIONS.

2.1 Electrical Specifications.

<u>DC Output voltage:</u>	24V	5V	-5V
Tolerances	$\pm 10\%$	$\pm 5\%$	$\pm 5\%$
Maximum Ripple	100 mV	50 mV	50 mV
Maximum Current	2x0.8A	2x1.2A	2x80mA

AC Output voltage: 220V unregulated

Maximum AC current 2x250 mA

Power Requirements: 220V $\pm 10\%$, 50HZ $\pm 1\%$, 1A

2.2 Environmental Specifications.

Heat Dissipation (full Load): 55W, 1980 KJ/h, 1889 BTU/h
 Ambient Temperature: 10-40°C (59-194°F)
 Relative Humidity: 30-70% (no condensing)

2.3 Physical Specifications.

Dimension:

Height: 120mm

Width: 352mm

Depth: 120mm

Weight: 4.2 kg

Mounting: For mounting in the CHS712 chassis.

3. FUNCTIONAL DESCRIPTION.

3.

The AC motor control logic is divided into two identical parts. Each part consists of an app. 30 sec. timer and a 2 sec. timer.

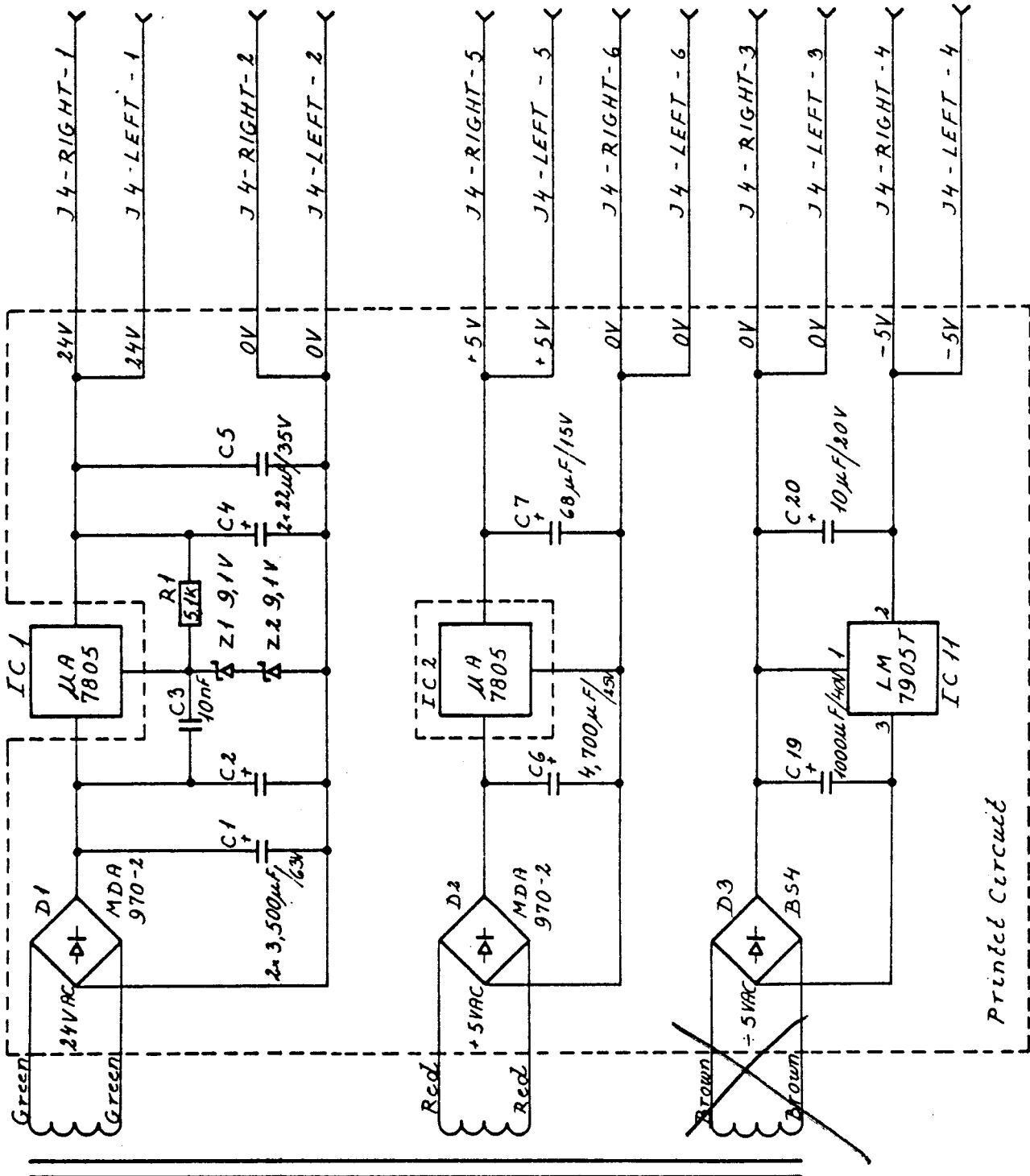
The FDC 705 flexible disk controller provides the POW 735 with the signal -IN USE, indicating that the appropriate disk drive is accessed by the controller. Whenever this signal has been inactive for more than app. 30 sec., the first timer runs out switching off the AC supply current for the drive. The status signal "MOTOR OFF" will also be set.

When the -IN USE signal becomes active again, the motor is turned on immediately and the status signal "MOTOR OFF" is cleared some 2 sec. later, allowing the motor to reach operational speed.

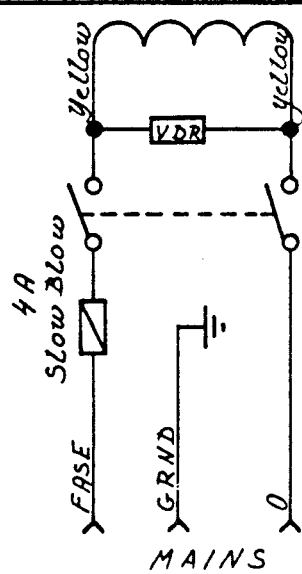
4. ELECTRIC DIAGRAMS.

The next two pages contains the electric and logic diagrams for the POW 735.

51.10.78 KF



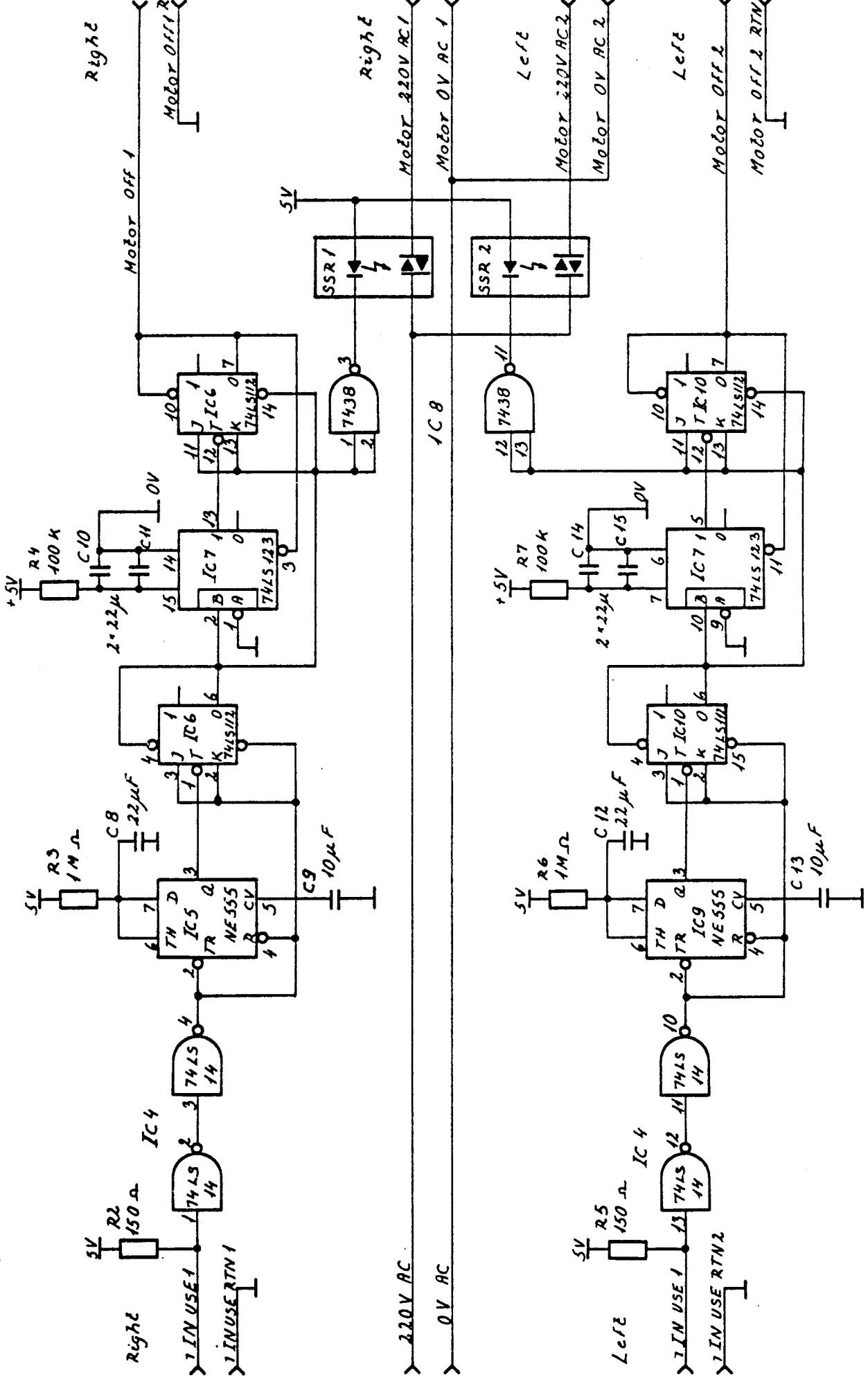
Printed Circuit



POW 735
R 12568

Rectifiers and DC Regulators

SI.10.78 KF



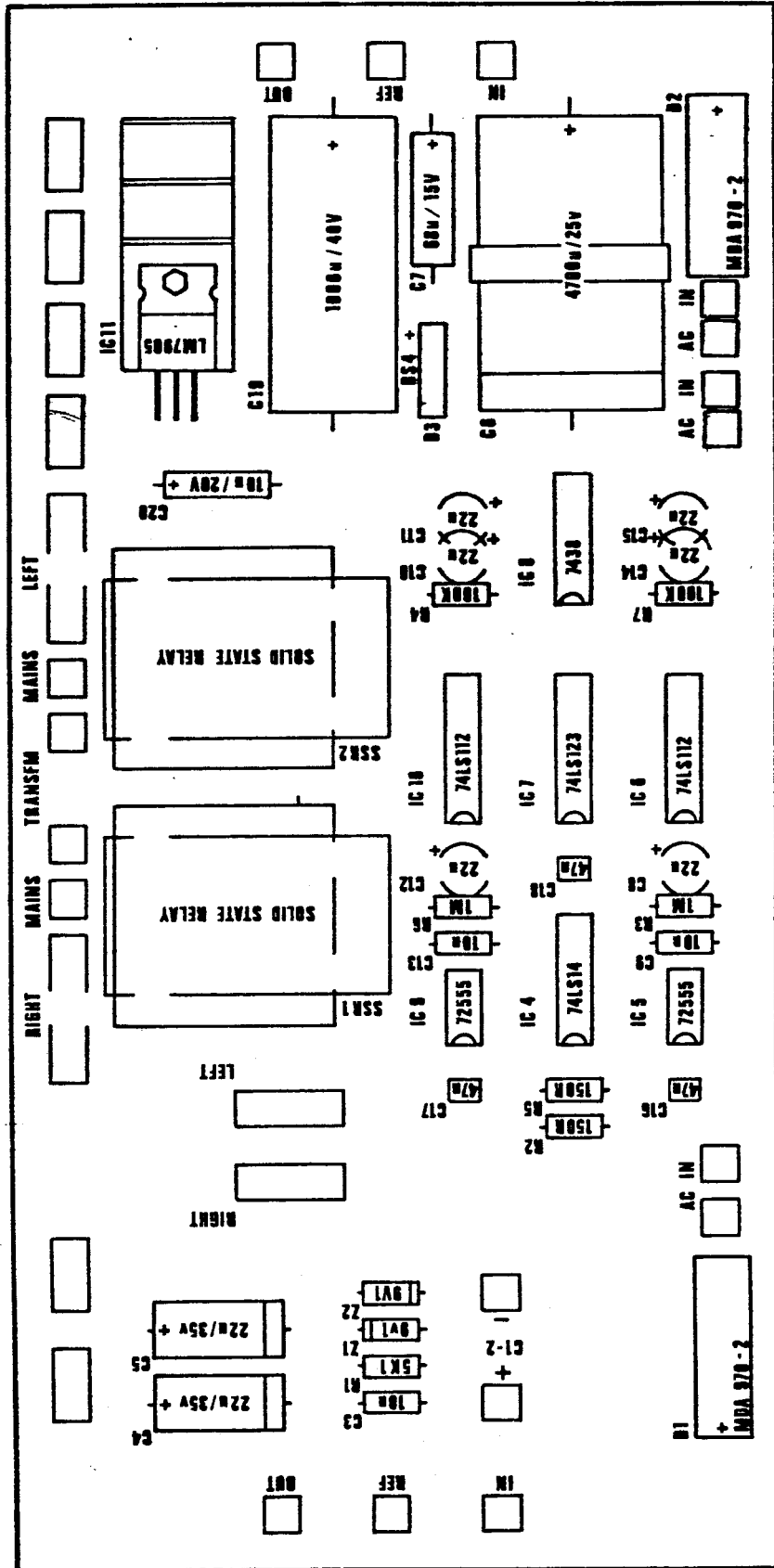
3 x 47nF A1 kodling,
C16 x 17 x 18

POW 735

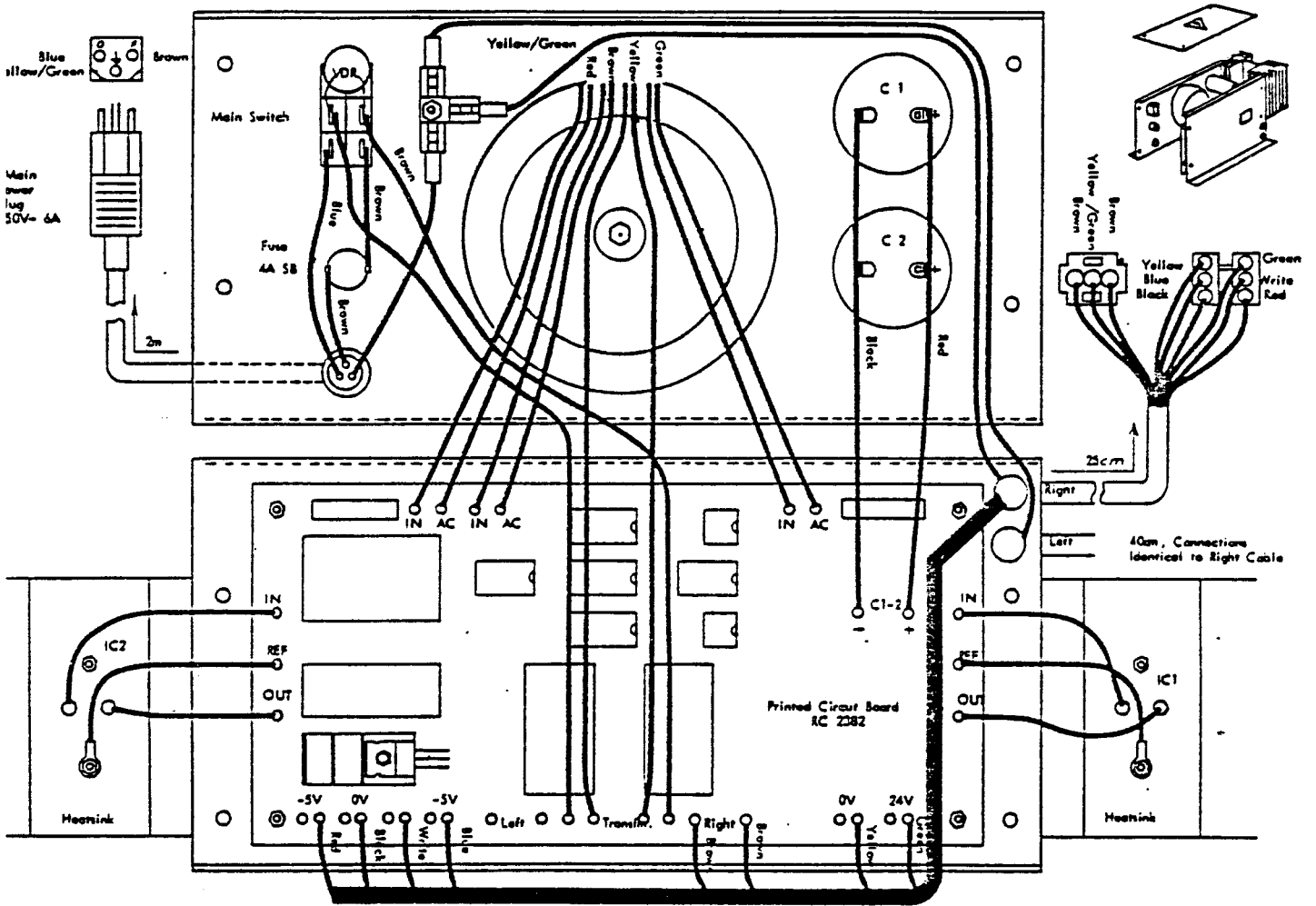
AC Možor Control Logic

R12569

5. ASSEMBLY DRAWINGS.



RC2382 Printed Circuit Board
component locations.



The Wires for Left Cable is Connected in a Similar Manner .

IC1 Must be Isolated from Heatink

POW 735 Assembly Drawing

6. COMPONENT LIST

6.

The following electrical components are used in the POW 735 power supply.

<u>QTY</u>	<u>Description</u>	<u>RC partnumber</u>
2	IC, MA7805	5-8317
1	IC, LM7905T	
2	MDA970-2, rectifier	
1	BS4, rectifier	
2	BZY88-C9V1, diode	4-3718
2	IC, 72555P	5-4717
1	IC, 7438N	4-0804
1	IC, 74LS14N	5-8111
2	IC, 74LS112N	6-1812
1	IC, 74LS123N	6-1915
2	S322, solid state relay	
2	Capacitor 3500 uF /63V	3-4413
1	Capacitor 4700 uF /25V	6-4404
1	Capacitor 68 uF /15V, tantal	1-1119
2	Capacitor 22 UF /35V, Tantal	1-0517
6	Capacitor 22 uF /15V, tantal	5-7001
3	Capacitor 46 uF /12V	4-3911
3	Capacitor 19 uF /100V	1-1315
1	Capacitor 10 uF /20V, tantal	
1	Capacitor 1000 uF /40V	
2	Resistor 150E , 1/8W	1-5108
1	Resistor 5K1 1/8W	1-0617
2	Resistor 100K 1/8W	1-0808
2	Resistor 1M 1/8W	1-0814
1	Fuse 4A SLO BLO 5x20	2-0718
1	Varistor 250V	4-5313
1	Transformator	

RCSL No: 44-RT1983

Edition: February 1981

Author: Mogens V. Pedersen

Title:

POW 740 Power Supply
Technical Manual

Keywords:

RC700, RC762, POW 740, Power Supply.

Abstract:

This paper contains the technical manual for POW 740 power supply to RC762 floppy disk drive.

(10 printed pages)

<u>TABLE OF CONTENTS</u>	<u>PAGE</u>
1. DESCRIPTION	1
Power Supply for Diskette Drive, POW740	2
RC899 Cable Lay Out	3
Connection 8" Disc Drive to RC equipment	4

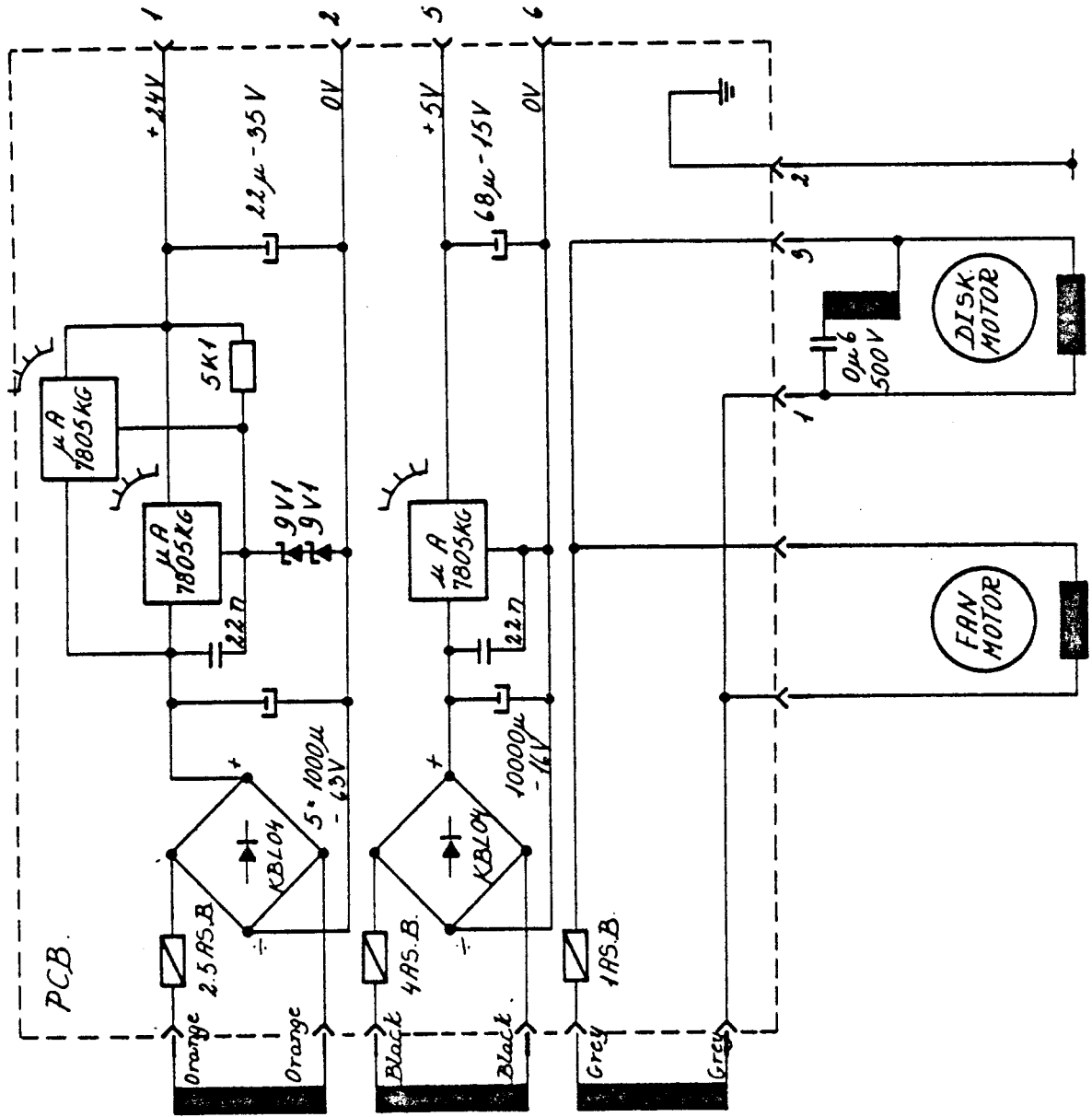
1. DESCRIPTION

1.

This paper contains the circuit diagram for the POW740 power supply used to supply the RC762 Floppy disk drive to RC702 microcomputer system.

The paper also contains a description of the cable connecting the floppy disk to RC702.

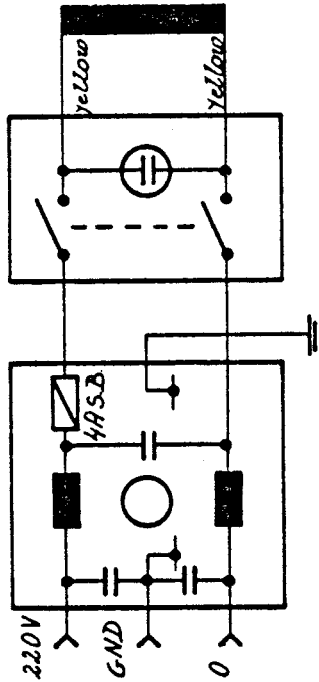
LOW VOLTAGE POWER
FOR DISKETTE DRIVE.

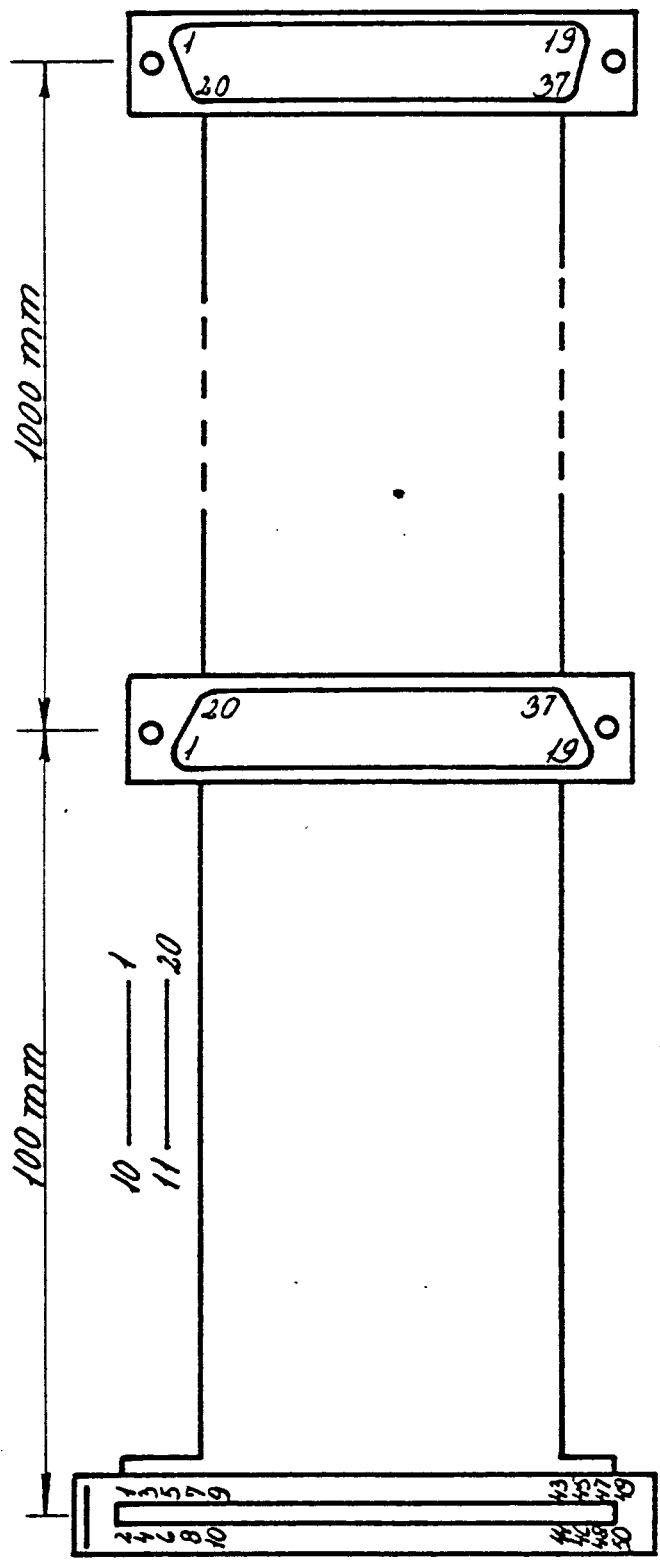


TRANSFORMER
DK 5459

SCAFFNER
FN 365-2/05

DOT 82/626





POW 740

RC 899 CABLE LAY OUT.

R.21333

8" DISC DRIVE				37 POL CANNON	
SIGNAL Return	SIGNAL	SIGNALNAME	DIRECTION	SIGNAL Return	SIGNAL
1	2				
3	4				
5	6				
7	8				
9	10	TWO SIDED	→	20	1
11	12			21	2
13	14	SIDE SELECT	←	22	3
15	16	LOW CURRENT	←	23	4
17	18	HEAD LOAD	←	24	5
19	20	INDEX	→	25	6
21	22	READY	→	26	7
23	24	MOTOR EN		27	8
25	26	DRIVE SEL 0	←	28	9
27	28	" " 1	←	29	10
29	30	" " 2	←	30	11
31	32	" " 3	←	31	12
33	34	DIRECTION SEL	←	32	13
35	36	STEP	←	33	14
37	38	WRITE DATA	←	34	15
39	40	WRITE GATE	←	35	16
41	42	TRACK 00	→	36	17
43	44	WRITE PROT	→	37	18
45	46	READ DATA	→		19
47	48				
49	50				

CONNECTION 8" DISK DRIVE TO RC EQUIPMENT

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Technical Manual

RCSL No.: 44-RT1983

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af 1979

Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark

RCSL No: 31-D619

Edition: September 1980

Author: Peter Koch Andersson

Title:

LIS701
V24 LINESELECTOR
Reference Manual

Keywords:

RC700, LINESELECTOR, RC791

Abstract:

This paper describes the operation of RC791.

(12 printed pages)

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TABLE OF CONTENTS	PAGE
1. GENERAL	1
2. LOGIC SPECIFICATION	2
2.1 Signals	2
2.2 Selection	2
2.3 Deselection	4
3. CABLE CONNECTIONS	5
4. PHYSICAL REQUIREMENTS	6

1. GENERAL

1.

The LIS701 Lineselctor is a device for connection of up to eight RC700 microcomputers to two common resources, so as a printer, a master computer with associated flexible discs or a modem.

The interface used is CCITT V24/ISO2110; The inputs 1 to 8 are of the type DCE while the outputs A and B are of the type DTE.

With each output A and B is associated a scanner scanning the inputs 1 to 8 for a possible request for connection, see figure 1.

A microcomputer requests a connection to one of the outputs specified by the start up sequence. The request is acknowledged by the corresponding scanner when the output and scanner are not engaged in servicing another input.

LED displays on the front at LIS701 indicate the current configuration. Each of the outputs A and B has a seven segment digit indicating to which input number it is currently connected; when it is idle, the display is dark.

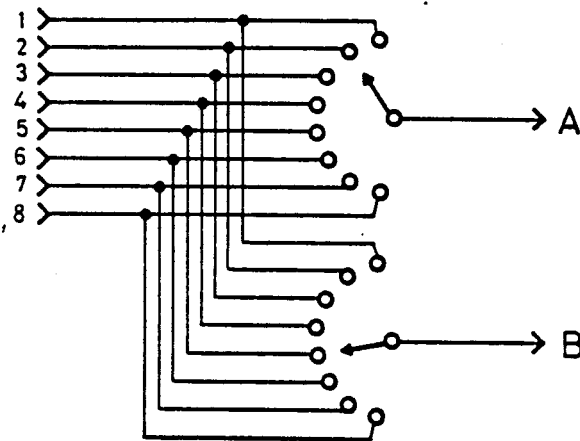


Figure 1.

2. LOGIC SPECIFICATION

2.

2.1 Signals

2.1

The LIS701 supports the following CCITT V24 signals:

V24 circuit	name	pin	abbrev.	direction *
101	protective ground	1	GND	
102	signal ground	7		
103	transmitted data	2	TXD	out
104	received data	3	RXD	in
105	request to send	4	RTS	out
106	clear to send	5	CTS	in
107	data set ready	6	DSR	in
108	data terminal ready	20	DTR	out
109	carrier detected	8	CD	in

* relative to outputport.

The input signals on ports 1 to 8 are found as output signals on ports A and B, and vice versa. All the signals except DTR are relayed directly through between the interconnected ports (via receiver and transmitter), but the four signals RTS, CTS, DTR and CD are used for establishing connection through the LIS.

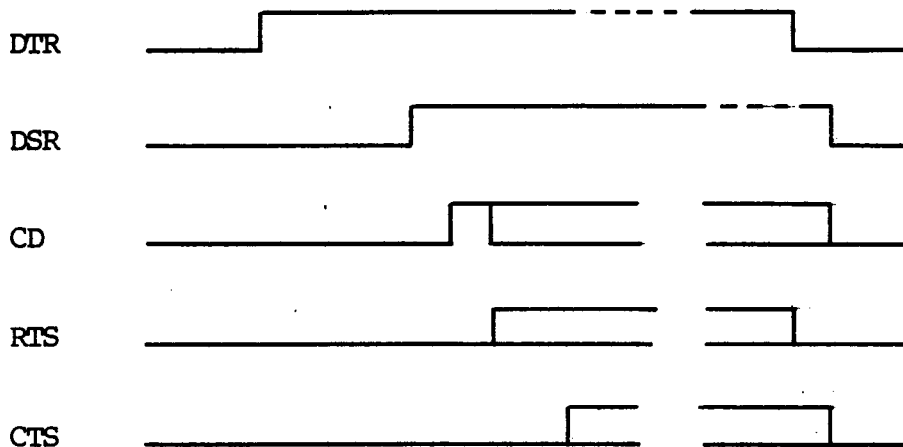
2.2 Selection

2.2

A microcomputer connected to an inputport 1 to 8 requests for connection to one of the ports A or B by rising DTR. The selection of A or B is accomplished by means of RTS (figure 2). The state of RTS must be stable at least 100 nanoseconds before the rising of DTR. The selection sequence is terminated by the reception of DSR plus one (or both) of the signals CD and CTS. The state of RTS must not be changed before this time. In the case the wanted port is busy, no response will arrive, and DTR may be dropped anytime.

In the case, the wanted port is ready, the LIS701 will add at most 10 msec to the duration of the selection phase.

Selection at Port A:



Selection of Port B:

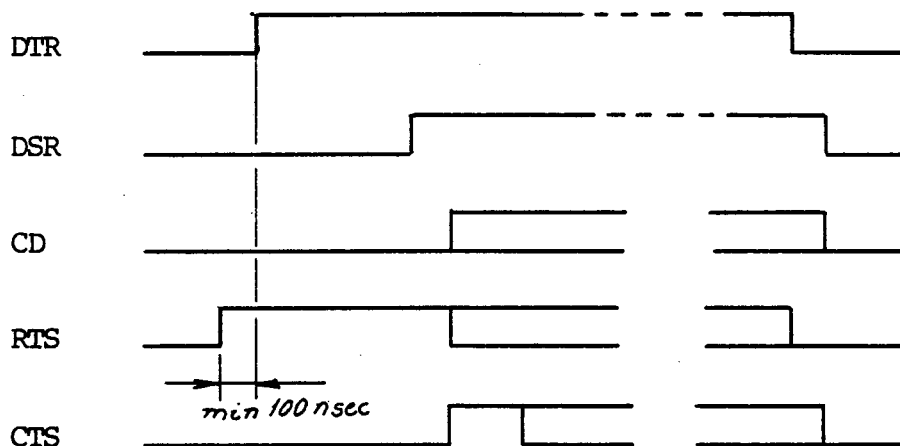


Figure 2.

The connection will be maintained by the LIS701 as long as DTR is high.

The DSR indicates that selection is performed. In the cases where the microcomputer is not sensitive to DSR, the alternative criterion may be chosen:

selection of Port A is done, when CD goes high.
 selection of Port B is done, when CTS goes high.

The signals out of Port A and B are in the off state (TXD circuit 103 is 1), when no connection is established.

When the A-scanner detects a request for connection, the A port will set DTR (circuit 108) on, and establish connection between all other circuits, so RTS will (because of the terminal connected to the input port) not go on until the common resource on port A responds with CD on.

If a second LIS701 is cascaded to port A, this will have its A-scanner activated as well.

When the B-scanner detects a request for connection, the B port will open connection between all circuits but DTR and after a delay of app. 10 micro second turn DTR on. This delay assures, that RTS on port B is on before DTR goes on, ensuring that a cascaded second LIS701 on port B also selects its port B.

Cascading is possible to any level, but because the same port selection (A or B) ripples through all levels cascading only increases the number of inputs, not the number of outputs.

2.3 Deselection

2.3

Deselection is done when DTR is dropped. The deselected scanner sets all outgoing control signals off and the outgoing data-signal to 1, and resumes scanning.

Reselection must not be requested (DTR must not be raised) on the same input, until the deselection is complete.

The deselection is complete when DSR, CD and CTS are all off, or max. 1 millisecond after the fall of DTR.

3. CABLE CONNECTIONS

3.

The LIS701 is regarded as being put between a RC700 and a resource, which is to be shared among several RC700's.

The cable which before connected RC700 with the resource, is disconnected from RC700 and connected to one of the outputs A or B on LIS701, and RC701 is then connected to one of the inputs 1 to 8 of LIS701 via a MF003 cable (Long, Median or Short).

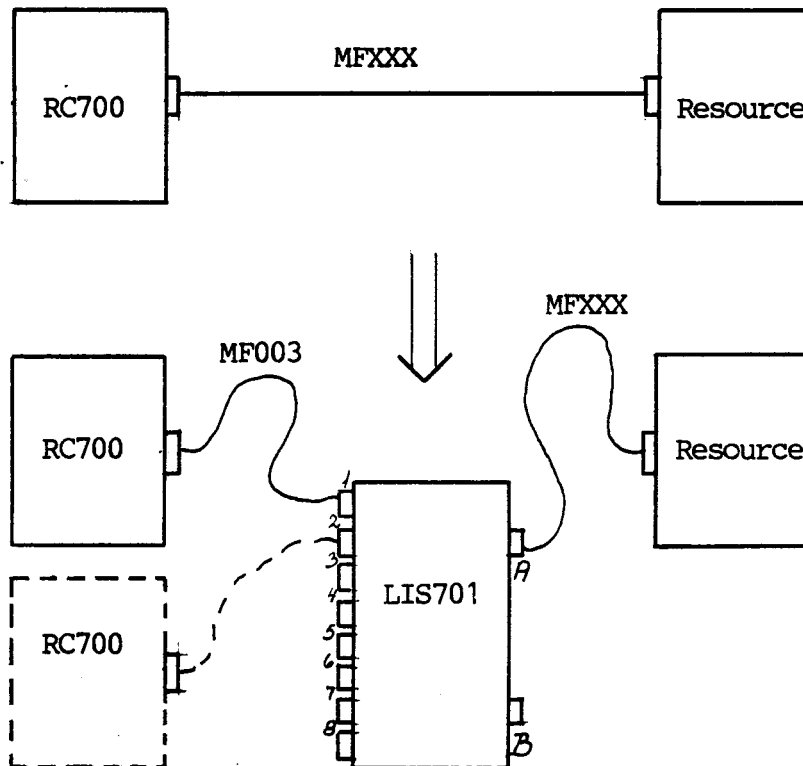


Figure 3.

The numbering of the line in plugs is arranged in a way, that allows straight forward insertion of cables in ascending order.

4. PHYSICAL REQUIREMENTS

4.

Power requirement: 220V \pm 10% 50 Hz 15 W

Ambient temperature: 16-32°C (60-90°F).

Relative humidity: 20-80% (no condensation).

Physical size: 470 mm x 300 mm x 70 mm

RETURN LETTER

Title: LIS701 V24 LINESELECTOR, Reference Manual RCSL No.: 31-D619

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af 1979

Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark

RCSL No: 44-RT1978

Edition: January 1981

Author: Peter Koch Andersson

Title:

RC791 Lineselector
Technical Manual

Keywords:

RC791, LIS701, Lineselector

Abstract:

This manual contains technical information on the RC791 lineselector.

(28 printed pages)

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1. DESCRIPTION	1
1.1 General Description	1
1.2 Functional Description	1
1.3 Power Supply	2
2. BLOCK DIAGRAM	4
3. LOGIC DIAGRAMS	6

1. DESCRIPTION

1.

1.1 General Description

1.1

LIS701 is a V24-switch able to connect two of eight DTE's with two DCE's, as requested by the DTE's.

A DTE performs a connection request by means of the signals Data Terminal Ready and Request To Send.

RTS is used to select the DCE, and DTR indicates connection request.

If the selected DCE is not busy, the signals are connected through, and the connection persists as long as DTR is true.

To each DCE output, is assigned a scanner, which, when the DCE is not busy, scans the DTE-inputs for a possible connection request.

1.2 Functional Description

1.2

The signal inputs from the DTE ports are connected through line receivers to tristate gates connecting them to the A-bus or B-bus (see the block diagram). The tristate enable signals \neg ASEL(1) to \neg ASEL(8) and \neg BSEL(1) to \neg BSEL(8) are the decoded values of A(0:2) and B(0:2). (The number 000 is converted into sel(8), creating a sequence 1 to 8 rather than 0 to 7). The pointers A(0:2) and B(0:2) are the outputs of two binary counters, which when ABUSY and BBUSY are false, are scanning the DTE inputs for a possible DTR.

If the A-scanner meets a DTR together with a \neg RTS, ABUSY is set, blocking the clockpulses to the A-scanner, turning on the A-display indicating the value on the A-scanner, gating the signals through between the DTE and the DCE and finally sending DTR to the DCE.

The power supply supplies ± 12 V for the V24 transmitters, and +5 V for the logic. The ± 12 V are supplied via monolithic serial regulators. Due to the greater power dissipation resulting if a linear regulator was used for the 5 V, a switch mode regulator is used for this voltage.

The function of this regulator is best understood by rewriting the diagram as done in figs. 1 and 2.

The box in fig. 1 contains a comparator and a 5 V reference. The voltage on the output of this switches between +25 V and 0 V with an average value of 5 V. The voltage developed across C is this average superposed a small ripple voltage, equal to the hysteresis defined by R1 and R2: $U_{\text{ripple.pp.}} = (r2/(R1+R2))*25$ V.

The operation cyclus is thus: point 1 outputs 25 V until the voltage on C has increased to 5 V + U_{ripple} , then the voltage on point 1 switches to 0 V, and the voltage on C decreases to 5 V, at which voltage, point 1 again switches to +25 V, etc.

Fig. 2 shows what the box in fig. 1 really contains. The IC LM78L05 contains the 5 V reference plus the comparator except the "output stage". This consists of the transistor T and the "freewheeling" diode D. Current flows always out of point 1 either through T from 25 V or through D from 0 V.

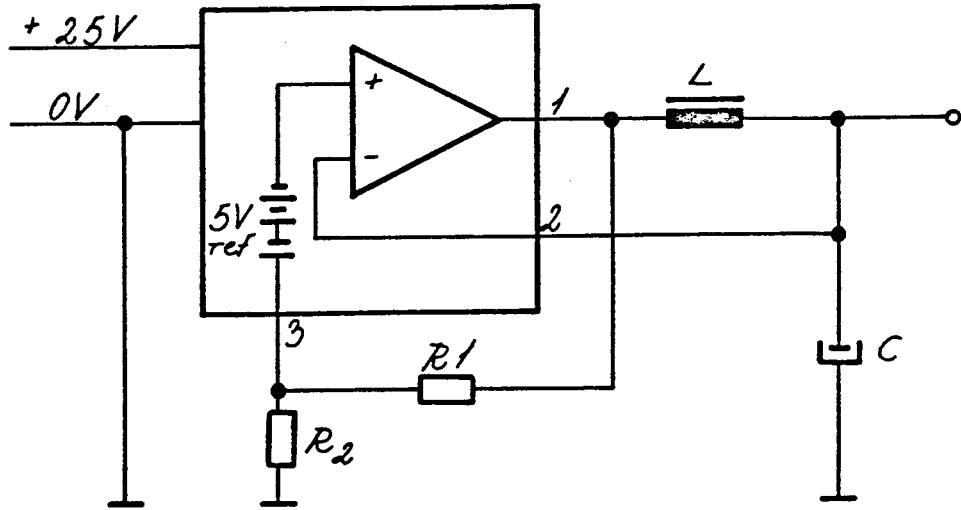


Fig. 1

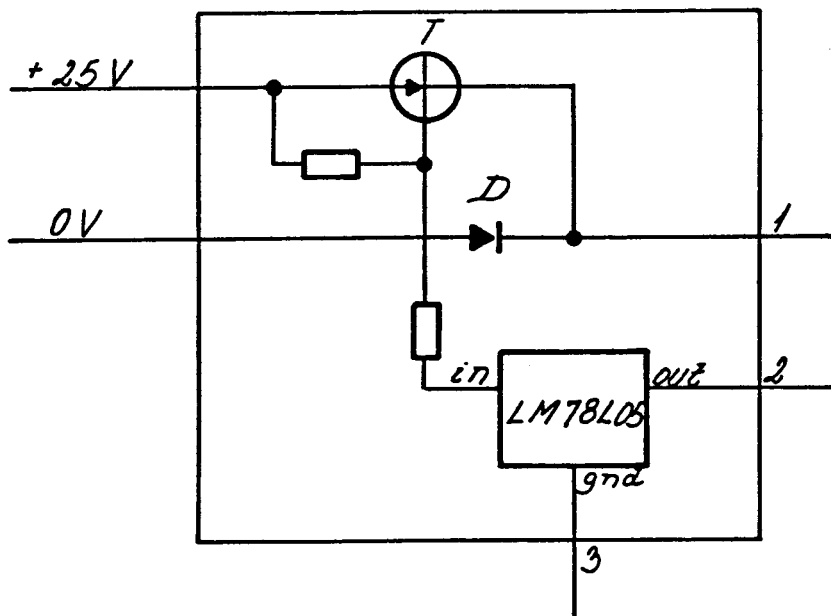
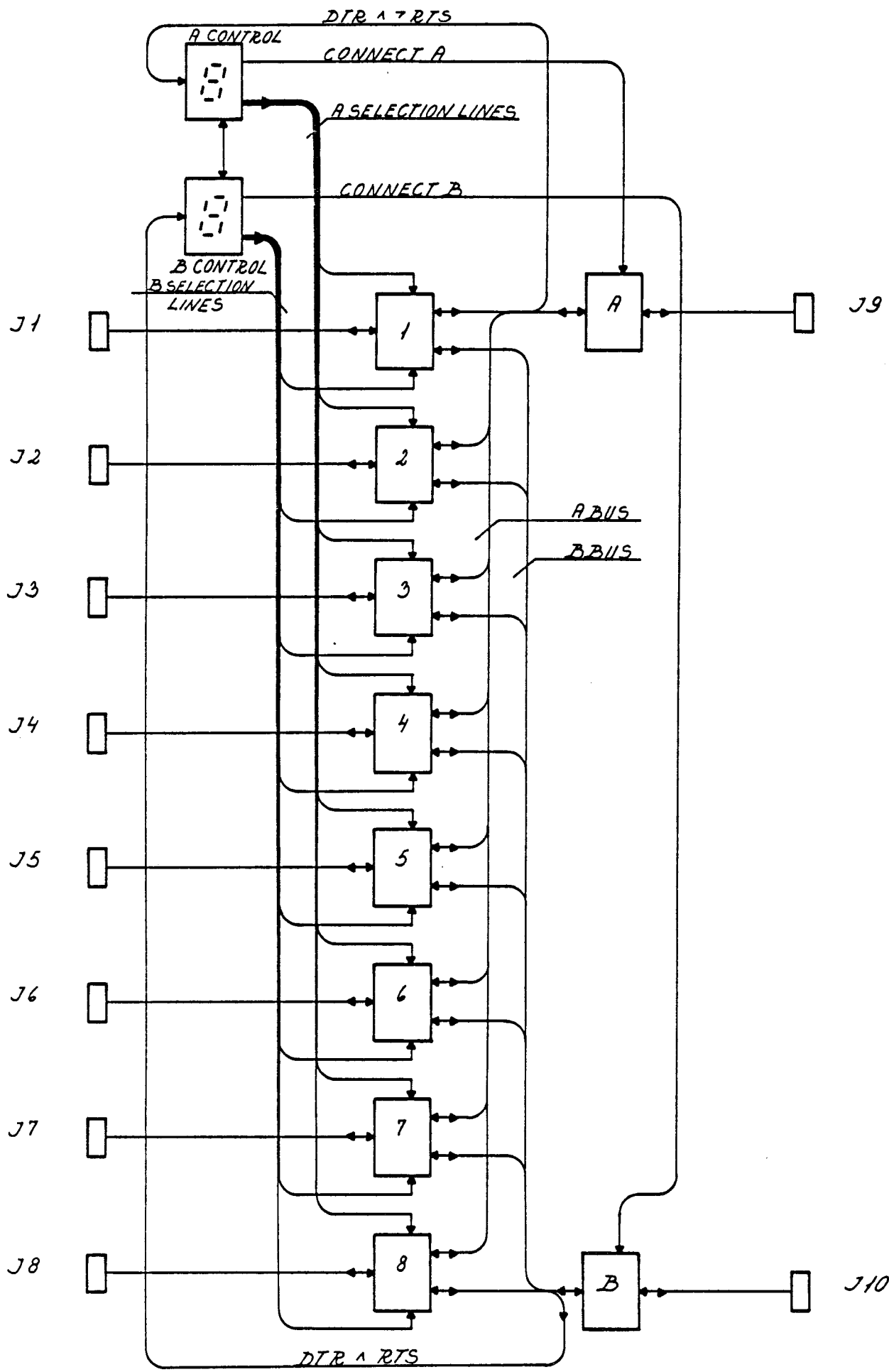


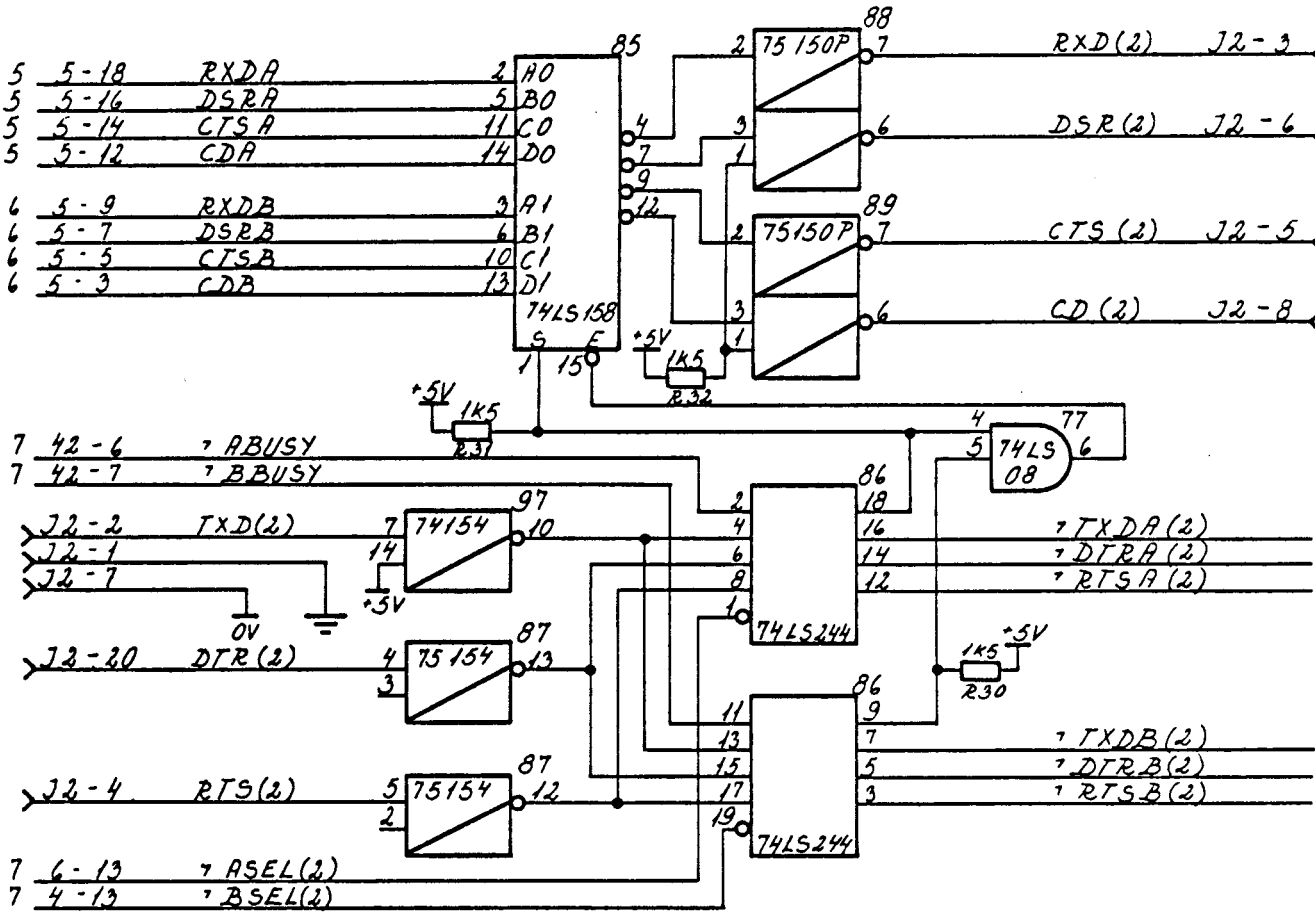
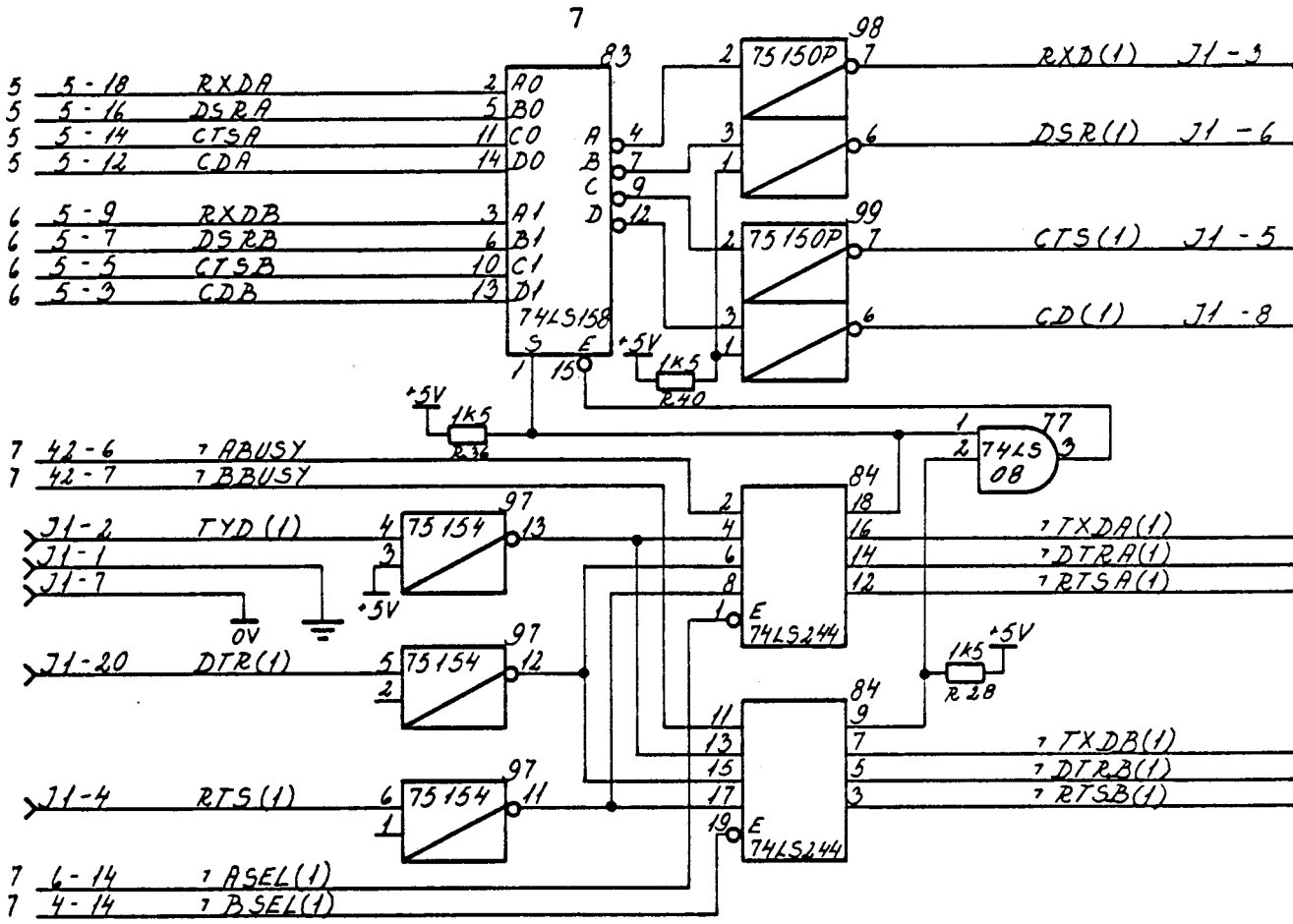
Fig. 2



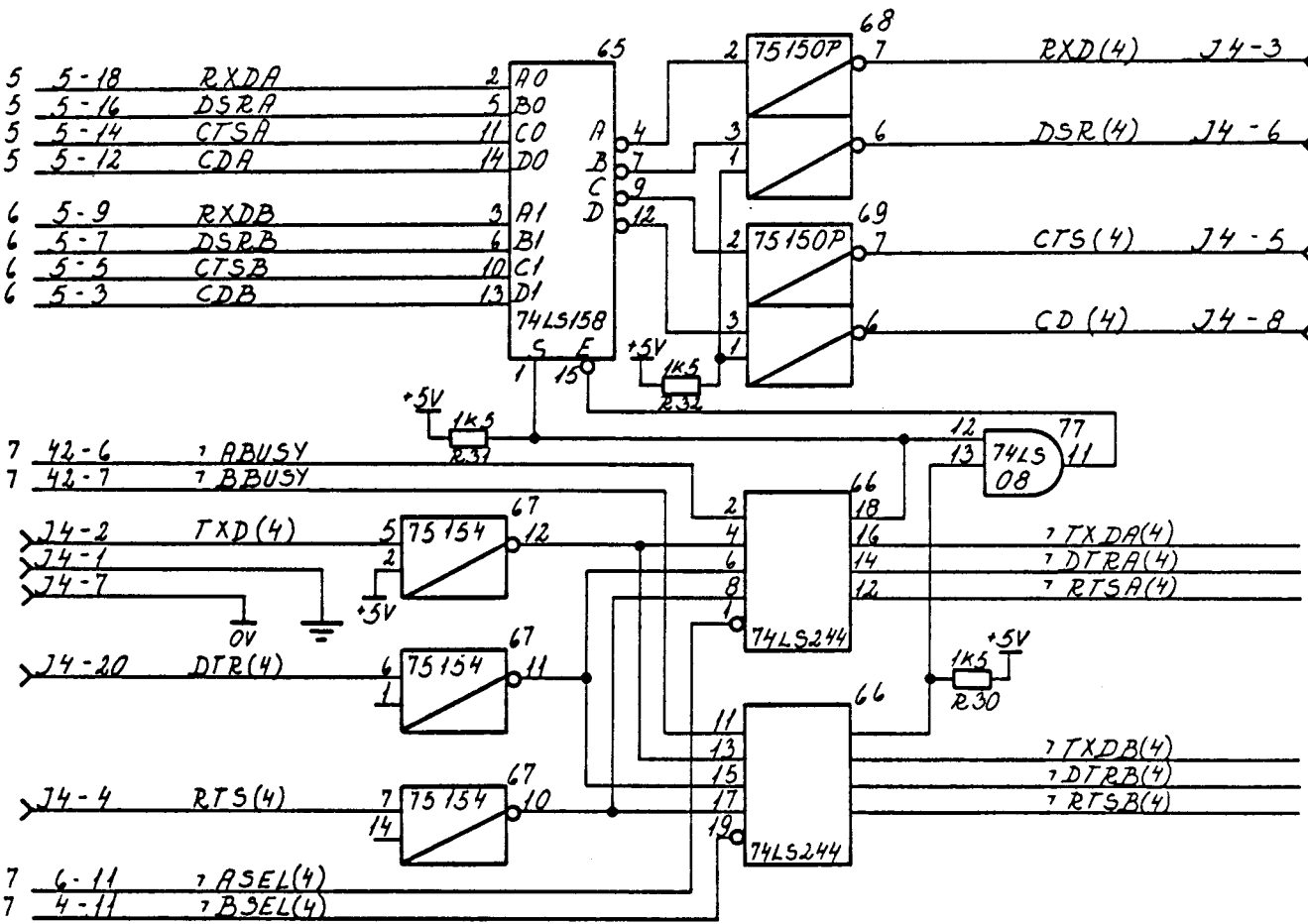
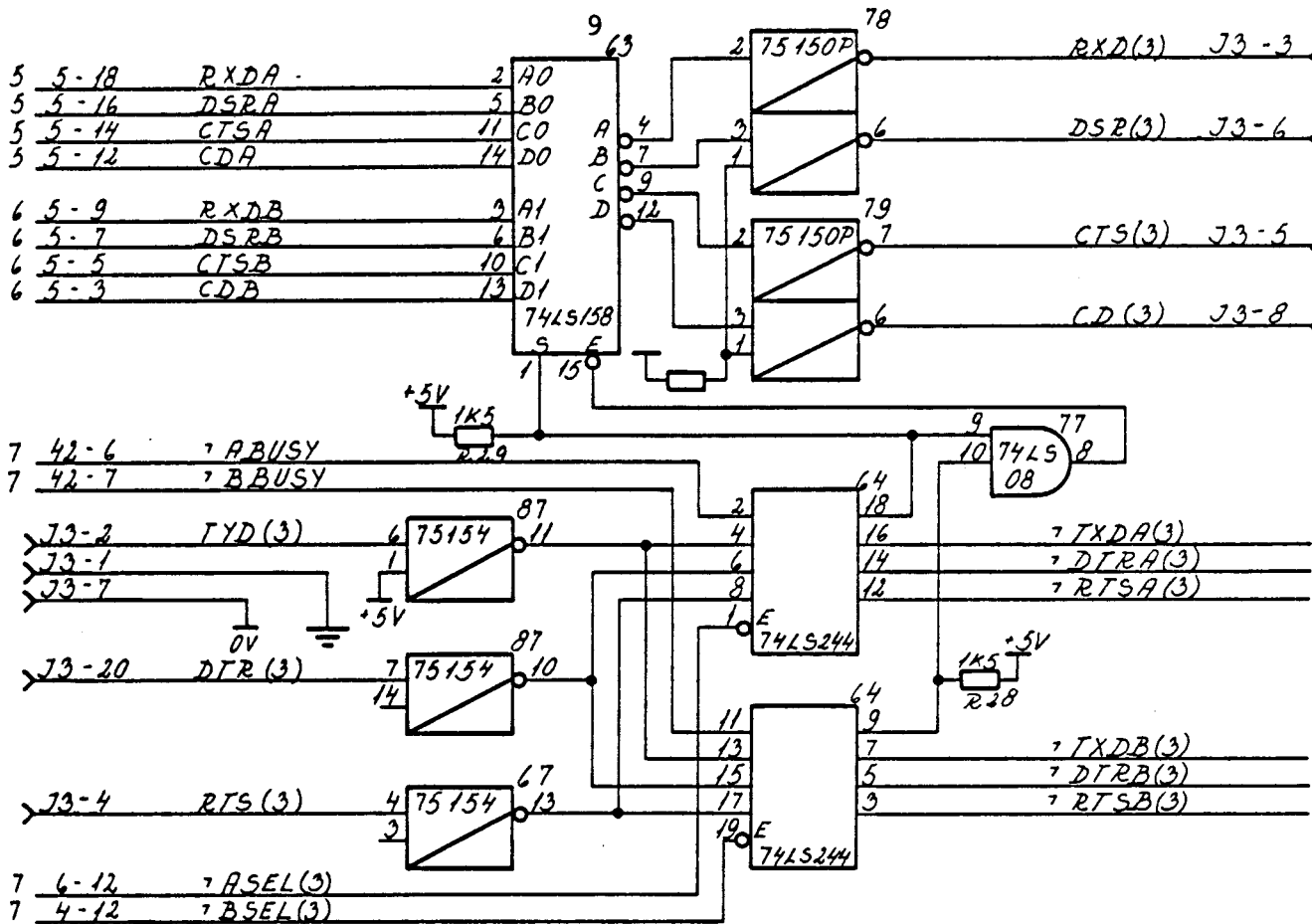
L15701
R 13098

BLOCK DIAGRAM

Signal	Destination	Description
RXD(1)	J1	Received Data to J1 V24-levels
DSR(1)	J1	Data Set Ready to J1 V24-levels
CIS(1)	J1	Clear To Send to J1 V24-levels
CD(1)	J1	Carrier Detect to J1 V24-levels
$\overline{\text{TXDA}}(1)$	p. 5	Transmitted Data from J1 tristate-multiplexed to A bus
$\overline{\text{DTRA}}(1)$	p. 5	Data Terminal Ready from J1 tristate-multiplexed to A bus
$\overline{\text{RTSA}}(1)$	p. 5	Request To Send from J1 tristate-multiplexed to A bus
$\overline{\text{TXD}}(1)$	p. 6	Transmitted Data from J1 tristate-multiplexed to B bus
$\overline{\text{DTR B}}(1)$	p. 6	Data Terminal Ready from J1 tristate-multiplexed to B bus
$\overline{\text{RTS B}}(1)$	p. 6	Request To send from J1 tristate-multiplexed to B bus
RXD(2)	J2	Received Data to J2 V24-levels
DSR(2)	J2	Data Set Ready to J2 V24-levels
CIS(2)	J2	Clear To Send to J2 V24-levels
CD(2)	J2	Carrier Detect to J2 V24-levels
$\overline{\text{TXDA}}(2)$	p. 5	Transmitted Data from J2 tristate-multiplexed to A bus
$\overline{\text{DTRA}}(2)$	p. 5	Data Terminal Ready from J2 tristate-multiplexed to A bus
$\overline{\text{RTSA}}(2)$	p. 5	Request To Send from J2 tristate-multiplexed to A bus
$\overline{\text{TXD}}(2)$	p. 6	Transmitted Data from J2 tristate-multiplexed to B bus
$\overline{\text{DTR B}}(2)$	p. 6	Data Terminal Ready from J2 tristate-multiplexed to B bus
$\overline{\text{RTS B}}(2)$	p. 6	Request To send from J2 tristate-multiplexed to B bus

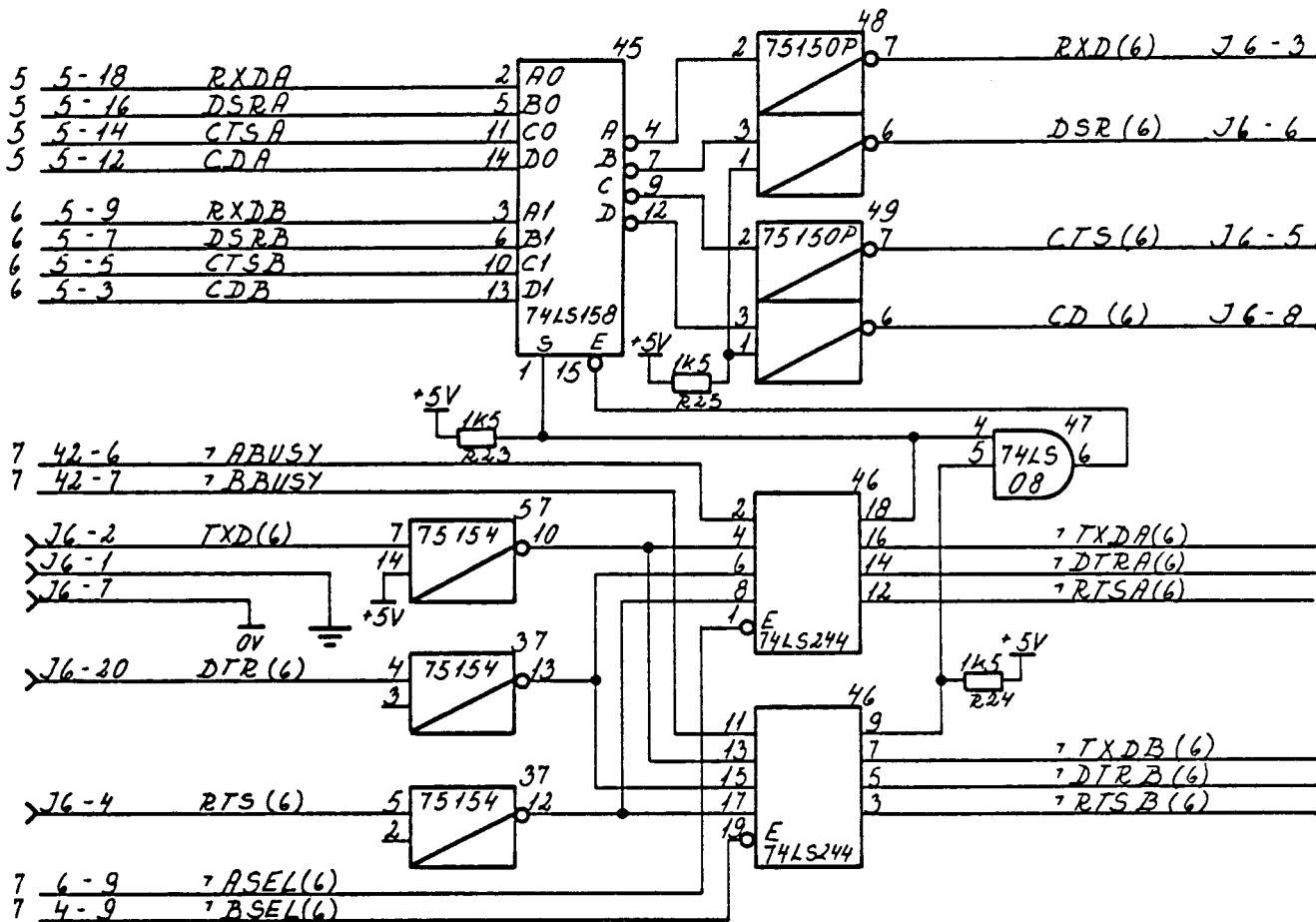
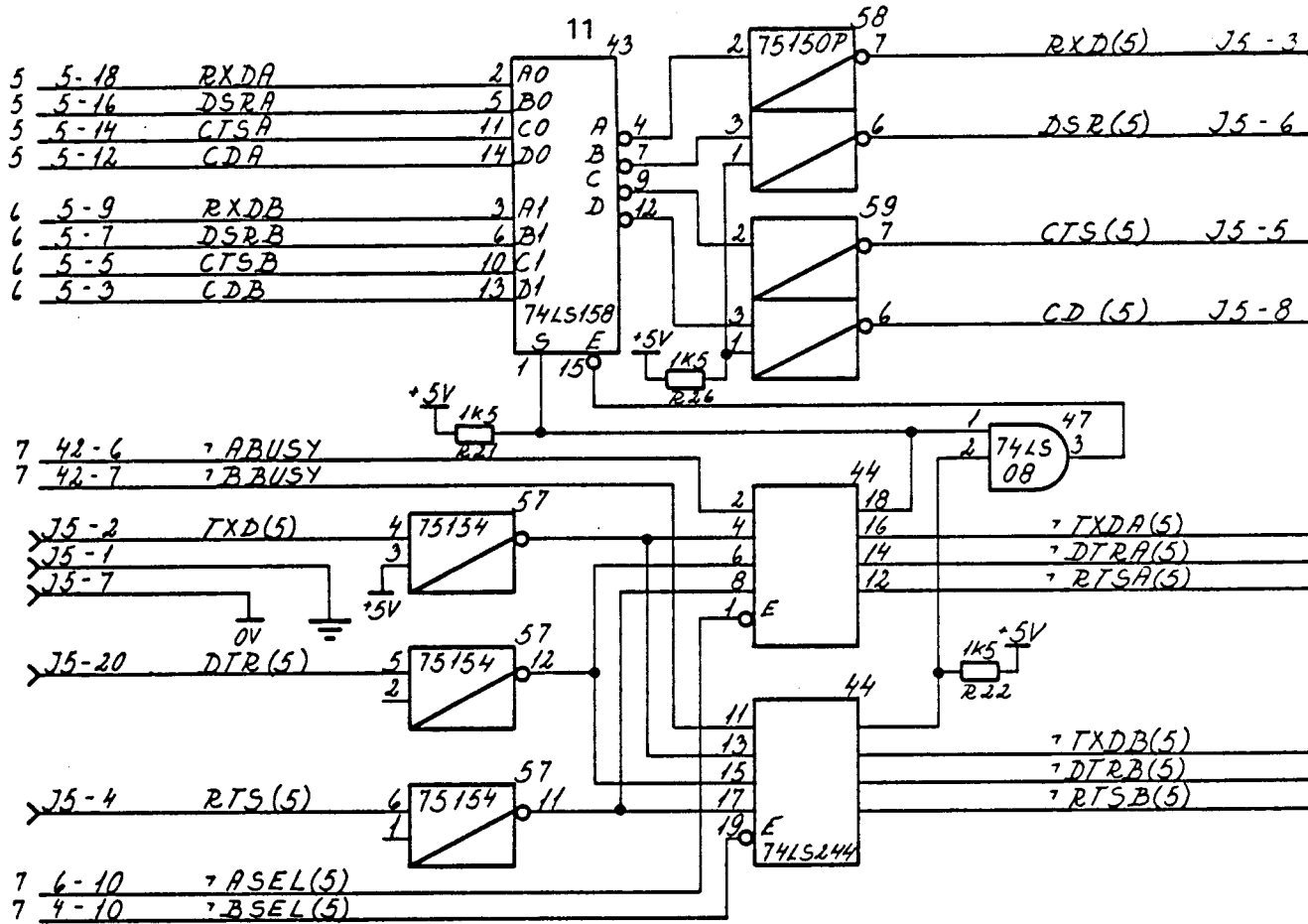


Signal	Destination	Description
RXD(3)	J3	Received Data to J3 V24-levels
DSR(3)	J3	Data Set Ready to J3 V24-levels
CTS(3)	J3	Clear To Send to J3 V24-levels
CD(3)	J3	Carrier Detect to J3 V24-levels
TXDA(3)	p. 5	Transmitted Data from J3 tristate-multiplexed to A bus
DTRA(3)	p. 5	Data Terminal Ready from J3 tristate-multiplexed to A bus
RTSA(3)	p. 5	Request To Send from J3 tristate-multiplexed to A bus
TXD(3)	p. 6	Transmitted Data from J3 tristate-multiplexed to B bus
DTR B(3)	p. 6	Data Terminal Ready from J3 tristate-multiplexed to B bus
RTS B(3)	p. 6	Request To send from J3 tristate-multiplexed to B bus
RXD(4)	J4	Received Data to J4 V24-levels
DSR(4)	J4	Data Set Ready to J4 V24-levels
CTS(4)	J4	Clear To Send to J4 V24-levels
CD(4)	J4	Carrier Detect to J4 V24-levels
TXDA(4)	p. 5	Transmitted Data from J4 tristate-multiplexed to A bus
DTRA(4)	p. 5	Data Terminal Ready from J4 tristate-multiplexed to A bus
RTSA(4)	p. 5	Request To Send from J4 tristate-multiplexed to A bus
TXD(4)	p. 6	Transmitted Data from J4 tristate-multiplexed to B bus
DTR B(4)	p. 6	Data Terminal Ready from J4 tristate-multiplexed to B bus
RTS B(4)	p. 6	Request To send from J4 tristate-multiplexed to B bus



PGA
PKA

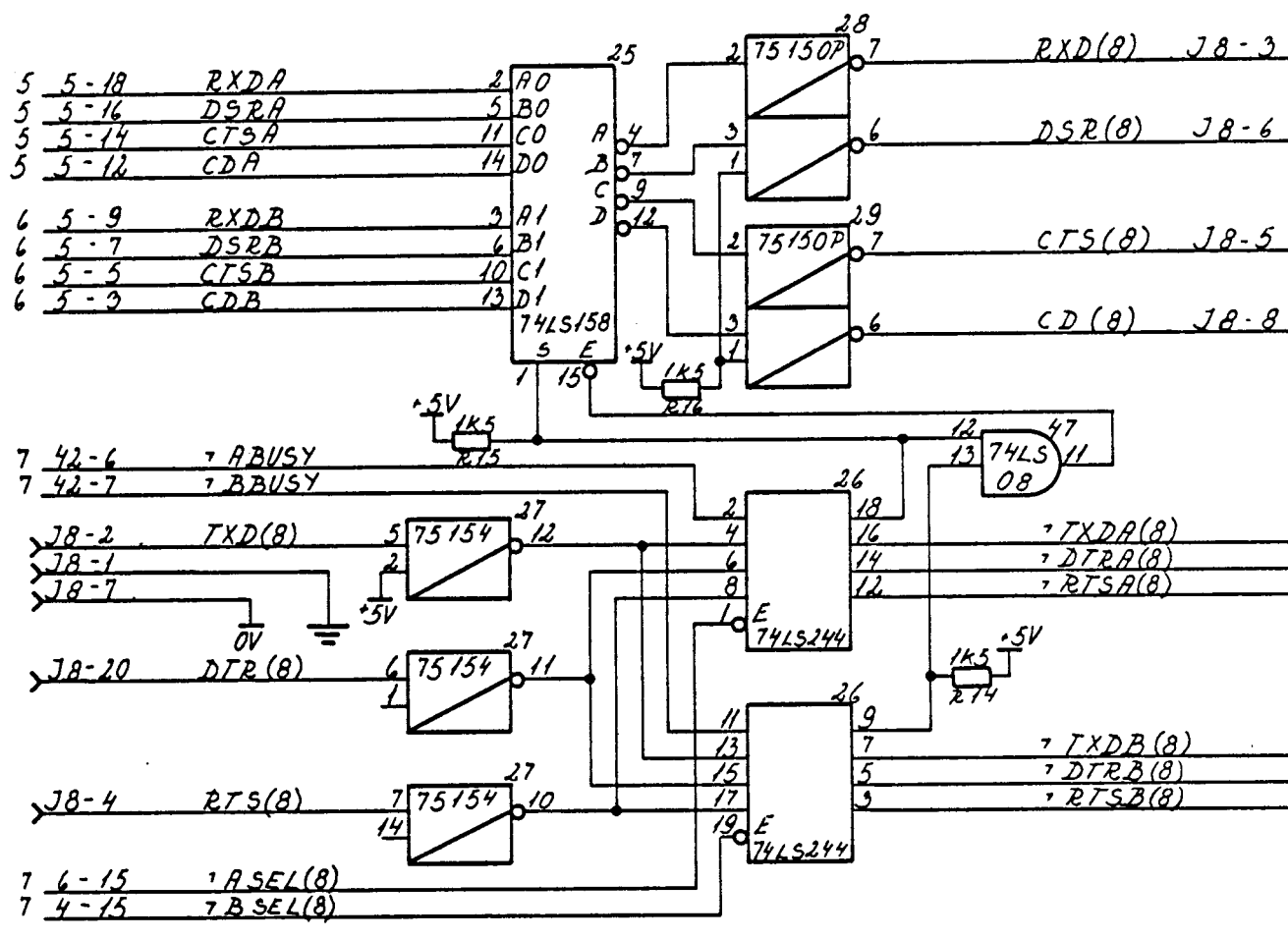
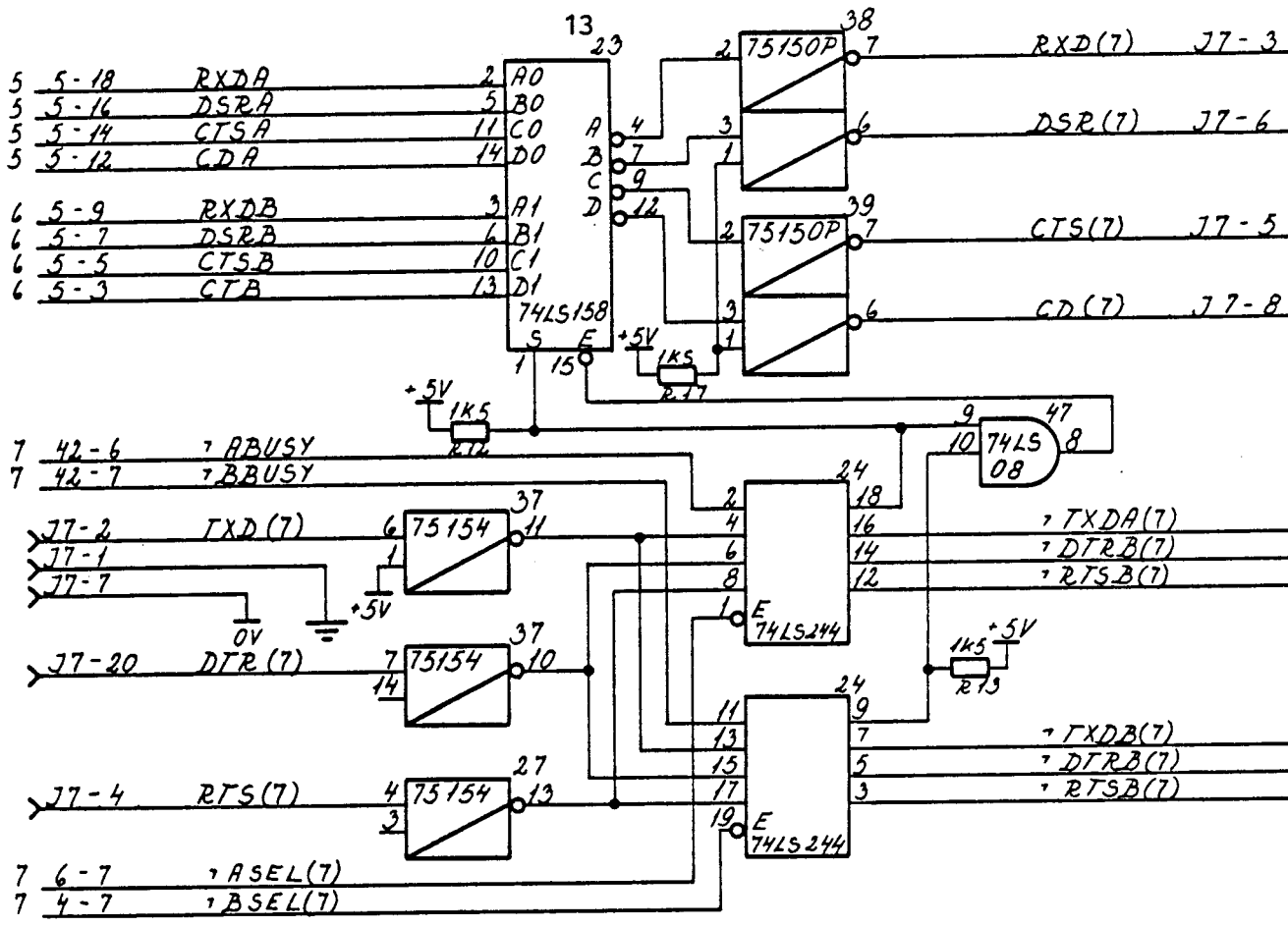
Signal	Destination	Description
RXD(5)	J5	Received Data to J5 V24-levels
DSR(5)	J5	Data Set Ready to J5 V24-levels
CTS(5)	J5	Clear To Send to J5 V24-levels
CD(5)	J5	Carrier Detect to J5 V24-levels
TXDA(5)	p. 5	Transmitted Data from J5 tristate-multiplexed to A bus
DTRA(5)	p. 5	Data Terminal Ready from J5 tristate-multiplexed to A bus
RTSA(5)	p. 5	Request To Send from J5 tristate-multiplexed to A bus
TXD(5)	p. 6	Transmitted Data from J5 tristate-multiplexed to B bus
DTR B(5)	p. 6	Data Terminal Ready from J5 tristate-multiplexed to B bus
RTS B(5)	p. 6	Request To send from J5 tristate-multiplexed to B bus
RXD(6)	J6	Received Data to J6 V24-levels
DSR(6)	J6	Data Set Ready to J6 V24-levels
CTS(6)	J6	Clear To Send to J6 V24-levels
CD(6)	J6	Carrier Detect to J6 V24-levels
TXDA(6)	p. 5	Transmitted Data from J6 tristate-multiplexed to A bus
DTRA(6)	p. 5	Data Terminal Ready from J6 tristate-multiplexed to A bus
RTSA(6)	p. 5	Request To Send from J6 tristate-multiplexed to A bus
TXD(6)	p. 6	Transmitted Data from J6 tristate-multiplexed to B bus
DTR B(6)	p. 6	Data Terminal Ready from J6 tristate-multiplexed to B bus
RTS B(6)	p. 6	Request To send from J6 tristate-multiplexed to B bus



L15701
R 13101

Port 5 and Port 6

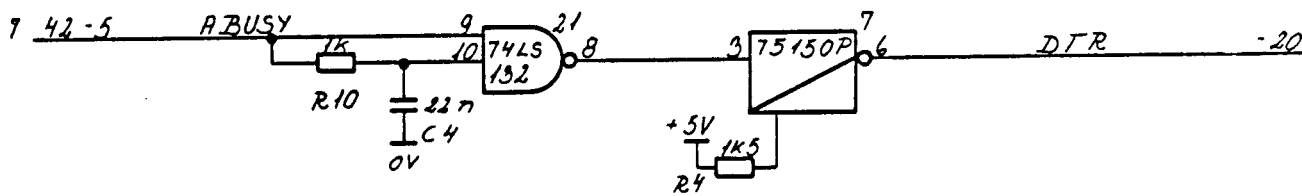
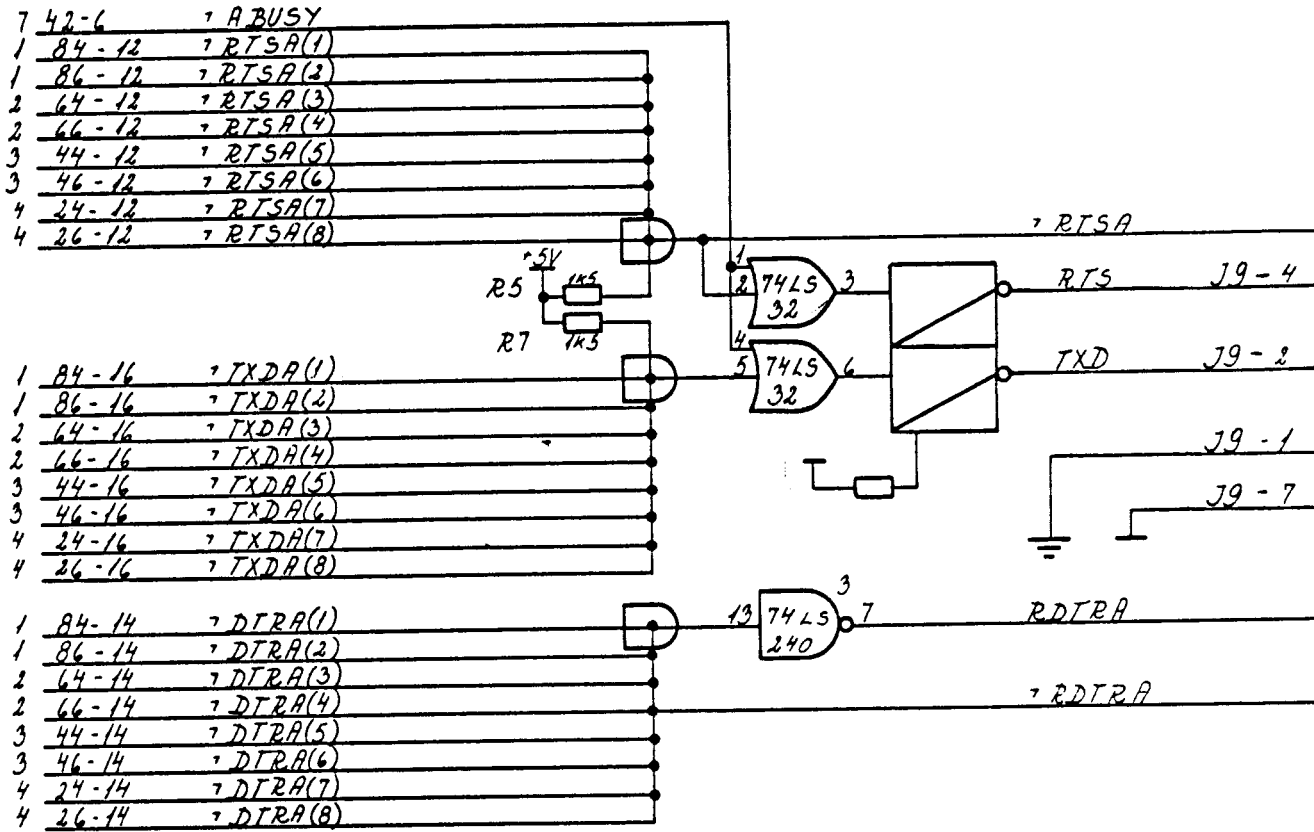
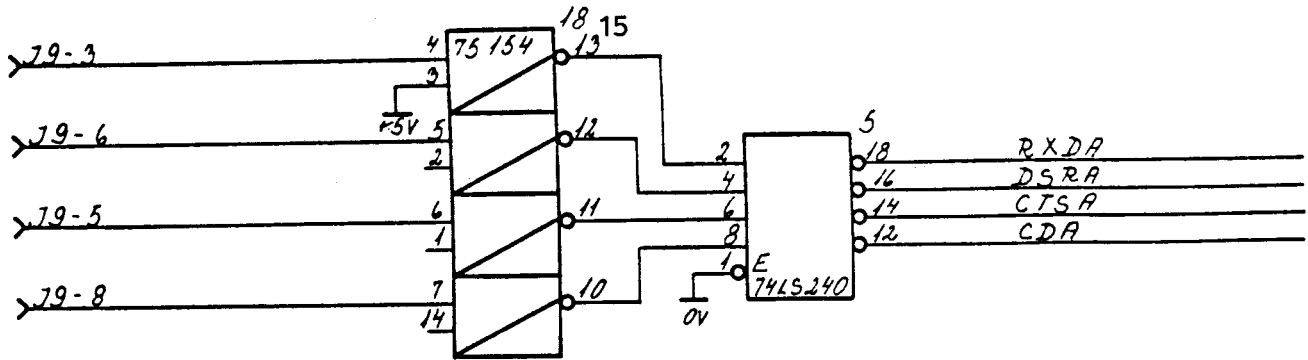
Signal	Destination	Description
RXD(7)	J7	Received Data to J7 V24-levels
DSR(7)	J7	Data Set Ready to J7 V24-levels
CTS(7)	J7	Clear To Send to J7 V24-levels
CD(7)	J7	Carrier Detect to J7 V24-levels
TXDA(7)	p. 5	Transmitted Data from J7 tristate-multiplexed to A bus
DTRA(7)	p. 5	Data Terminal Ready from J7 tristate-multiplexed to A bus
RTSA(7)	p. 5	Request To Send from J7 tristate-multiplexed to A bus
TXD(7)	p. 6	Transmitted Data from J7 tristate-multiplexed to B bus
DTR B(7)	p. 6	Data Terminal Ready from J7 tristate-multiplexed to B bus
RTS B(7)	p. 6	Request To send from J7 tristate-multiplexed to B bus
RXD(8)	J8	Received Data to J8 V24-levels
DSR(8)	J8	Data Set Ready to J8 V24-levels
CTS(8)	J8	Clear To Send to J8 V24-levels
CD(8)	J8	Carrier Detect to J8 V24-levels
TXDA(8)	p. 5	Transmitted Data from J8 tristate-multiplexed to A bus
DTRA(8)	p. 5	Data Terminal Ready from J8 tristate-multiplexed to A bus
RTSA(8)	p. 5	Request To Send from J8 tristate-multiplexed to A bus
TXD(8)	p. 6	Transmitted Data from J8 tristate-multiplexed to B bus
DTR B(8)	p. 6	Data Terminal Ready from J8 tristate-multiplexed to B bus
RTS B(8)	p. 6	Request To send from J8 tristate-multiplexed to B bus



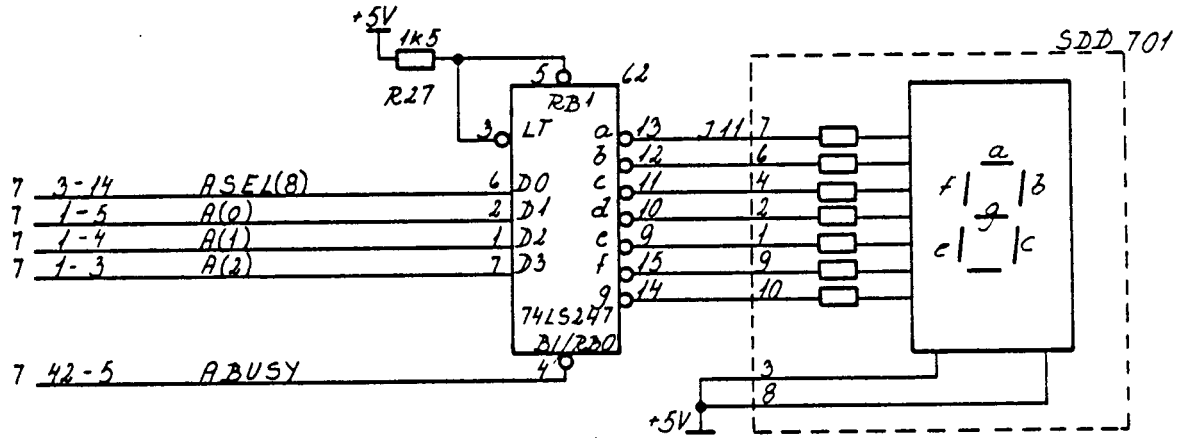
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Port 7 and Port 8

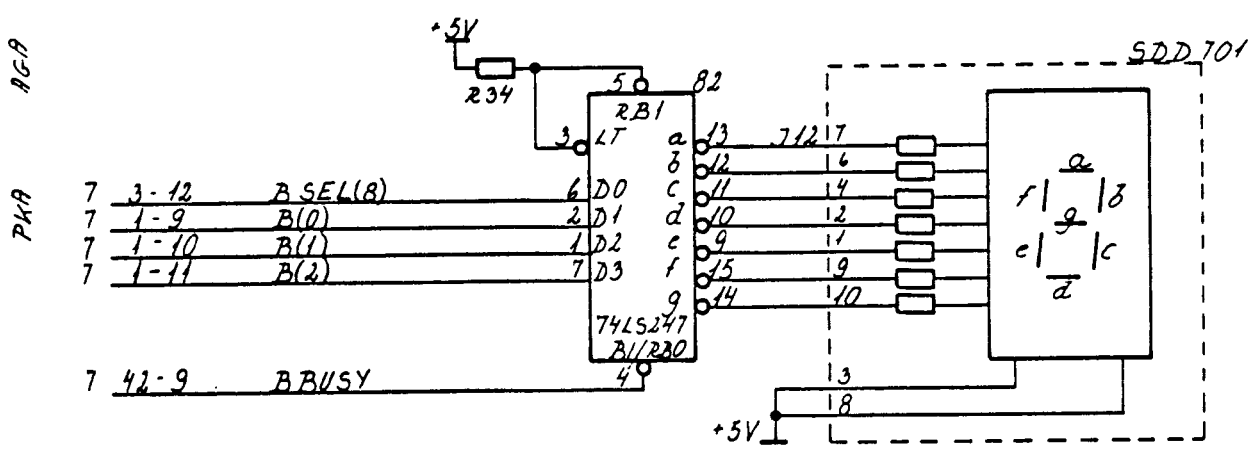
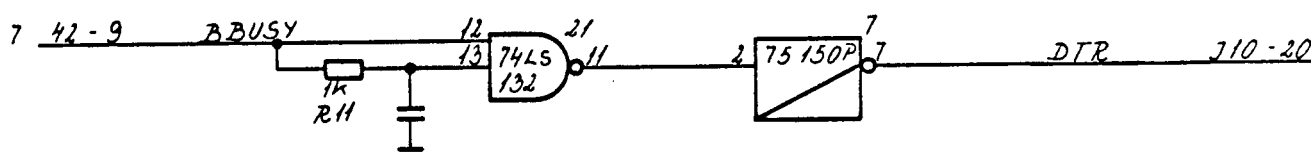
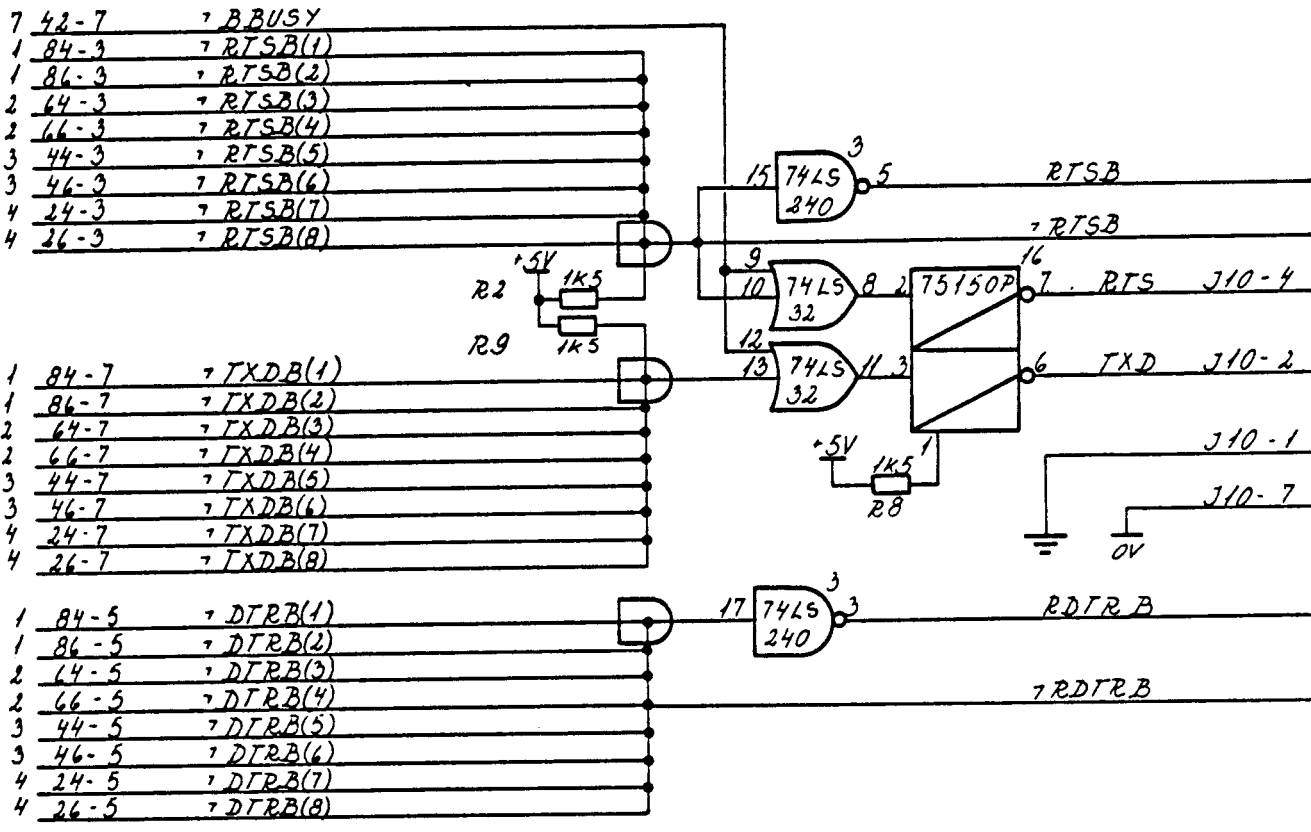
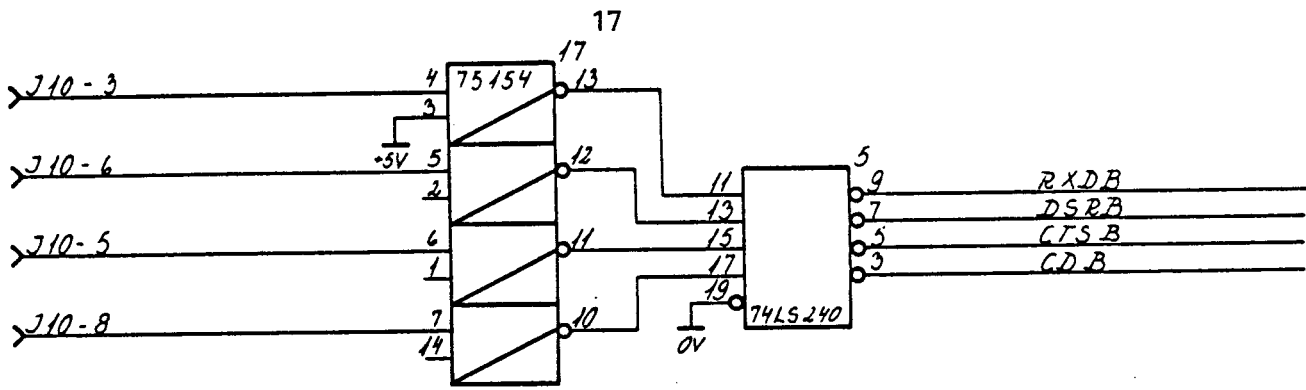
Signal	Destination	Description
RXDA	p. 1. 2. 3. 4	Received Data to J9
DSRA	p. 1. 2. 3. 4	Data Set Ready to J9
CTSA	p. 1. 2. 3. 4	Clear To Send to J9
CDA	p. 1. 2. 3. 4	Carrier Detected from J9
RTSA(7)	p. 5, 7	Request To Send from A bus V24-levels
TXD	J9	Transmitted Data to J9 V24-levels
RDTR A, RDTR A	p. 7	Data Terminal Ready from A bus
DTR	J9	Data Terminal Ready to J9 V24-levels



ACA
PKA



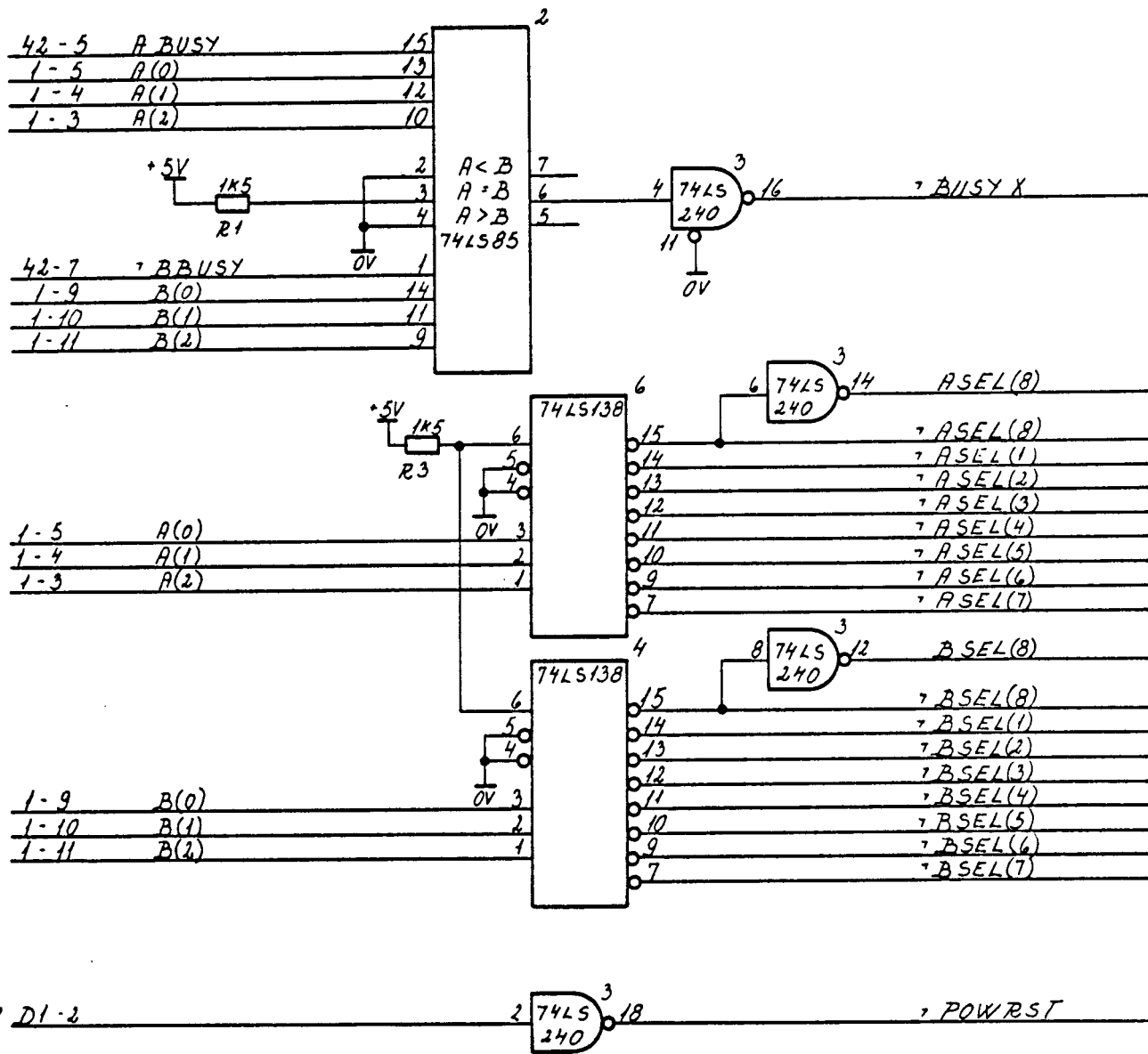
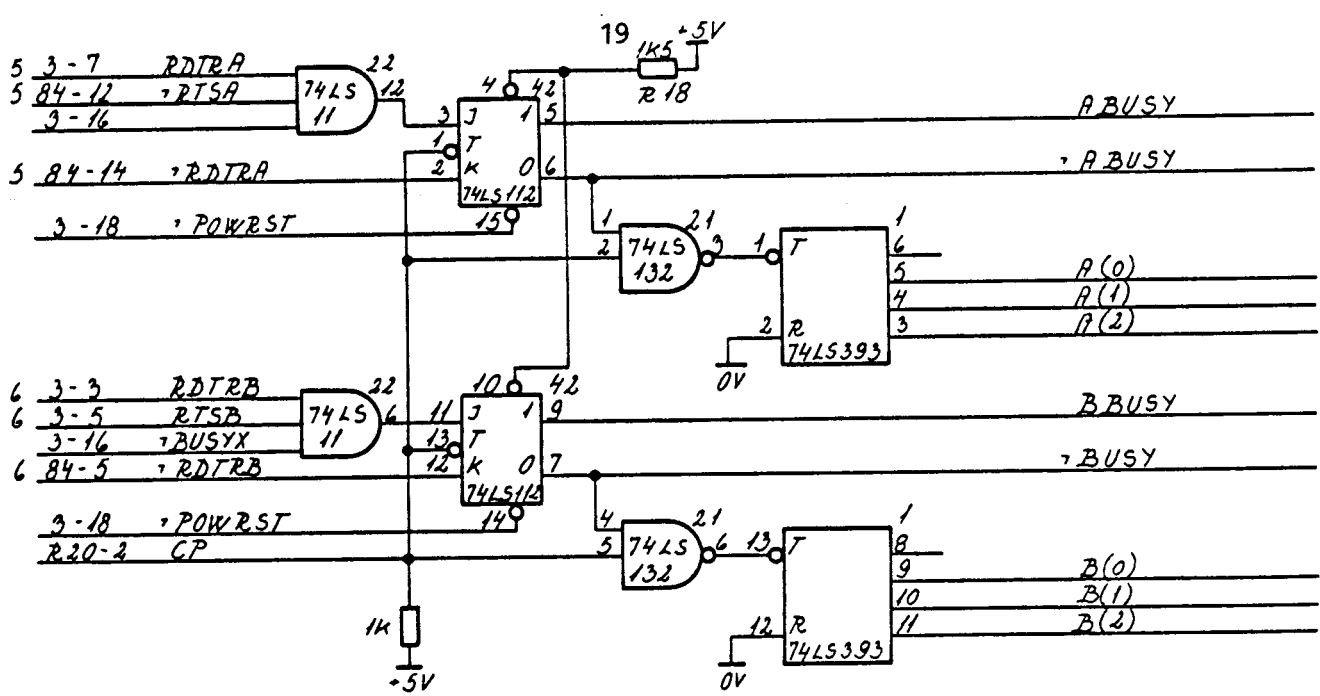
Signal	Destination	Description
RXDB	p. 1. 2. 3. 4	Received Data from J10
DSRB	p. 1. 2. 3. 4	Data Set Ready from J10
CTSB	p. 1. 2. 3. 4	Clear To Send from J10
CDB	p. 1. 2. 3. 4	Carrier Detected from J10
RISB	p. 7	Request To Send from B bus
TRISB	p. 5	
RIS	J10	Request To Send to J10 V24-levels
TXD	J10	Transmitted Data to J10
TRDTR B, DTR B	p. 7	Data Terminal Ready from B bus
DTR	J10	Data Terminal Ready to J10 V24-levels



LIS 701
R 13104

Port B

Signal	Destination	Description
ABUSY	p. 5, 7	port A busy, indicates that
\neg ABUSY	p. 1, 2, 3, 4, 7	A(0:2) points at an input port which is currently connected to port A.
A(0:2)	p. 5, 7	A-Scanner output
BBUSY	p. 6, 7	port B busy, indicates that
\neg BBUSY	p. 1, 2, 3, 4, 7	B(0:2) points at an input port which is currently connected to port B.
\neg BUSYX	p. 7	low when both scanners point at same input port, and one is busy. Used to prevent one input from connecting to both outputs, at the same time.
\neg ASEL(1), \neg ASEL(2), \neg ASEL(3), \neg ASEL(4), \neg ASEL(5), \neg ASEL(6), \neg ASEL(7), \neg ASEL(8)	p. 1 p. 2 p. 3 p. 4	tristate-enable signals for the A bus.
ASEL8	p. 5	most significant bit of A(-1:2)
\neg BSEL(1), \neg BSEL(2), \neg BSEL(3), \neg BSEL(4), \neg BSEL(5), \neg BSEL(6), \neg BSEL(7), \neg BSEL(8)	p. 1 p. 2 p. 3 p. 4	tristate-enable signals for the B bus.
BSEL8	p. 6	most significant bit of B(-1:2)

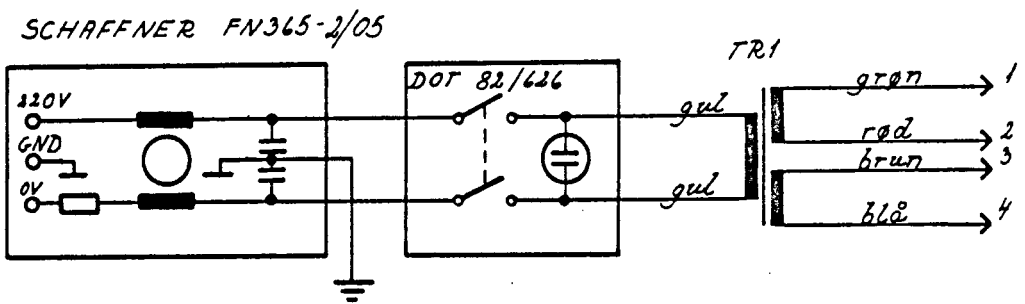
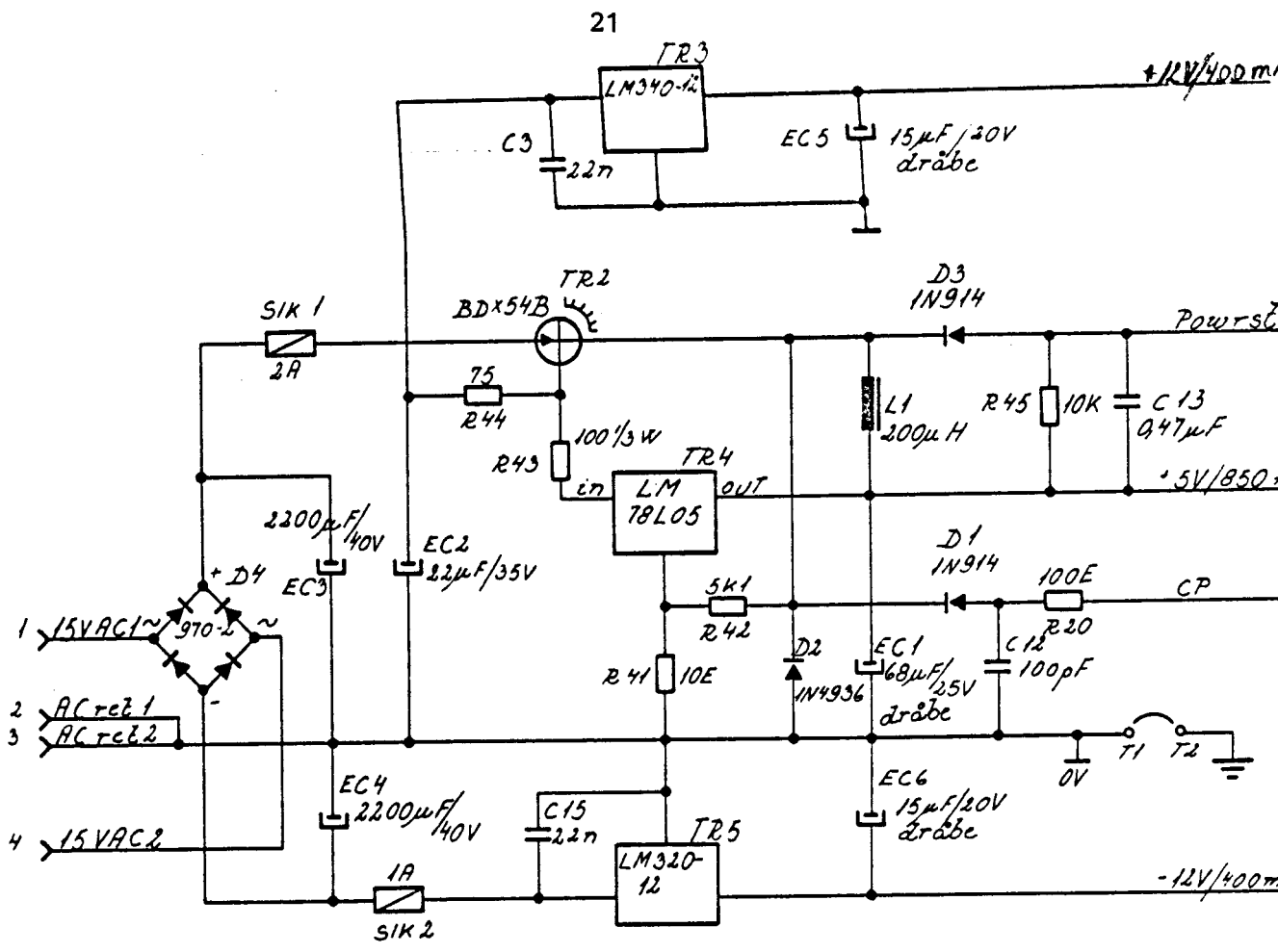


PGA
AGA

LIS 701
R 13105

control

Signal	Destination	Description
12 V/400 mA, -12 V/400 mA		Power supply for V24 transmitters
+5 V/850 mA		Power supply for all logic circuits, and LED-displays.
T1, T2		Jumper is installed, when signal ground is required connected to protective ground.
Powrst	p. 7	Logic reset signal, goes low when 5 V regulator starts switching (when 5 V is up).
CP	p. 7	Clockpulse for driving the scanners, derived from the 5 V switches. Frequency is about 30 KHz.



PKA
 AGR

LIS 701
 R 13106

Power supply

RETURN LETTER

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THE TWO-SIDED FLOPPY DISK DRIVE YD-174
Maintenance Manual

Keywords: RC700, RC702, RC762, Floppy Disk Drive, FDD711, FDD712.

Abstract: This manual is produced by Y-E DATA INC. JAPAN and it may be distributed according to an agreement between Y-E DATA and RC Computer.
RC Computer uses the technical numbers FDD711 and FDD712 for the floppy disk drive.

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 **Y-E DATA**

THE TWO-SIDED FLOPPY DISK DRIVE

YD-174

MAINTENANCE MANUAL

REVISION			
REV.	DESCRIPTION	DATE	DRIVE S/N APPLIED
A	PRELIMINARY	10.31.77	
B	J2 AND J3 CONNECTOR PIN ASSIGNMENT CHANGES AND EDITORIAL CHANGES ALL PAGES	4.3.'78	-06-XXX
C	LOW CURRENT PIN ASSIGNMENT CHANGE FROM J1-24 TO J1-2 PAGE 29,34	5.6.'78	-07-XXX
D	TAP-TAP RELIABILITY IMPROVEMENT	11.27.78	-10-XXX
E	PAGE 33	12.14.'78	-10-XXX
DRWN	<i>J. Sakai</i>	Y E DATA THE TWO-SIDED FLOPPY DISK DRIVE YD-174 PRODUCT SPECIFICATION	
CHK			
APPD	<i>J. Tatum's</i>	DWG No. FDB-527007	REV. E
APPD	<i>K. H. W. T. S. H.</i>		
		SHEET 1 OF 53	

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1.0 GENERAL

This manual contains the instructions required to maintain the YD-174. The information is provided in the form of preventive maintenance, corrective maintenance and recommended spare part list.

2.0 MAINTENANCE TOOLS

The special tools required to maintain the YD-174 are listed below:

tool	Y-E DATA Part Number
1. Tool Kit	140263-01
Screw driver	140264-01
Tweezer	140265-01
Setscrew wrench, 1.5	140266-01
Setscrew wrench, 2.0	140266-02
Feeler guage, 0.500 mm	140267-01
Feeler guage, 0.530 mm	140267-02
Inspection mirror	140268-01
Cutter	140269-01
Needle-nose pliers	140364-01
2. CE disk	140272-01

3.0 MAINTENANCE LEVEL

The maintenance is divided into two categories; preventive maintenance and corrective maintenance.

The corrective maintenance on this manual is divided into two levels; level 1 and level 2.

The maintenance level 1 includes removal/replacement of printed wired board (PWB) and five photo sensor assemblies and also contains drive belt and steel belt wiper.

The maintenance level 2 includes removal/replacement of all mechanical assemblies including that of level 1.

4.0 PREVENTIVE MAINTENANCE

4.1 GENERAL

Under normal circumstances preventive maintenance is not required on the YD-174. If severely dirty environments are encountered, an occasional cleaning of the drive may be performed to assure continued reliable performance.

4.2 VISUAL CHECK

Visual inspection is the first step in any maintenance operation.

Always look for corrosion, dirt, wear, binds, and loose connections.

Noticing these items may save downtime later..

4.3 CLEANING

Cleanliness cannot be overemphasized in maintenance of the YD-174.

CAUTION; The head/carriage assembly is a factory-adjusted and tested assembly. Do not try to adjust or repair this internal component. Do not, for any reason, clean the read/writeheads. To do so would cause severe damage to the head surfaces or head spring supports.

Parts	Observe	Procedure
1. Main Frame	Inspect for loose screws, connectors, switches, etc.	Clean main frame
2. Drive Belt	Frayed or weakend area	Change new belt

5.0 MAINTENANCE LEVEL 1

This section contains the detail maintenance procedure on the assemblies listed below.

- 5.1 PWB
- 5.2 INDEX LAMP ASSEMBLY
- 5.3 INDEX SENSOR ASSEMBLY
- 5.4 TRACK 00 SENSOR ASSEMBLY
- 5.5 WRITE PROTECT SENSOR ASSEMBLY
- 5.6 IN USE LED
- 5.7 WIPER
- 5.8 DRIVE BELT AND DRIVE PULLEY

5.1 PWB REMOVAL AND REPLACEMENT

CAUTION: Check the drive serial number on the main frame, to replace the PWB. (See Fig.1, page 25).

1. For the drive serial number from S/N 001-xxx to S/N 009-xxx with label [3] near AC connector, or from S/N 010-xxx, use only PWB PN 110018-02. Do not use PWB PN 110018-01.
2. For the drive serial number from S/N 001-xxx to S/N 009-xxx without label [3] near AC connector, use only PWB PN 110018-01.

NOTE: To modify the PWB PN 110018-02 into PN 110018-01, follow the procedure below.

1. Cut the three (3) components (49C, 50c, and 39D) on the PWB.
 2. Change PWB PN from 110018-02 to 110018-01.
1. Disconnect four connectors (J1, J2, J3, J5) from PWB.
 2. Remove two mounting screws near J1 connector and loosen two screws.
 3. Slide PWB away from stepper and remove it.
 4. Reverse the procedure for replacement.

5.2 INDEX LAMP ASSEMBLY

5.2.1 SERVICE CHECK

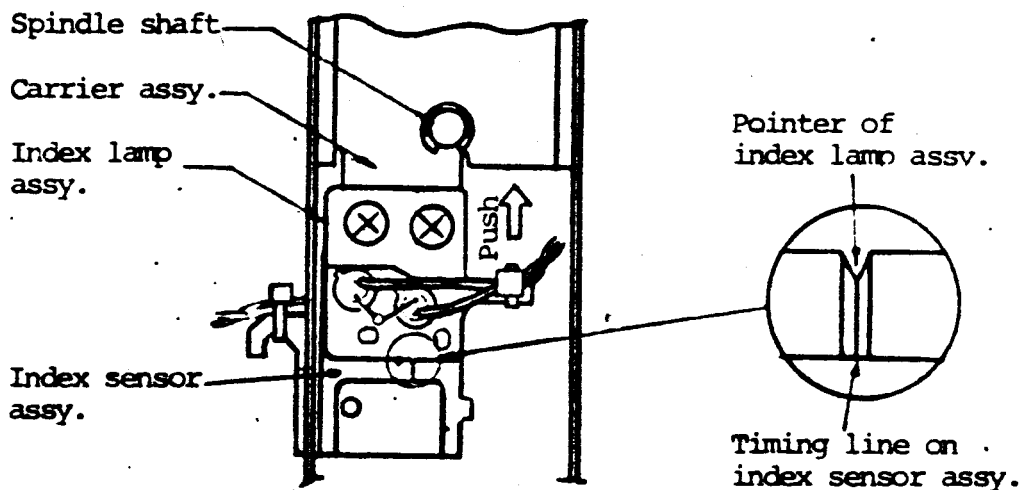
1. Turn on power.
2. Verify voltage of 2.0 to 3.4 V between "J2-16" and " GND " test points on PWB.

5.2.2 REMOVAL AND REPLACEMENT

1. Disconnect J2 connector from PWB.
2. Remove two lamp leads from J2 connector by pushing down on tabs with a tweezer, (BLACK to J2-A8, RED to J2-B8)
3. Remove cable clamp and lamp cable.
4. Remove two mounting screws and lamp assembly.
5. Reverse the procedure for replacement.

NOTE; When installing the assembly, align the pointer of lamp assembly with the timing line of index sensor assembly and tighten two mounting screws by pushing lamp assembly against carrier stop away from the front door.

CAUTION; Make sure the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.



5.3 INDEX SENSOR ASSEMBLY

5.3.1 SERVICE CHECK

1. Turn on power.

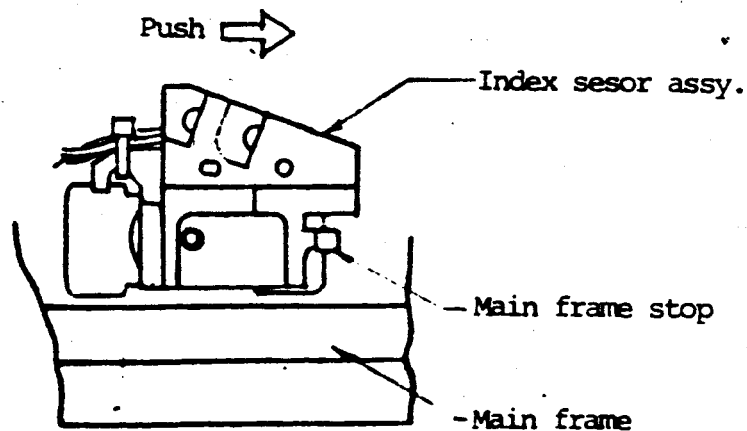
2. Verify the voltage of 4 to 5.25 V when door closed without a Diskette, 0 to 0.3 V when a Diskette inserted backward and door closed, between "J2-A7" and " GND " test points on PWB.
3. Repeat the same ptocedure between "J2-A6" and " GND " test points on PWB.
4. Remove the Diskette.

5.3.2 REMOVAL AND REPLACEMENT

1. Disconnect J2 connector from PWB.
2. Remove four SENSOR leads from J2 connector by pushing down on tabs with a tweezer.(BLACK to J2-A7 RED to J2-B7, BLUE to J2-A6, ORANGE to J2-B6)
3. Remove, screw, washer and assembly.
4. Reverse the procedure for replacement.

NOTE; When installing assembly, push it against the main frame stop away from its cable.

CAUTION; Make sure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.



5.4 TRACK 00 SENSOR ASSEMBLY

5.4.1 SERVICE CHECK

1. Position the head/carriage by hand to its limit away from spindle (the outer of TRACK 00).
2. Turn on power.

NOTE: This positions head/carriage to TRACK 00.

3. Verify voltage of 1.0 to 1.7 V between "J2-B12" and "GND" test points on PWB without a Diskette.
4. Verify voltage of 0 to 0.3 V between "J2-A11" and "GND" test points on PWB.
5. With power off, move the head/carriage by hand toward spindle, 4 stepper detent positions. (TRACK 04)
6. With power on, verify voltage of 4.0 to 5.25 V between the same test points in step 4

5.4.2 REMOVAL AND REPLACEMENT

1. Disconnect J2 connector from PWB.
2. Remove four leads from J2 connector by pushing down on tabs with a tweezer. (BLUE to J2-A12 ORANGE to J2-B12 BLACK to J2-A11 RED to J2-B11)
3. Remove a mounting screw and assembly.

NOTE: When installing assembly, inspect its two pins into main frame holes and tighten a screw.

CAUTION: Make sure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.

5.5 WRITE PROTECT SENSOR ASSEMBLY

5.5.1 SERVICE CHECK

1. Turn on power.
2. Verify voltage of 1.0 to 1.7 V between J2-B14 and "GND" test points on PWB without a Diskette.
3. Verify voltage of 4 to 5.25 V when door closed and 0 to 0.3 V when a Diskette without a write protect notch is inserted, and the door closed, between "J2-A13" and "GND" test points on PWB.
4. Remove the Diskette.

5.5.2 REMOVAL AND REPLACEMENT

1. Disconnect J2 connector from PWB.
2. Remove four leads from J2 connector by pushing down on tabs with a tweezer. (BLUE to J2-A14 ORANGE to J2-B14 BLACK to J2-A13 RED to J2-B13)
3. With door open, remove the bail mounting screw, washer and bail. (6.4)
4. Remove a screw and assembly.
5. Reverse the procedure for replacement.

NOTE; When installing assembly, insert its pin into the main frame hole and tighten a screw.

CAUTION; Make sure that the locking tabs on the terminals engage in the connector slot to prevent the leads from pushing out when plugged in.

5.6 IN USE LED REMOVAL AND REPLACEMENT

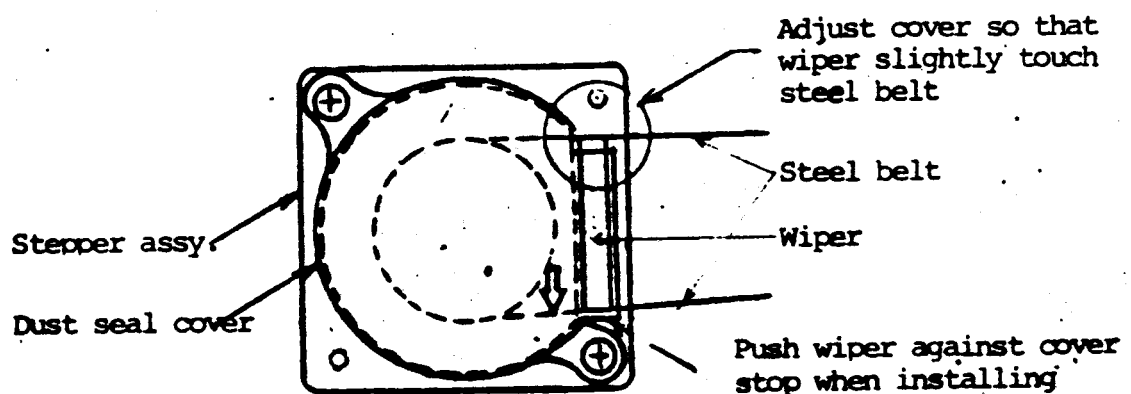
1. Disconnect J2 connector from PWB.
2. Remove two leads from J2 connector by pushing down on tabs with a tweezer. (BLACK to J2-A15 RED to J2-B15)
3. Remove LED holder and LED.
4. Reverse the procedure for replacement.

5.7 STEEL BELT WIPER REMOVAL AND REPLACEMENT

1. With door open, remove two screws and pop-up assembly.
2. Remove 2 screws and dustseal cover.
3. Remove wiper from dustseal cover.
4. Reverse the procedure for replacement.

NOTE; When installing a new wiper into dustseal cover, push it against the cover stop toward the arrow direction on cover.

CAUTION; When installing dustseal cover on stepper, align the dustseal cover so that wiper may slightly touch steel belt between head/carriage and pulley.



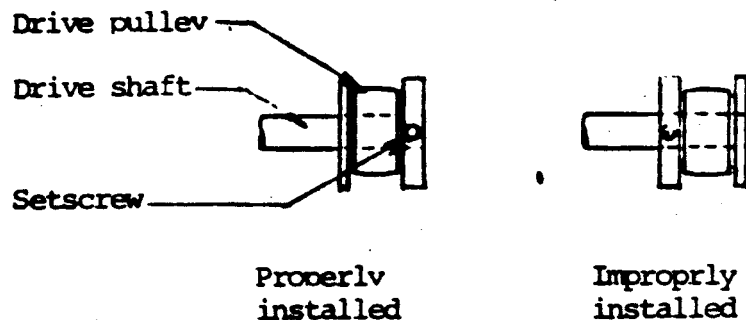
5.8 DRIVE BELT AND PULLEY, REMOVAL AND REPLACEMENT

1. Remove PWB. (5.1)
2. Remove belt.
3. Loosen a setscrew and remove pulley from motor shaft.

4. Reverse the procedure for replacement. Align the set-screw with the flat surface of motor shaft.

NOTE; Check that the surface of pulley is aligned with the end of motor shaft.

NOTE; Check that the belt is riding on center of spindle pulley and drive pulley, rotating spindle pulley counterclockwise by hand.



6.0 MAINTENANCE LEVEL 2

This section contains the detail maintenance procedure on the listed below.

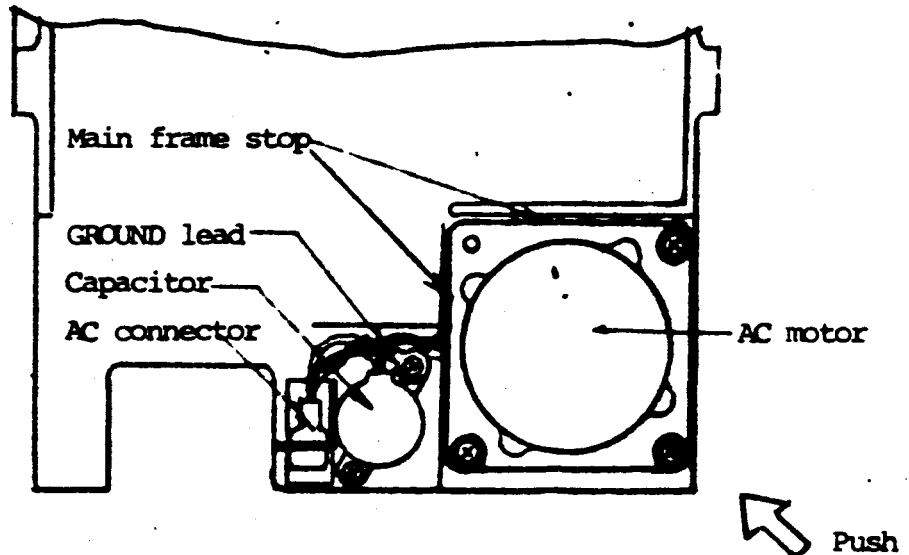
- 6.1 DRIVE MOTOR ASSEMBLY
- 6.2 CARRIER ASSEMBLY
- 6.3 POP-UP ASSEMBLY
- 6.4 BAIL ASSEMBLY
- 6.5 HEAD LOAD ASSEMBLY
- 6.6 FRONT BESEL ASSEMBLY
- 6.7 DOOR LOCK SOLENOID ASSEMBLY
- 6.8 HEAD/CARRIAGE ASSEMBLY
- 6.9 STEEL BELT
- 6.10 STEPPER ASSEMBLY
- 6.11 IDLER ASSEMBLY
- 6.12 SPINDLE BEARINGS

6.1 DRIVE MOTOR ASSEMBLY REPLACEMENT AND REPLACEMENT

1. Remove PWB (5.1) and belt.
2. Loosen a pulley setscrew and remove it from motor shaft.
3. Remove AC connector from connector clamp by pushing down on the latch.
4. Remove two screws holding capacitor clamp to main frame.
5. Remove three screws and drive motor assembly.
6. Reverse the procedure for installation.

NOTE; When installing motor, push it two main frame stops, toward front door and AC connector clamp.

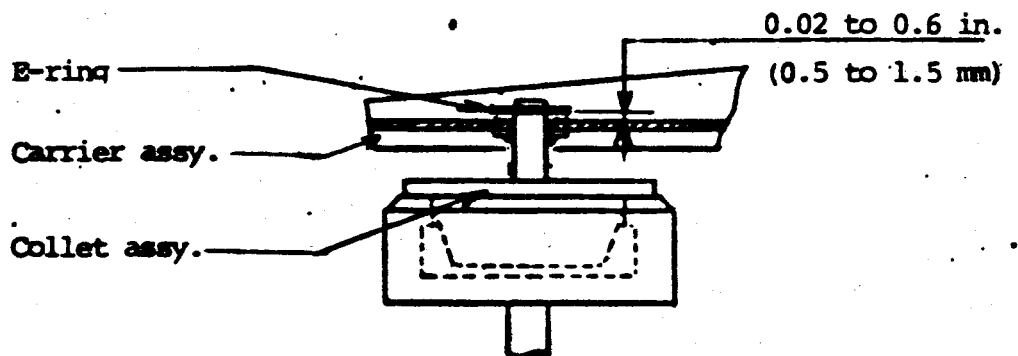
NOTE; Make sure ground lead is installed on capacitor clamp.



6.2 CARRIER ASSEMBLY

6.2.1 SERVICE CHECK

1. Close the door.
2. Verify gap of 0.02 to 0.06 in. (0.5 to 1.5 mm) between carrier and E-ring of collet assembly shaft.



6.2.2 CARRIER ACCESS .

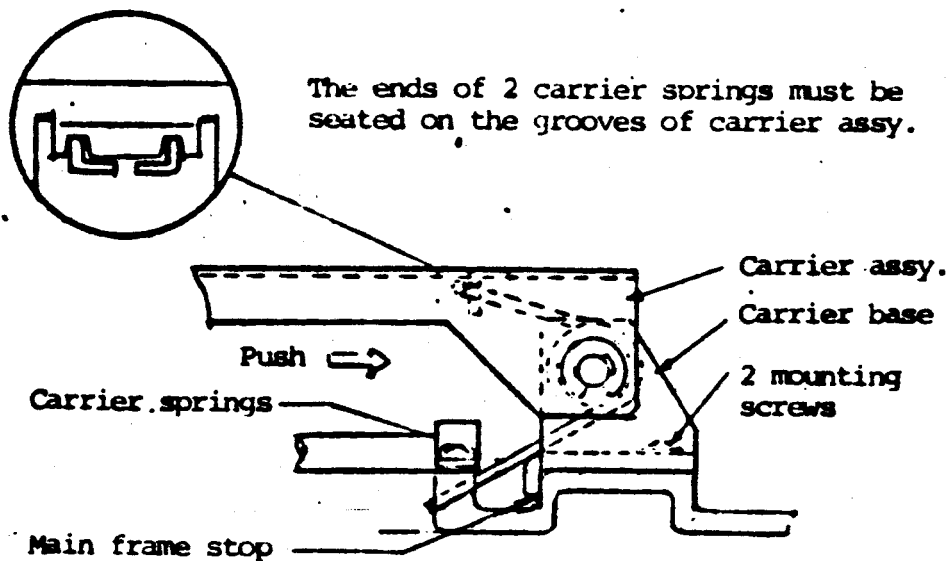
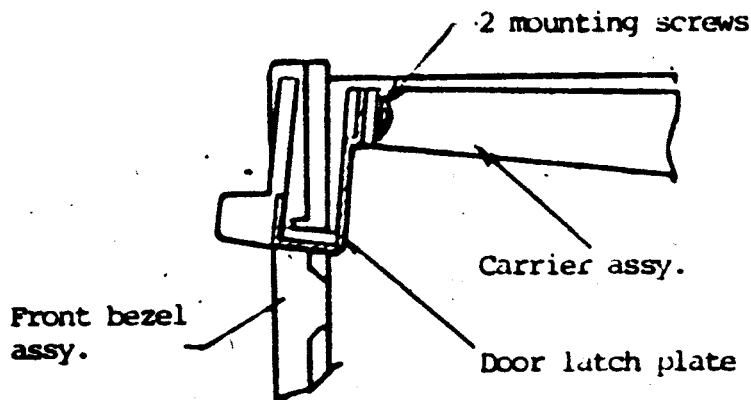
1. Remove two screws holding carrier to door latch plate.
2. Swing carrier up carefully.

CAUTION; Carrier is spring loaded, take care when opening carrier.

3. Reverse the procedure to close carrier. Align the upper side of carrier with top edge of door latch plate at step 1.

NOTE; Ensure that two carrier springs are properly seated in the carrier grooves.

4. Do carrier service check. (6.2.1)



6.2.3 REMOVAL AND REPLACEMENT

1. Remove two screws and index lamp assembly. (5.2.2)
2. Remove cable clamp from carrier.
3. Remove two screws holding carrier to door latch plate.
4. Remove two screws holding carrier base to main frame.
5. Remove carrier.
6. Reverse the procedure for replacement.

NOTE; When installing assembly, push it against the main frame stop away from the front door and tighten two screws.

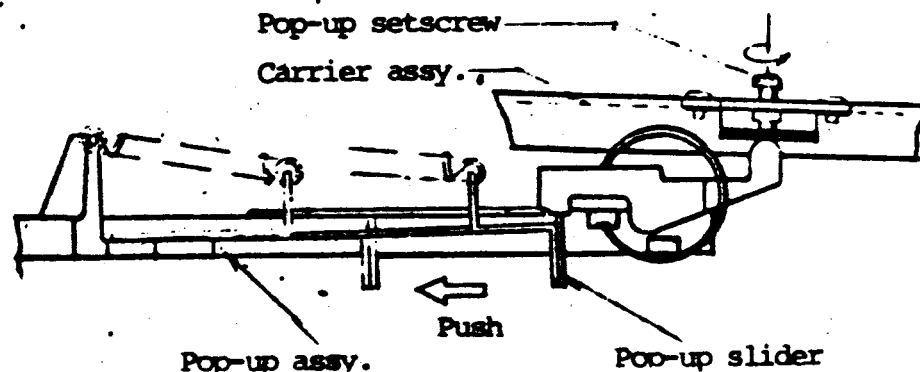
CAUTION; Check that the both ends of two carrier springs are properly seated in grooves.

7. Replace the index lamp assembly. (5.2.2)
8. Adjust the backstop screw. (6.5.2)
9. Adjust the pop-up setscrew. (6.3.2)

6.3 POP-UP ASSEMBLY

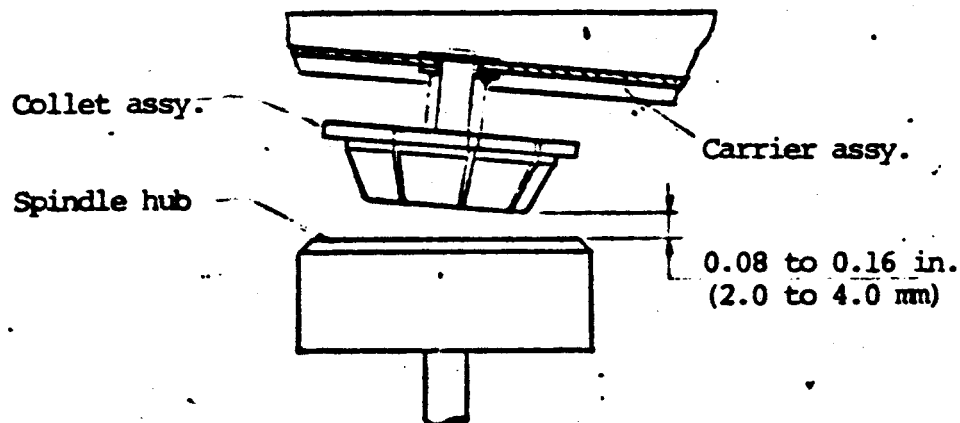
6.3.1 SERVICE CHECK

1. Insert a Diskette and close the door.
2. Push the button on front bezel, holding front door by hand.
3. Open the door slowly and hold it when a Diskette just ejected.
4. Verify gap of 0.08 to 0.16 in. (2 mm to 4 mm) between the surface of spindle hub and the end of collet assembly.



6.3.2 ADJUSTMENT

1. Rotate the pop-up setscrew on carrier assembly clockwise fulley.
2. With door close, latch the pop-up slider away from the front door.
3. Open the door slowly and hold the door looking for approximately 0.12 in. (3mm) gap between the surface of spindle hub and the end of collet assembly.
4. Rotate the screw clockwise spindle until pop-up slider is just unlatched.
5. Do service check. (6.3.1)



6.3.3 REMOVAL AND REPLACEMENT

1. Remove two screws holding assembly to frame.
2. To install, reverse the procedure.
3. Do service check. (6.3.1)

6.4 BAIL ASSEMBLY REMOVAL AND REPLACEMENT

CAUTION; The read/write heads must not be allowed to come together without a piece of clean paper inserted between the head surfaces.

1. Insert a piece of clean paper between the head surfaces.
2. Remove a mounting screw and washer.
3. Remove bail assembly, pulling away from solenoid.
4. Reverse the procedure for replacement.

NOTE; Check that the plunger must be moved when pushing its side.

CAUTION; When installing bail assy, make sure that it is under the carriage arm tab.

6.5 HEAD LOAD SOLENOID ASSEMBLY

CAUTION; The read/write heads must not be allowed to come together without a diskette or piece of clean paper inserted between the head surfaces.

CAUTION; Without removal of pop-up assembly, the head/carriage assembly would cause severe damage by diskette which may be ejected at the head load condition.

6.5.1 SERVICE CHECK

1. Remove pop-up assembly.
2. Insert a diskette and close the door.
3. With power on, energize the head load solenoid by installing a jumper between "HA" test points on PWB.
4. Verify gap of 0.02 to 0.04 in. (0.5 to 1.0 mm) between bail and carriage arm tab throughout carriage travel.
5. Remove jumper installed in step 3 and power off.
6. Remove a diskette and close the door.
7. Check the drive serial number on the frame.

NOTE; For the drive serial number from S/N 001-xxx to S/N 009-xxx without label 3 near AC connector, go to step 3

For the drive serial number from S/N 001-xxx to S/N 009-xxx with label 3 near AC connector or from S/N 010-xxx, go to step 10.

8. Look for gap of 0.06 to 0.1 in. (1.5 to 2.5 mm) between head surfaces.

NOTE; This gap cannot be measured and must be estimated using inspection mirror.

9. Go to step 14.
10. Move the head/carriage to approximately track 40.
11. Put the drive at horizontal position. (PWB at bottom side).
12. With power on, jumper the test points "HA" and then disconnect them by using extension wires.
13. Look for gap of 0.004 to 0.01 in. (0.1 to 0.25mm) between head surfaces.

NOTE; This gap cannot be measured and must be estimated using inspection mirror.

14. Replace the pop-up assembly.

6.5.2 ADJUSTMENT

1. Remove pop-up assembly.
2. Insert a diskette and close the door.

3. With power on, energize the head load solenoid by installing a jumper "HA" test points on PWB.
4. Loosen two solenoid setscrews slightly holding solenoid to its clamp.
5. Rotate a solenoid adjusting screw on solenoid clamp, for gap of 0.02 to 0.04 in. (0.5 to 1.0 mm) between bail and carriage arm tab.

NOTE; A clockwise rotation of screw decreases the gap.

6. Verify this gap throughout carriage travel.
7. Tighten two setscrews in step 4.
8. Remove jumper in step 3 and power off
9. Remove the diskette and close the door.
10. Check the drive serial number on the frame.

NOTE; For the drive serial number from S/N 001-xxx to S/N 009-xxx without [3] near AC connector, go to step 11.
For the drive serial number from S/N 001-xxx to S/N 009-xxx with label [3] near AC connector or S/N 010-xxx, go to step 13.

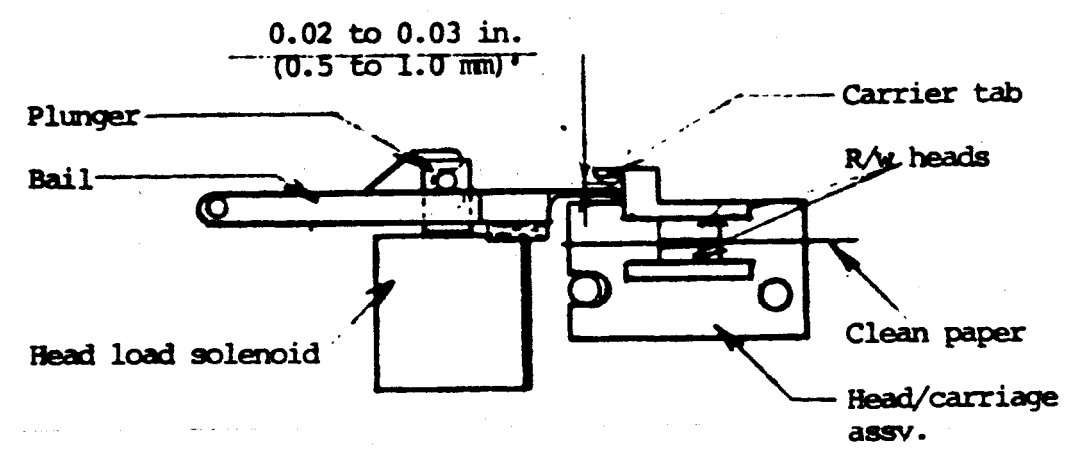
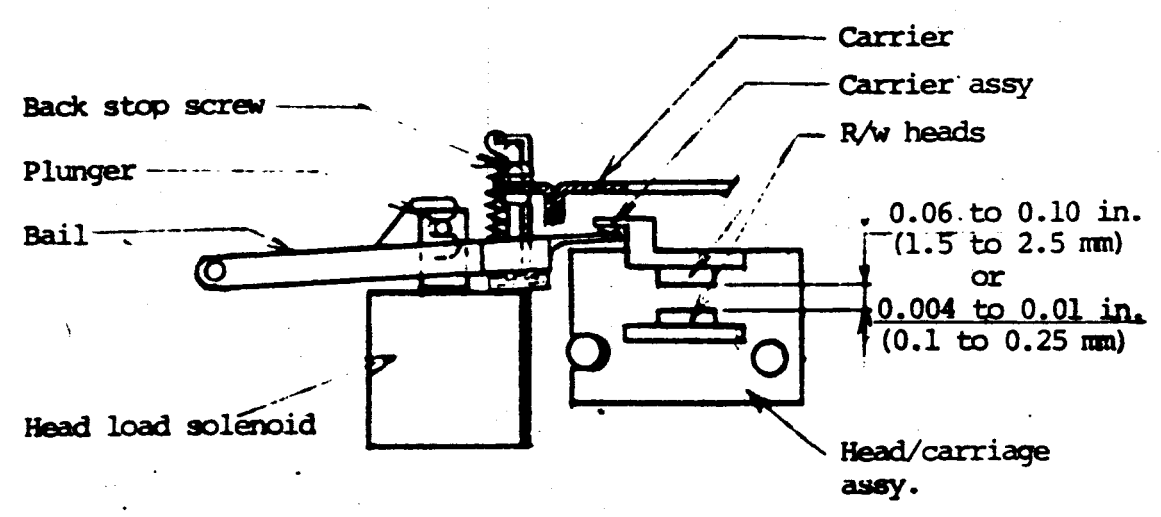
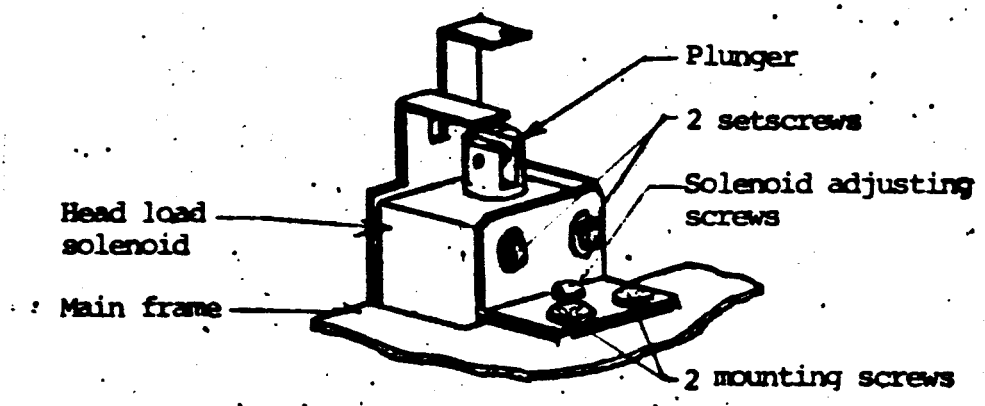
11. Look for gap of 0.06 to 0.1. (1.5 to 2.5mm) between head surfaces.

NOTE; This gap cannot be measured and must be estimated, using inspection mirror. To obtain this gap, turn back stop setscrew clockwise, until the heads just touch, then back open the heads by turning the screw one turn counterclockwise.

12. Go to step 15.
13. Move the head/carriage to approximately track 40.
14. Put the drive at horizontal position. (PWB at bottom side)
15. With power on, jumper the test points "HA" and then disconnect them by using extension wires.
16. Look for gap of 0.004 to 0.01 in. (0.1 to 0.25 mm) between head surfaces.

NOTE; This gap can not be measured and must be estimated using inspection mirror. A clockwise rotation of backstop setscrew decreases the gap.

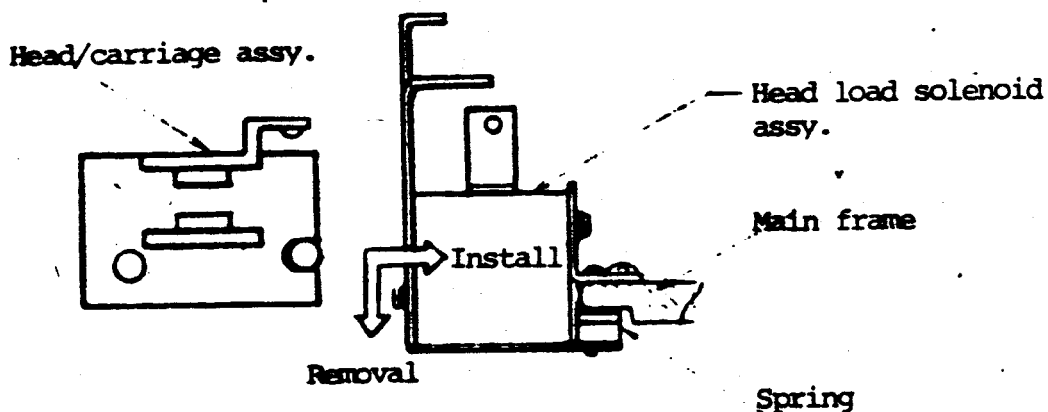
17. Do service check. (6.5.1)



6.5.3 REMOVAL AND REPLACEMENT

1. Remove PWB. (5.1) and belt.
2. Remove 2 leads from J2 connector by pushing down on tabs with a tweezer. (BLACK to J2-A1, RED to J2-B1)
3. Swing up carrier.
4. Insert a piece of clean paper between the head surfaces.
5. Remove bail assembly.
6. Remove bail return spring.
7. Remove two mounting screws holding clamp to frame and solenoid, moving it toward head/carriage and then downward.
8. Reverse the procedure for replacement.

CAUTION; Ensure that the bail is under tab of head/carriage arm.



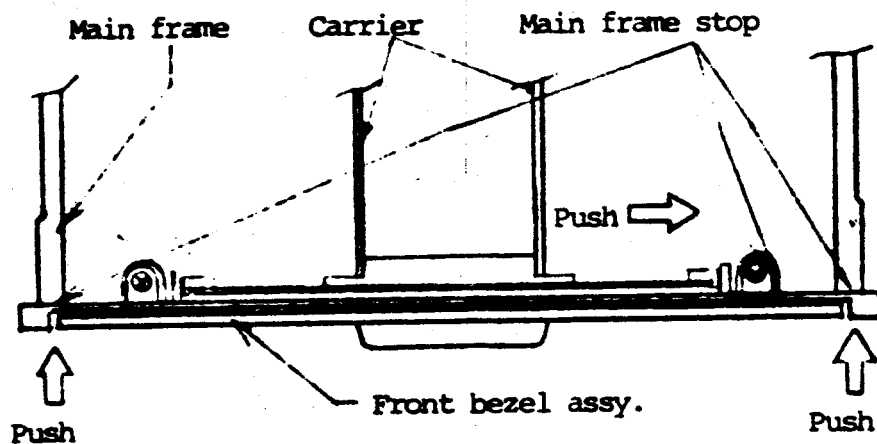
9. Do adjustment. (6.5.2)

6.6 FRONT DOOR ASSEMBLY REMOVAL AND REPLACEMENT

1. Remove J2 connector from PWR.
2. Remove two leads of door lock solenoid from connector by pushing down on tabs with a tweezer. (BLACK to J2-A2, RED to J2-B2)
3. Repeat same procedure to remove two leads of IN USE LED. (BLACK to J2-A15 RED to J2-B15)
4. Remove two screws holding carrier to door latch plate.
5. Remove two mounting screws and bezel assembly.
6. Reverse the procedure for replacement.

NOTE; When installing assembly, push it against two main frame stops, toward the spindle and pop-up assembly.

7. Do carrier service check. (6.2.1)



6.7 DOOR LOCK SOLENOID REMOVAL AND REPLACEMENT

1. Disconnect J2 connector.
2. Remove two leads from connector by pushing down on tabs with a tweezer. (BLACK to J2-A2, RED to J2-B2)
3. Remove two mounting screws and washers on front bezel.
4. Remove hook pin from hook and solenoid assembly.
5. Reverse the procedure for replacement.

6.8 HEAD/CARRIAGE ASSEMBLY

CAUTION; The head/carriage assembly is a factory-adjusted and tested assembly. Do not try adjust or repair this internal component. Do not, for any reason, clean the read/write heads. To do so would cause severe damage to the head surfaces or head spring supports.

CAUTION; The read/write head must not be allowed to come together without a piece of paper inserted between the head surfaces.

6.8.1 POSITION SERVICE CHECK

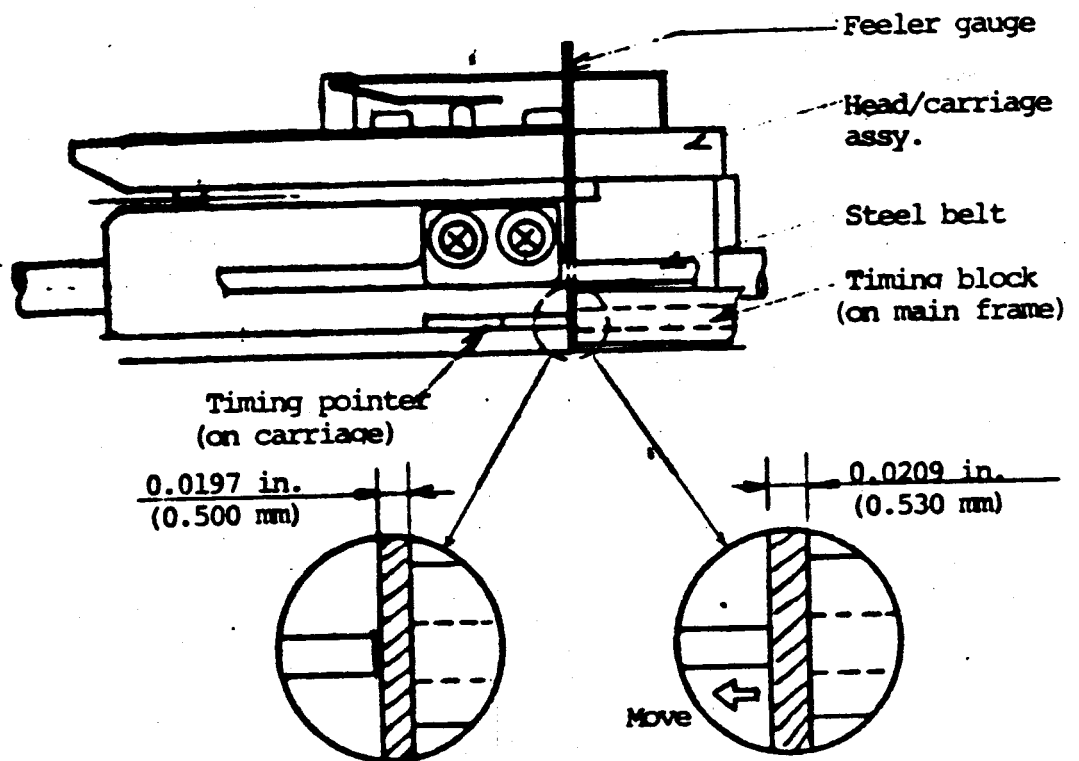
1. Remove pop-up assembly.
2. Insert a piece of clean paper between the head surfaces.
3. Position the head/carriage by hand for approximately 0.01 in. (0.25 mm) gap between timing pointer on carriage and timing block on frame.
4. With power on, electrically detent stepper to phase 0 by installing jumper "T40" test points on PWB.

NOTE; This moves the head/carriage assembly approximately 0.01 in. (0.25 mm) toward spindle and position it at track 40.

5. Verify that stepper pulley timing hole is aligned with the timing slot on stepper bracket.
6. Verify gap of 0.0197 to 0.0209 in. (0.500 to 0.530 mm) between timing pointer on carriage and timing block on frame by look for no motion of head carriage assembly when 0.0197 in. (0.500 mm) feeler gauge is inserted. Check for motion of head/carriage assembly when inserting a 0.0209 in. (0.530mm) feeler gauge.
7. If for some reason, verification in steps 5 to 6 is not positive, repeat steps 3 through 6.

NOTE; If still not positive, adjust assembly.
(6.8.2)

8. Remove jumper installed in step 4.
9. Remove paper from between head surfaces.
10. Replace pop-up assembly.



6.8.2 ADJUSTMENT

1. Remove pop-up assembly.
2. Insert a piece of clean paper between the head surfaces.
3. Position head/carriage by hand to track 40.
4. Loosen two steel belt/carriage clamping screws on head/carriage assembly.
5. Align stepper pulley timing hole with timing slot on stepper bracket.
6. With power on, install jumper between "T40" test points on PWB.
7. Verify that stepper pulley timing hole is aligned with the timing slot on stepper bracket.

NOTE; If this does not, replace stepper assembly.

8. Insert 0.0198 in. (0.500 mm) feeler gauge between timing pointer on carriage and timing block on frame.
9. With light pressure applied to top of carriage, tighten clamping screws.
11. Do position service check starting in step 6. (6.8.1)

6.8.3 REMOVAL AND REPLACEMENT

CAUTION; Before installing head/carriage assembly, insert a piece of clean paper between head surfaces.

CAUTION; When installing carriage assembly, make sure that bail assembly is under tab of the carriage arm with bail return spring properly installing.

1. Remove PWB.
2. Remove carriage cable clamp to flame.
3. Insert a piece of clean paper between head surfaces.
4. Swing the carrier.
5. Position carriage to approximately track 40.
6. Remove two steel belt/ carriage clamping screws and clamp.
7. Remove two guide bar clamping screws and clamp.
8. Carefully remove carriage assembly from drive.
9. Remove two guide bars from carriage.
10. Check the drive serial number on the frame.

NOTE; For the drive serial number from S/N 001-xxx to S/N 009-xxx without label [3] near AC connector, go to step 11

For the drive serial number from S/N 001-xxx to S/N 009-xxx with label [3] near AC connector or from S/N 010-xxx, go to step 15.

11. Check the carriage parts number just removed at at step 8

NOTE; For carriage PN 120028-01, use the same carriage parts number and go to step 12, or use carriage P/N 120028-02 and go to step 13.

For carriage PN 120028-02, use the same carriage parts number (P/N 120028-02) only. Do not use carriage 120028-01 and go to step 16.

12. Reverse the procedure for installation and go to step 17
13. Reverse the procedure for replacement.
14. Remove the bail return spring
15. Install the bail return spring P/N 140222-02 and go to step
16. Reverse the procedure for installation.
17. Do adjustment. (6.8.2)

6.9 STEEL BELT

6.9.1 REMOVAL

1. Remove pop-up assembly.
2. Position carriage to approximately track 40.
3. Remove two steel belt clamping screws and clamp on carriage.
4. Remove two mounting screws and dustseal cover.
5. Push idler slider against spring tension and remove steel belt from idler pulley.
6. Remove a steel belt clamping screw and clamp on stepper pulley.
7. Remove belt ends from stepper pulley pin and steel belt.

6.9.2 REPLACEMENT

1. Install belt ends on stepper pulley pin and replace clamp and screw, but do not tighten.
2. Replace belt around the idler pulley by pushing idler slider against spring tension.
3. Rotate stepper pulley and check that steel belt is centered in idler pulley throught travel several times.
4. Tighten stepper pulley clamping screw.
5. Replace dust seal cover. (5.7)
6. Replace two steel belt clamping screws and clamp on carriage.
7. Adjust carriage position. (6.8.2)

6.10 STEPPER ASSEMBLY REMOVAL AND REPLACEMENT

1. Disconnect J2 connector from PWB.
2. Remove five leads from connector and cable clamp (BLUE to J2-A5, RED to J2-A4, YELLOW to J2-B4, GREEN to J2-A3, WHITE to J2-B3)
3. Remove steel belt. (6.8)
4. Remove two mounting screws and stepper.
5. Reverse the procedure for installation.
6. Adjust head/carriage position. (6.8.1)

6.11 IDLER ASSEMBLY REMOVAL AND REPLACEMENT

1. Push idler slider against spring tension and remove the steel belt from idler.
2. Remove two mounting screws and idler.
3. Reverse the procedure for installation.

NOTE; When installing idler, push idler base toward stepper and tighten two mounting screws.

4. Check that steel belt is centered on idler pulley throughout travel.

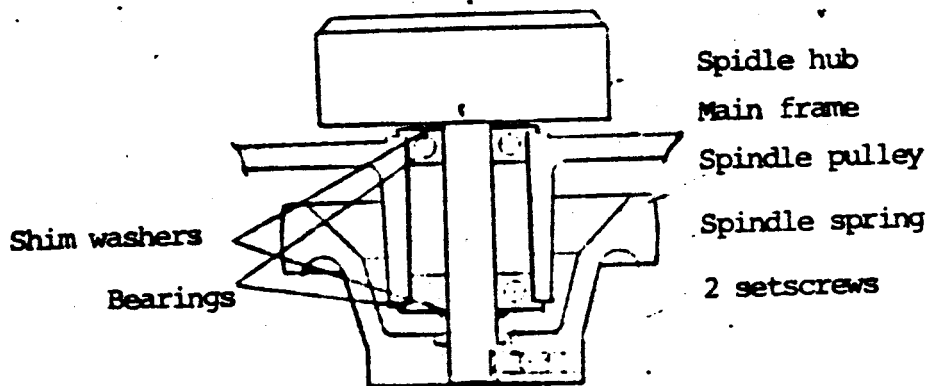
6.12 SPINDLE BEARINGS REMOVAL AND REPLACEMENT

1. Swing up carrier and turn drive to vertical position (side up, door forward).
2. Remove two setscrews holding spindle pulley.

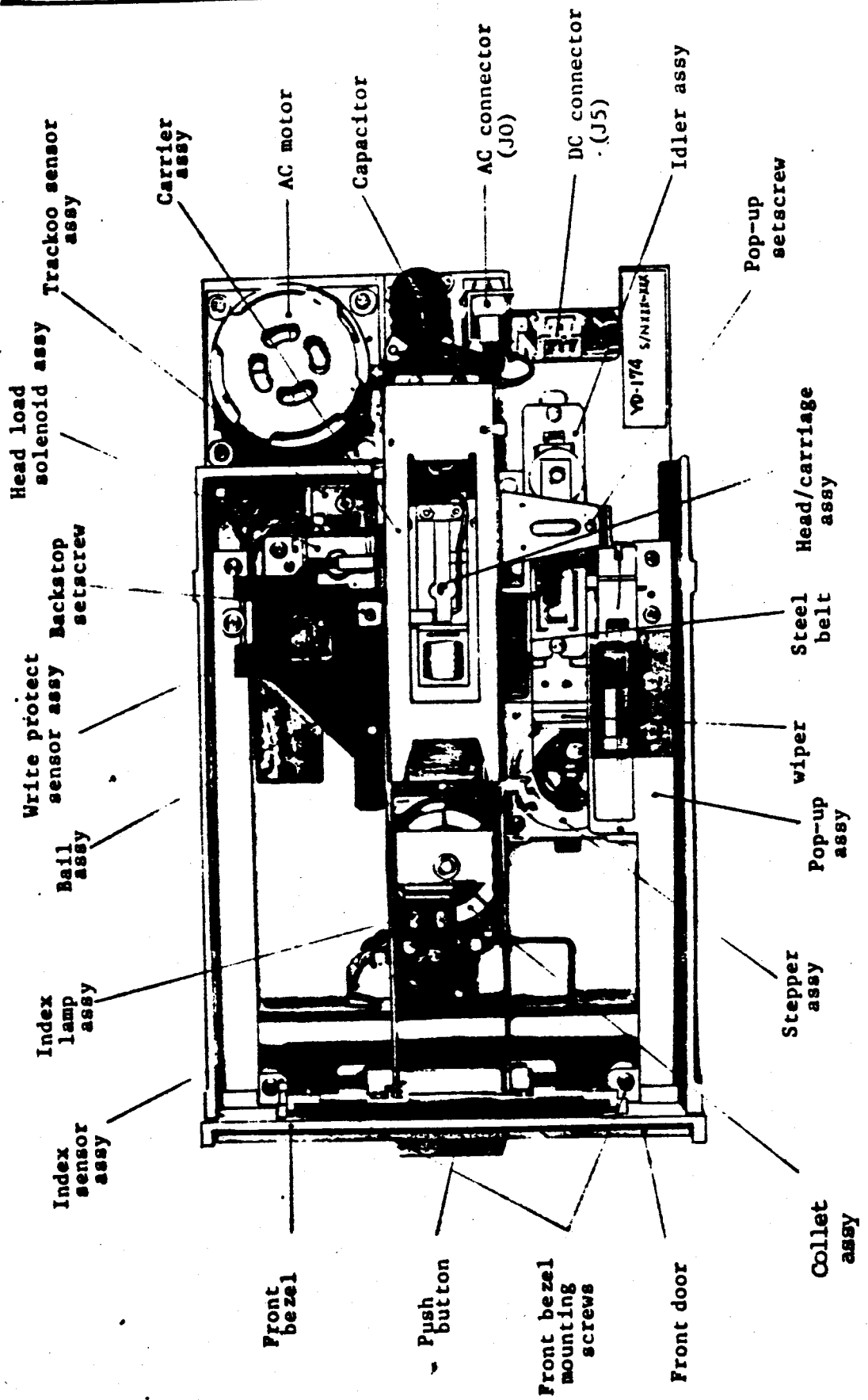
CAUTION; The spring-loaded pulley may fly out when the setscrews are removed.

3. Carefully withdraw spindle hub from opposite side of baseplate. Retain the shim washers which are on the spindle shaft.
4. Remove two spindle bearings from main frame.
5. Reverse the procedure for replacement.

NOTE; Use shim washers to obtain the same dimension as the old spindle. The distance from hub face, on which the Diskette sits, to the reference surface of baseplate should be identical to the unit previously removed.



1.0 PARTS/ASSEMBLIES LOCATIONS



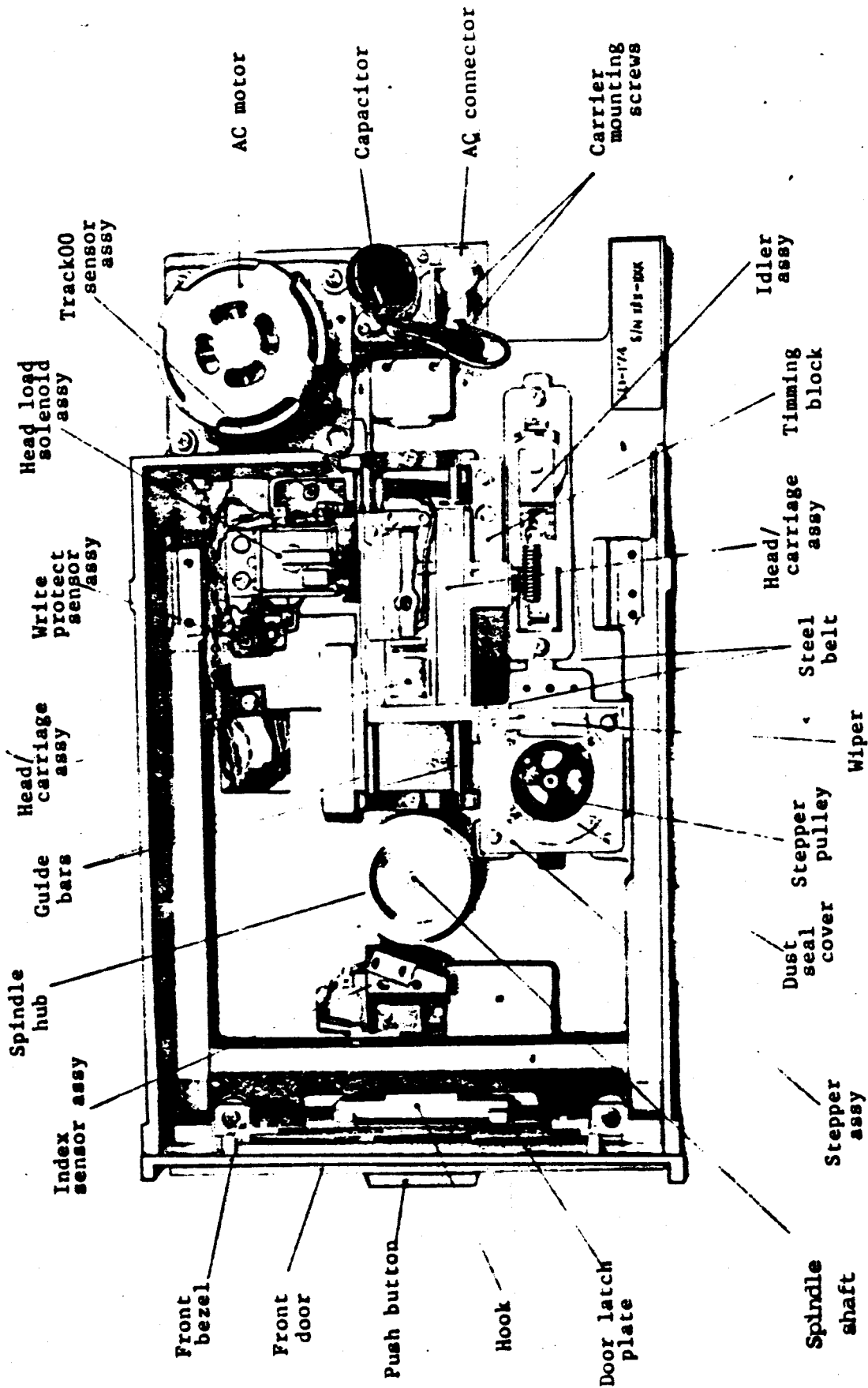


Fig.2 Top view of YD-174 with carrier, bail and pop-up assy removed

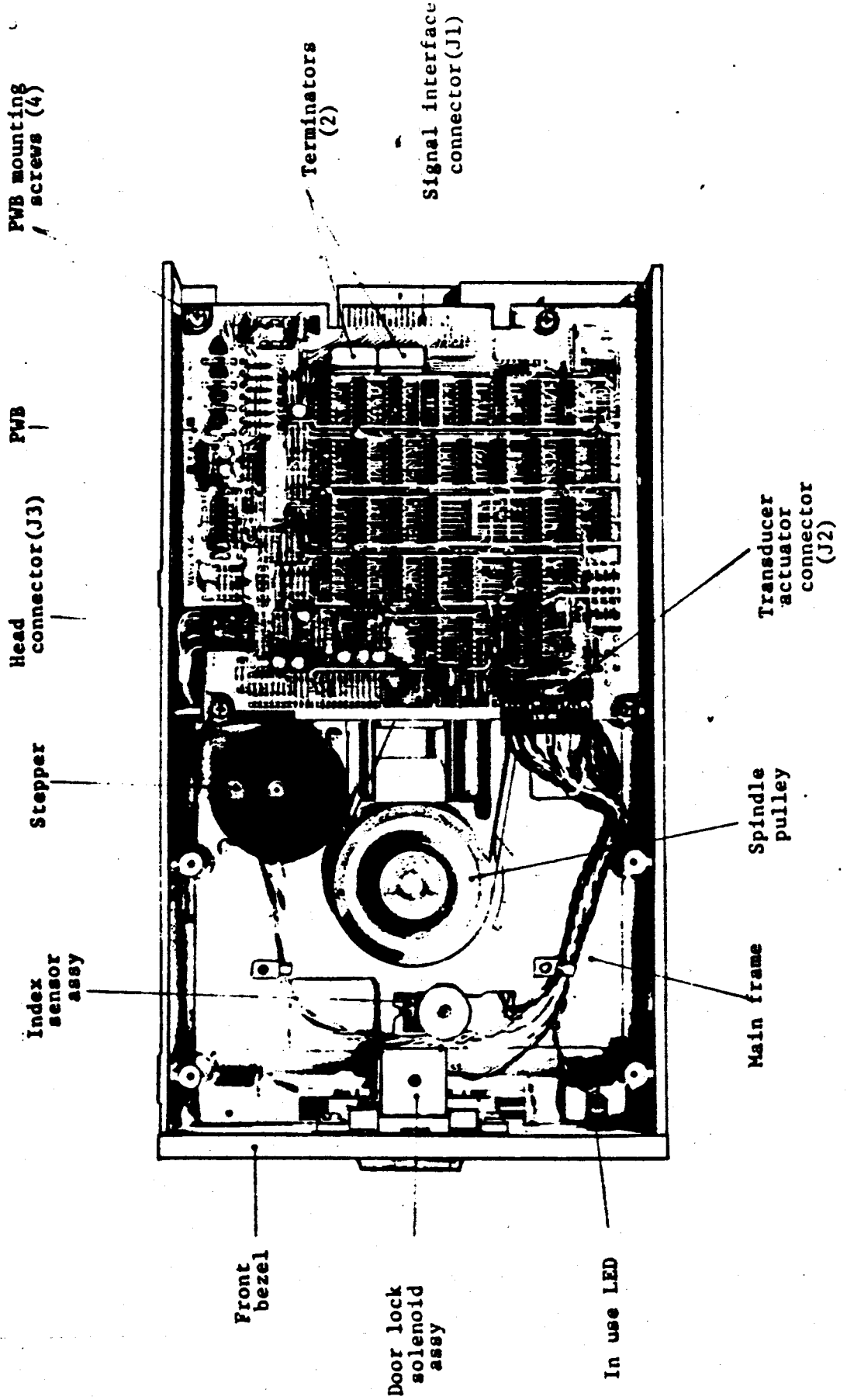


Fig. 3 Rear view of YD-174

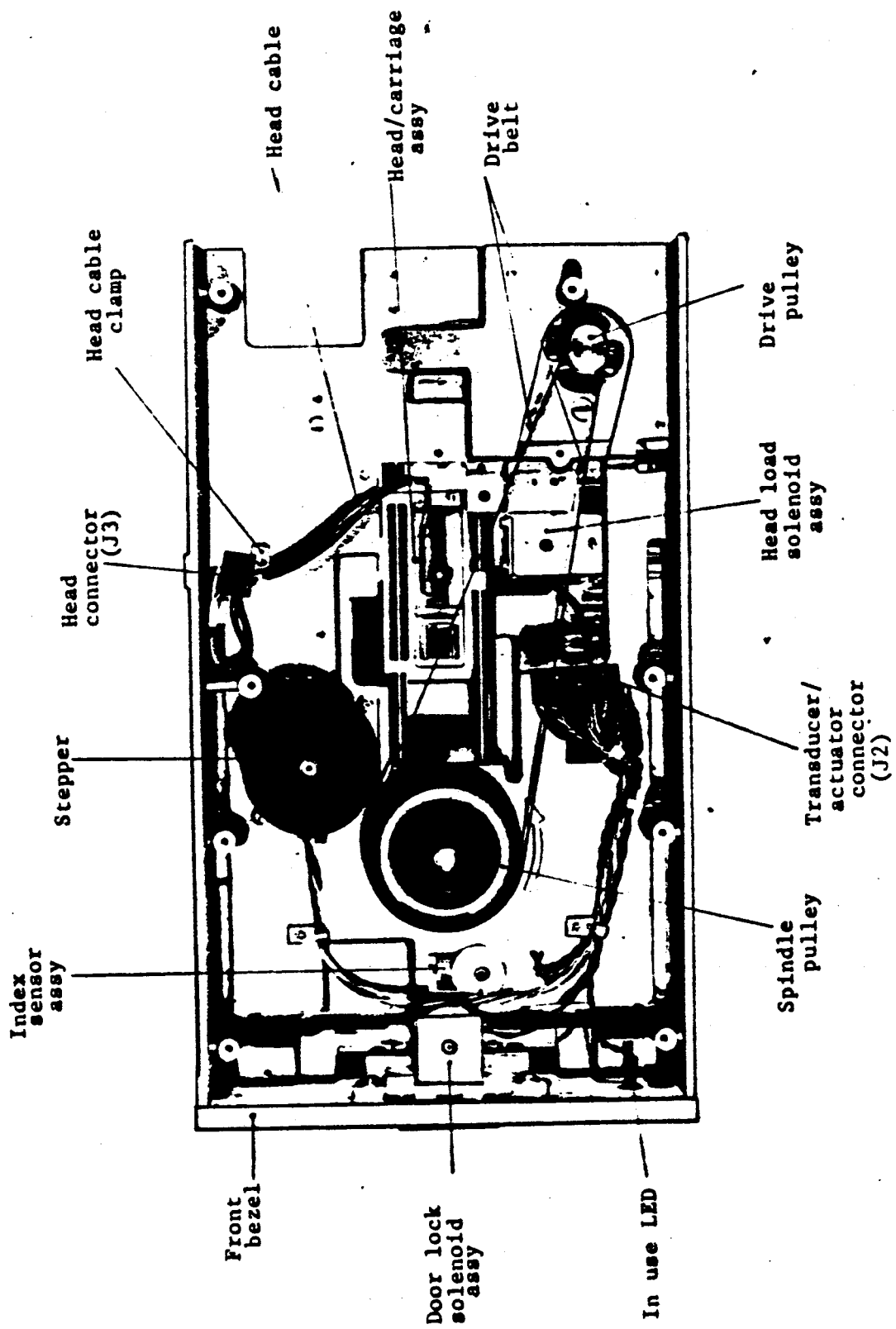


Fig. 4 Rear view of YD-174 with PWB removed

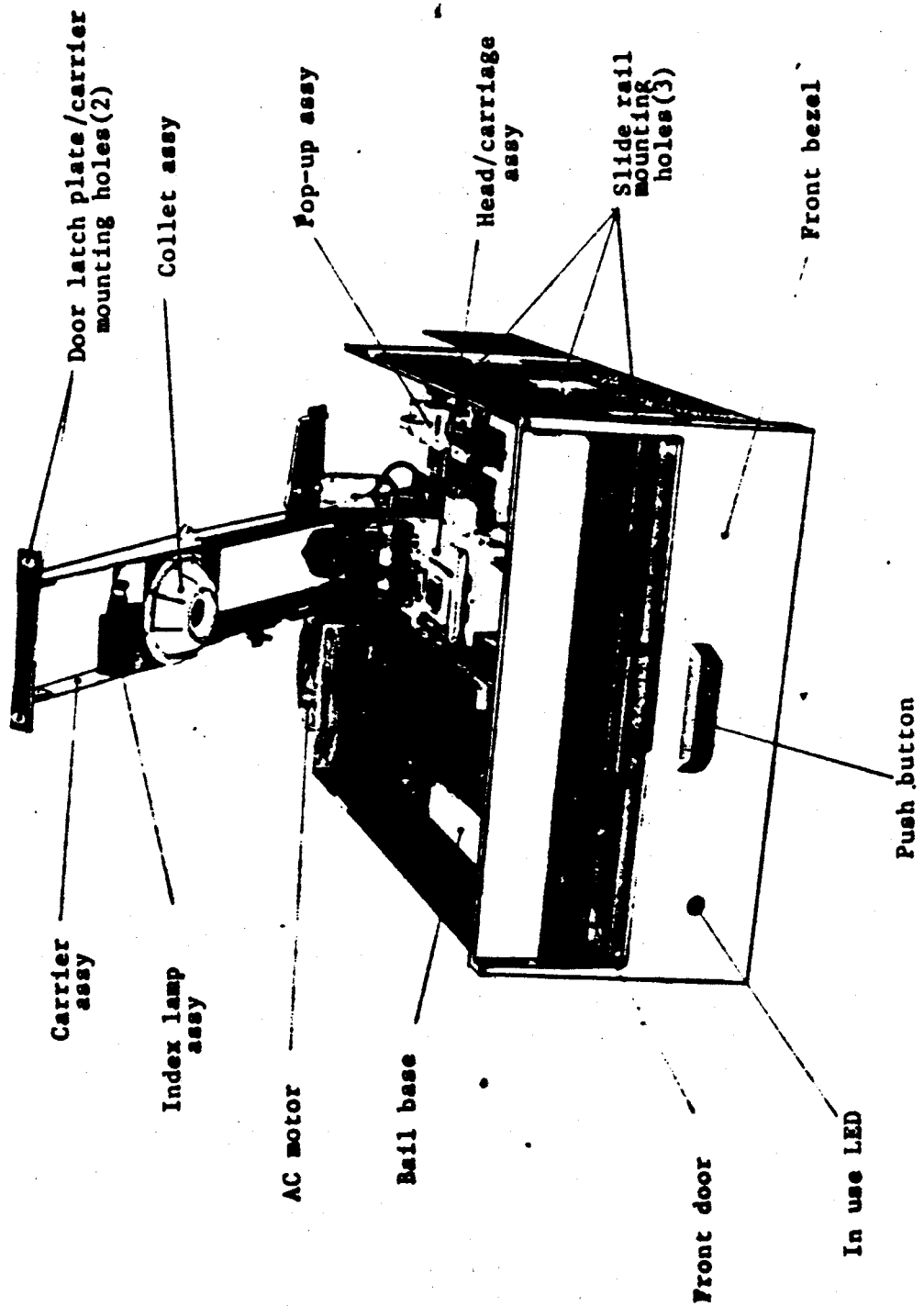


Fig. 5 Front view of YD-174 with carrier open

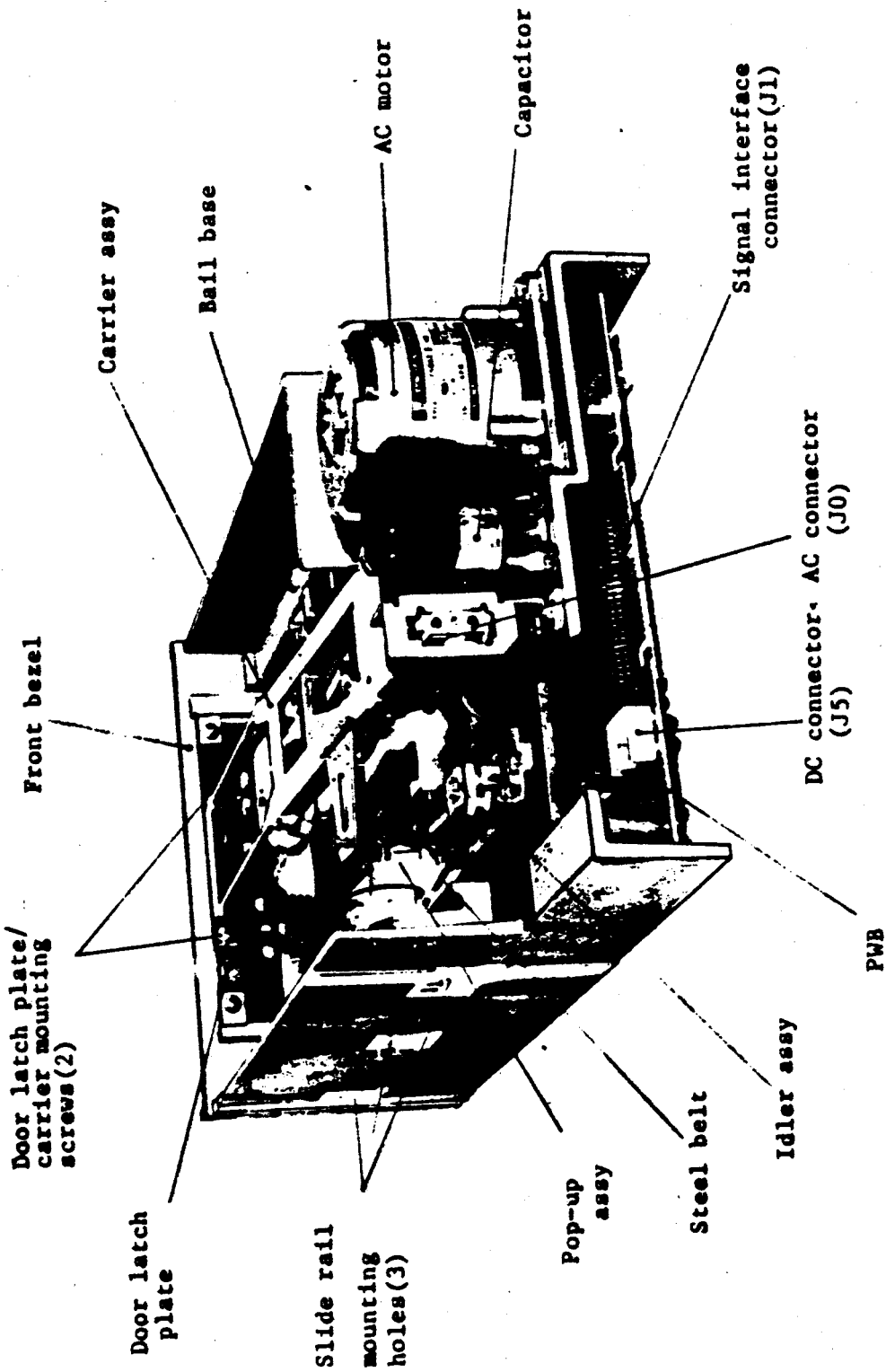
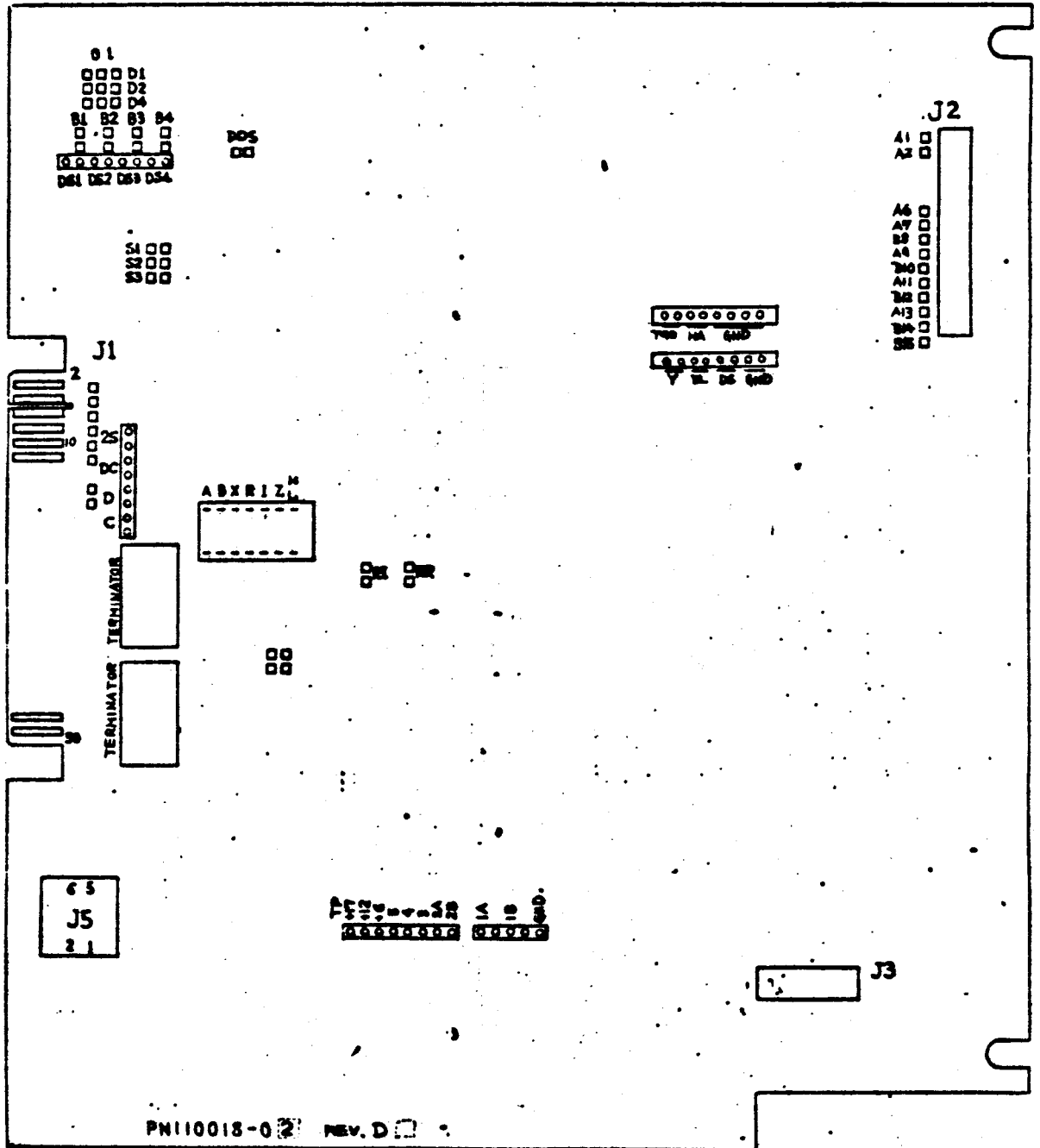


Fig. 6 Rear view of YD-174

8.0 TEST POINTS/CONNECTOR PIN ASSIGNMENTS



INTERFACE - J1

PIN NO	SIGNAL NAME
1	RETURN 1A
2	ALTERNATE 1A
3	RETURN 1B
4	ALTERNATE 1B
5	RETURN 2A
6	ALTERNATE 2A
7	RETURN 2B
8	ALTERNATE 2B
9	RETURN 3A
10	ALTERNATE 3A
11	RETURN 3B
12	ALTERNATE 3B
13	RETURN 4A
14	BIPE SELECT
15	RETURN 4B
16	ALTERNATE 4A
17	RETURN 4B
18	ALTERNATE 4B
19	RETURN 5A
20	INDEX
21	RETURN 5B
22	READY
23	RETURN 5C
24	LOW CURRENT
25	RETURN 5D
26	DRIVE SELECT 1
27	RETURN 5E
28	DRIVE SELECT 2
29	RETURN 5F
30	DRIVE SELECT 3
31	RETURN 6A
32	DRIVE SELECT 4
33	RETURN 6B
34	DIRECTION
35	RETURN 6C
36	STEP
37	RETURN 6D
38	WRITE DATA
39	RETURN 6E
40	WRITE GATE
41	RETURN 6F
42	TRACK 00
43	RETURN 7A
44	WRITE PROTECT
45	RETURN 7B

TRANSDUCERS - J2

PIN NO	SIGNAL NAME	COLOR
A15	IM USE LED RETURN	BLACK
B15	+IM USE LED	RED
A16	WP LED RETURN	BLUE
B16	+WP LED	ORANGE
A17	WP PTA RETURN	BLACK
B17	+WP PTA	RED
A18	TRK 00 LED RETURN	BLUE
B18	+TRK 00 LED	ORANGE
A19	TRK 01 PTA RETURN	BLACK
B19	+TRK 01 PTA	RED
A20		
B20		
A21		
B21		
A22	INDEX LED RETURN	BLACK
B22	+INDEX LED	RED
A23	INDEX PTA RETURN (DISK 1)	BLACK
B23	+INDEX PTA (DISK 1)	RED
A24	INDEX PTA RETURN (DISK 2)	BLUE
B24	+INDEX PTA (DISK 2)	ORANGE
A25	STEPPER 01	BLUE
B25	KEY	
A26	STEPPER 02	RED
B26	STEPPER 02	YELLOW
A27	STEPPER 04	GREEN
B27	STEPPER 04	WHITE
A28	- DOOR LOCK	BLACK
B28	DOOR LOCK 124VDC	RED
A29	- HEAD LOAD	BLACK
B29	HEAD LOAD 124VDC	RED

HEAD - J3

PIN NO.	SIGNAL NAME	COLOR
A7	W/R (HEAD B)	WHITE
B7	W/R (HEAD 1)	WHITE
A6	W/R RETURN (HEAD 0)	BLUE
B6	W/R RETURN (HEAD 1)	BLUE
A5	W/R (HEAD 0)	BLACK
B5	W/R (HEAD 1)	BLACK
A4	ERASE RETURN (HEAD 0)	RED
B4	ERASE RETURN (HEAD 1)	RED
A3	ERASE (HEAD B)	YELLOW
B3	ERASE (HEAD 1)	YELLOW
A2		
B2	KEY	
A1	SHIELD (HEAD 0)	
B1	SHIELD (HEAD 1)	

TEST POINTS

PIN NO	SIGNAL NAME
QND	GND
1B	FEAMP 1B
1A	FEAMP 1A
2B	FEAMP 2B
2A	FEAMP 2A
3	INDEX
4	ERASE
5	READ DATA
16	+6V DC
12	+12V DC
17	+17V DC

DC - J5

PIN NO	SIGNAL NAME
1	+34V DC
2	+24V RETURN
3	RESERVED
4	RESERVED
5	+5V DC
6	+5V GND

46	READ DATA
47	RETURN
48	RESERVED
49	RETURN
50	RESERVED

FIG. 8 PWB INTERFACE

9.0 RECOMMENDED SPARE PARTS LIST

MAINTENANCE LEVEL 1

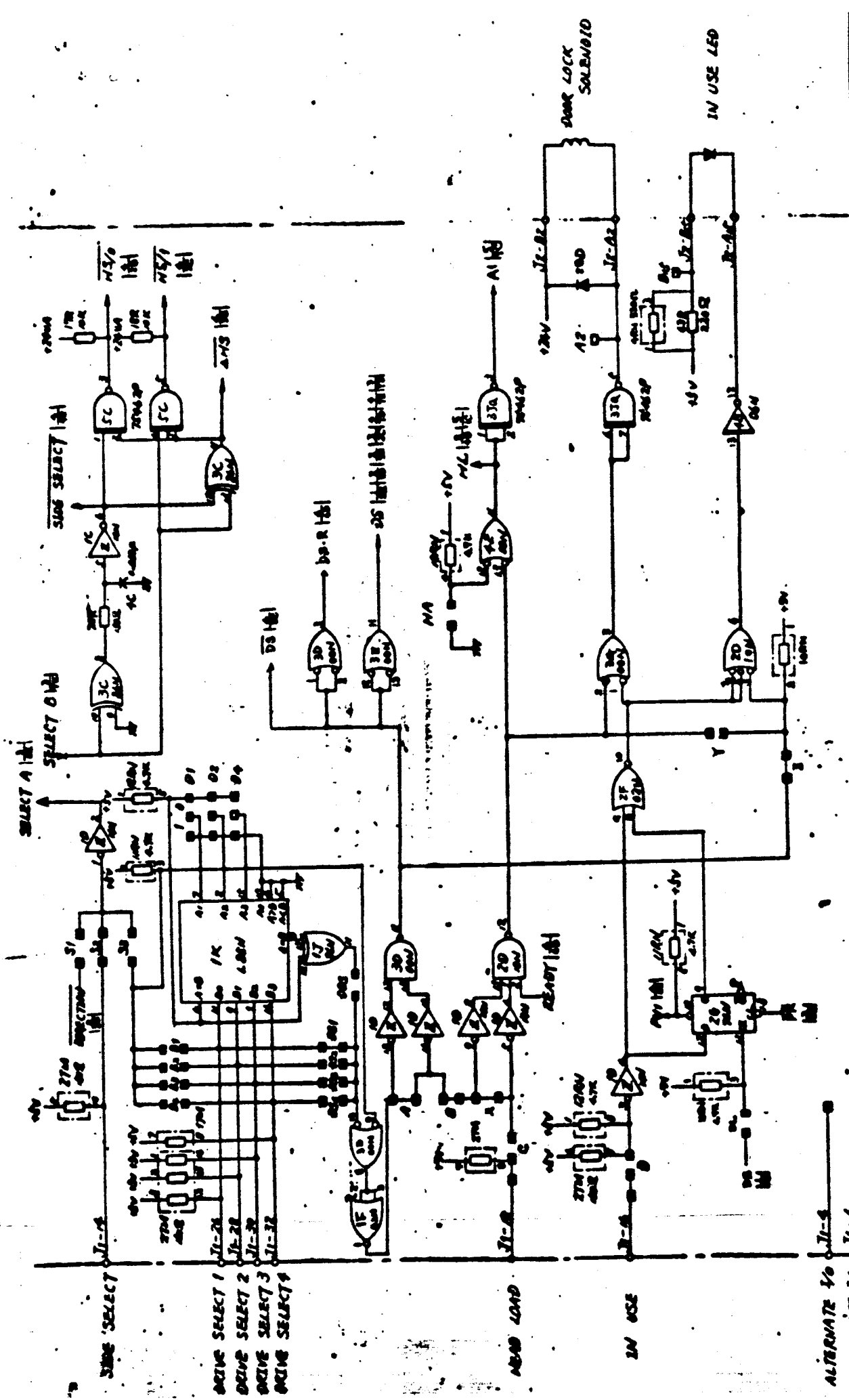
<u>PART NUMBER</u>	<u>PART DESCRIPTION</u>
110018-02	PWB
140099-01	Index Lamp Assy.
130052-01	Index Sensor Assy.
130044-01	Track 00 Sensor Assy.
130045-01	Write Protect Sensor Assy.
140025-01	In Use LED
140072-01	Drive Belt
140036-01	Drive Pulley (50 Hz)
140036-02	Drive Pulley (60 Hz)
140060-01	Wiper

MAINTENANCE LEVEL 2

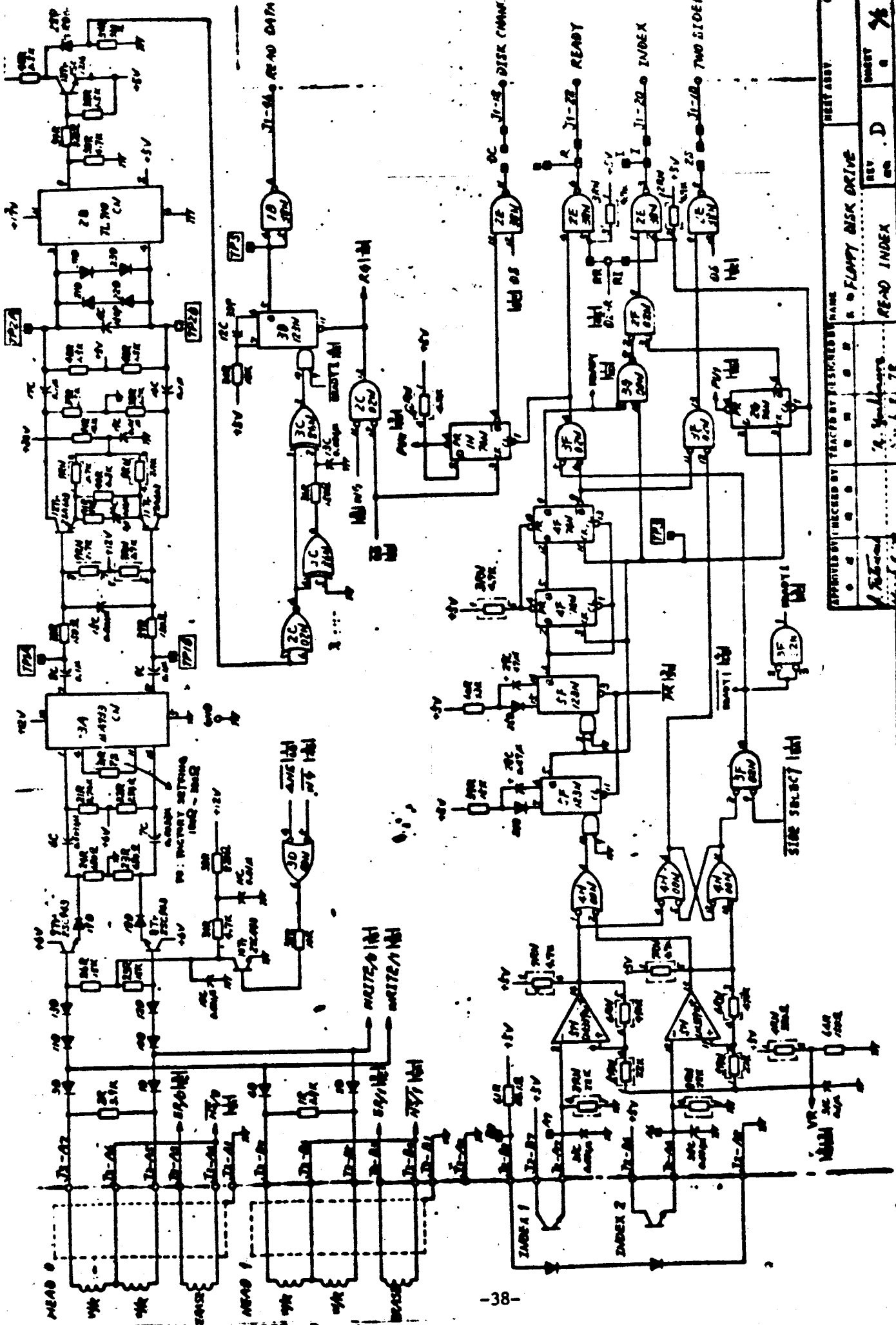
<u>PART NUMBER</u>	<u>PART DESCRIPTION</u>
140144-01	Drive Motor (115 V)
140144-03	Drive Motor (230 V)
120049-03	Carrier
130096-C1	Pop-up Assy.
140045-04	Head Load Solenoid Assy.
120027-03	Bail Assy.
140223-01	Door Lock Solenoid Assy.
120057-02	Head/Carriage Assy.
140250-01	Steel Belt
130053-01	Dust Seal Cover
130023-01	Idler Assy.
120155-01	Front Bezel (Cosmetic, YD174-1213, IVORY)
120155-02	Front Bezel (Oversize, YD174-1212, IVORY)
120155-03	Front Bezel (Functional, YD174-1214, IVORY)
028238-22	Spindle Bearing
140222-02	Bail return spring

10.0 TYPICAL SCHEMATIC DIAGRAMS

This section contains detailed schematic diagrams which describe the performance of the YD-174. Since there may be detailed differences between the logic appearing in this manual and that actually implemented in a given machine, these diagrams should not be used for faultfinding purposes. A set of diagrams for this purpose are shipped with each machine.



APPROVED BY	CHECKED BY	TRACED BY	DESIGNED BY	NAME	REV	NO	DATE
					D		
FLOPPY DISK DRIVE				SELECT HEAD LOAD			
MODEL				REV. NO.			
10-174-1213				1/5			
VE DATA							
-138112							



FDB-527007 Rev. D

REV. DATE		REVISED DESCRIPTION		PAGE		OF		SHEET NO.		OF		SHEETS	
APPROVED BY: <input type="checkbox"/> TRACKED BY: <input type="checkbox"/> DESIGNED BY: <input type="checkbox"/>													
MODEL: <input type="checkbox"/> FLOPPY DISK DRIVE													
STATE: <input type="checkbox"/> READ INDEX													
PART NO. <input type="checkbox"/>													
REV. <input type="checkbox"/> D													
SHEET <input type="checkbox"/> 1													
MODEL: <input type="checkbox"/> 10-174-1713													
STATE: <input type="checkbox"/>													
PART NO. <input type="checkbox"/>													
REV. <input type="checkbox"/>													
SHEET <input type="checkbox"/>													
OF <input type="checkbox"/>													
SHEETS <input type="checkbox"/>													

Y-E DATA

— 100112

11.0 Trouble shooting procedure

The trouble shooting procedures about the following error made are described in this section.

- (1) NOT READY
- (2) SEEK error
- (3) READ error
- (4) WRITE error

11.1 NOT READY

001

Check that the diskette is not visibly damaged or bound and is correctly inserted. Check that DRIVE SELECT pin (DS1 to DS4) and terminators on PWB are correctly inserted.

Is the spindle hub turning?

Y N

002

Is the drive motor turning?

Y N

003

. Measure AC line voltage at the motor connector.

Is measured voltage within limits?

Y N

004

Check the controller

005

. Check the motor connector and cables

. Remove drive belt

Does the motor start?

Y N

006

Remove binds if any .

If no binds, install a new drive motor (6.1)

007

Close the door

Is there a bind in the hub assembly?

Y N

008

. Install a new belt

. If trouble still exists, install a new drive motor (6.1)

009

Open the door

Is there still a bind in the hub assembly?

Y N

010

Replace carrier assembly (6.2) or collect assembly

011

Remove bind or replace the spindle assembly

001 002

012

Are any pulleys loose?

Y N

013

Go to NOT READY Step 003

014

Tighten loose pulleys (5.8)

015

Measure DRIVE SELECT 1 to 4 input on PWB.

NOTE: SIDE SELECT input should be inactive when Diskette 1 is inserted otherwise READY output is inactive.

Is proper DRIVE SELECT input in active?

Y N

016

Check the controller

017

Measure the following DC power voltages at the connector on PWB

+5v : 4.75 to 5.25v, +24v: 22.6 to 26.4v

Are the voltages within limits?

Y N

018

Check the controller

019

Perform Index sensor assembly service check (5.3.1)

Are the output voltages within limits?

Y N

020

Replace the Index sensor assembly.

021

Perform Index lamp assembly service check (5.2.1)

Are the output voltages within limits?

Y N

022

Replace the Index lamp assembly

023

021

023

If an oscilloscope is available check the diskette speed. Look for index pulses every 166.7 ± 3.3 ms at the following two test points on FWB

Test point J2-A7 with Diskette 1 inserted.

Test point J2-A6 with Diskette 2 or Diskette 2D inserted.

Is the Diskette rotational speed within limits?

Y N

024

Check carrier, door and bail assembly for defects that are visibly observed.

Do these parts appear to be correct?

Y N

025

Replace as required: carrier (6.2.3), door (6.6), bail (6.4)

026

Go to NOT READY Step 012

027

Replace FwB

1.2 SEEK ERROR

001

Check that the diskette is not visibly damaged or bound and is correctly inserted.

Check that DRIVE SELECT pin (DS1 to DS4) and Terminators on PWB are correctly installed.

Check the carriage guide bars and the steel belt for damage or dirt.

Check that the guide bar clamps and the steel belt is not loose.

Turn off power and manually move head carriage to approximately track 76.

Turn on power and issue "seek to track 00" command.

Does the head carriage go to track 00?

Y N

002

Measure DRIVE SELECT 1 to 4 input on PWB (J1-26 to J1-32)

NOTE: SIDE SELECT input should be inactive when Diskette 1 is inserted. Otherwise READY output is inactive.

Is proper DRIVE SELECT input in active?

Y N

003

Check the controller

004

Measure the following DC power voltages at the connector on PWB
+5V (J5-5); 4.75 to 5.25V; +24V (J5-1); 22.6 to 26.4V

Are the voltage within limits?

Y N

005

Check the controller

006

Is READY input active?

Y N

007

Go to NOT READY Step 001

017 008

001 006

008

Perform track 00 sensor assembly service check (5.4.1)

Is track 00 sensor assembly good?

Y N

009

Replace track 00 sensor assembly (5.4.2.)

010

Is direction input (J1-34) inactive (high)?

Y N

011

Check the controller

012

Is the period of STEP input (J1-36) larger than 3 ms?

Y N

013

Check the controller

014

Replace the PWB

Is start up good?

Y N

015

Return original PWB

GO TO SEEK ERROR Step 029

017 016

Verify fix

001

017

Issue the "seek to track 76" command,

Does the head carriage go to track 76?

Y N

018

Is Direction input (J1-34) active (low)?

Y N

019

Check the controller

020

Replace PWB

Is start up good?

Y N

021

Return original PWB

GO TO SEEK ERROR Step 029

022

Verify fix

023

Do head carriage position service check (6.8.2)

Is the adjustment correct?

Y N

024

Readjust the carriage positioning (6.8.2)

025

Perform the random seek test

Are there seek error?

Y N

026

Verify fix

027

Replace PWB

Are there still seek error?

Y N

028

Verify fix

029

027

029

Return original FWB.

Remove the steel belt clamping screws on the carriage, manually move the head carriage.

Are there any binds in head carriage and guide bars?

Y N

030

Remove steel belt

Is there any bind in idler assembly?

Y N

031

Replace the stepper assembly (6.10)

032

Replace the idler assembly (6.11)

033

Replace the head carriage assembly (6.8.3)

..3 READ ERROR

001

Check that the diskette is not visibly damaged or bound and is correctly inserted.

Check that the DRIVE SELECT pin (DS1 to 4) and terminators on PWB are correctly installed.

Issue the Read command.

Measure DRIVE SELECT 1 to 4 input (J1-26-J1-32) on PWB.

Is proper DRIVE SELECT input in active?

Y N

002

Check the controller

003

Measure the following DC power voltages at the connector on PWB

+5v (J5-5); 4.75 to 5.25v, +24v (J5-1): 22.6 to 26.4v

Are the voltage within limits?

Y N

004

Check the controller

005

Is the head loaded?

Y N

006

Is Ready output active?

Y N

007

GO TO NOT READY Step 001

008

Replace PWB (5.1)

Is the head loaded?

Y N

009

Return original PWB

Replace head load solenoid assembly (6.5.2)

011 010

Verify fix

005

011

Does Read Error occur at the same sector of the same track?

N Y

012

Remove the diskette and insert another known-to-be-good diskette.
Verify fix

013

Measure the head preamplifier differential output voltage at the test points between Tp 1A and Tp 1B on FWB

Is the measured voltage greater than 50 mVpp?

Y N

014

Replace FWB (5.1)

Is the measured voltage greater than 50 mVpp?

Y N

015

Return original FWB (5.1)

Replace head carriage assembly (6.8.3)

016

GO TO READ ERROR Step 017

017

Measure the Index positioning timing by using CE disk.

Is the Index timing within limits?

Y N

018

Perform Index sensor assembly service check (5.3.1)

Are the output voltages within limits?

Y N

019

Replace the Index sensor assembly (5.3.2)

025

020

017

018

020

Perform Index lamp assembly service check (5.2.1.)

Are the output voltages within limits?

Y N

021

Replace the Index lamp assembly. (5.2.2)

022

Perform the read test

Are there read error?

Y N

023

Verify fix

024

Replace the head carriage assembly (6.8.3)

025

Measure the track positioning by using CE disk.

Is the track positioning within limits?

Y N

026

Adjust the track positioning (6.8.2)

027

If an osillo-scope (or counter) is available, check the diskette speed.
Look for index pulses every $166.7 \pm 3.3 \mu s$ at the following two test points
on PWB.

Test point J1 - A7 with Diskette 1 inserted

Test point J1 - A6 with Diskette 2 or Diskette 2D inserted

Is the Diskette rotational speed within limits?

Y N

031

028

027 Q27

028

Is power frequency of drive motor, correct?

Y N

029

Correct power frequency of drive motor

030

GO TO NOT READY Step 024

031

. Replace FWB (5.1)

Are there still read error?

Y N

032

Verify fix

033

Return original FWB

Replace the head carriage assembly (6.8.3)

L.4 WRITE ERROR

001

Check that the diskette is not visibly damaged or bound and is correctly inserted.

Check that the DRIVE SELECT pin (DS1 to 4) and terminators on PWB are correctly installed.

Issue the Write command.

Measure DRIVE SELECT 1 to 4 input (J1-26 - J1-32) on PWB.

Is proper DRIVE SELECT input in active?

Y N

002

Check the controller

003

Measure the following DC power voltages at the connector on PWB

+5v (J5-5) 4.75 to 5.25v

=24v (J5-1) 22.6 to 26.4v

Are the voltage within limits?

Y N

004

Check the controller

005

Check the diskette

Does there write protect notch exist on diskette?

N Y

006

Change diskette to another one without write protect notch and
GO TO WRITE ERROR Step 007

007

Is the head loaded?

Y N

008

GO TO READ ERROR Step 006

009

Check the WRITE PROTECT SENSOR ASSEMBLY (5.5.1)

Y N

010

Replace the WRITE PROTECT SENSOR ASSEMBLY

011

009

011

Does Write Error occur at the same sector of the same track?

N Y

012

Remove the diskette and insert another known to be a good diskette.
Verify fix

013

Perform the Read Only test with diskette written another good drive

Are there Read error?

Y N

031

Verify fix

032

Replace FWB (5.1)

Are there still Write error?

Y N

032

Verify fix

033

Return original FWB .

Replace head carriage.

(6.8.3)

RETURN LETTER

Title: THE TWO-SIDED FLOPPY DISK DRIVE YD-174 RCSL No.: 44-RT1991
Maintenance Manual

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Abstract: This manual is produced by Y-E DATA INC. JAPAN and it may be distributed according to an agreement between Y-E DATA INC. and RC Computer. RC Computer uses the technical numbers FDD709 and FDD710 for the floppy disk drive.

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TWO-SIDED 5.25 INCH FLOPPY DISK DRIVE

YD-274

MAINTENANCE MANUAL

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YD-274 MAINTENANCE MANUAL

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1 GENERAL

This manual contains the instructions required to maintain the two-sided 5.25 inch floppy disk drive YD-274. This manual provides detailed information for maintenance check, parts replacement, and adjustment to aid the customers engineer.

2 MAINTENANCE TOOLS AND TEST EQUIPMENT

The tables below list the maintenance tools, maintenance supplies, test equipment, and exerciser for the YD-274.

2.1 MAINTENANCE TOOLS LIST

Tools	YE DATA Part Number
Screwdriver, Phillips (M3)	141034-01
Screwdriver, Slot	141035-01
Cutter	141039-01
Long-nose pliers	141040-01
Tweezers	141042-01
Screwdriver, torque* (with hex wrench, 1.5)	141036-01
Tr00 stopper adjustment gauge*	141037-02
Spindle pulley - motor pulley center adjustment gauge	141038-01
CE disk	141082-01

* to be used at maintenance level 2

YD-274 Tool kit (including the tools listed above except CE disk)	P/N 141041-01
--	---------------

2.2 MAINTENANCE SUPPLIES

Supplies	YE DATA Part Number
Cable clamp	031005-01
Cleaning kit Applicator Gauze Head cleaning fluid (Isopropyl alcohol) Lubricant (Idemitsu oil "Apollo first oil")	141046-01

2.3 TEST EQUIPMENT

Test equipment
Circuit tester
Electronic counter
Oscilloscope*

* to be used at maintenance level 2

2.4 EXERCISER

Equipment	YE DATA Part Number
Exerciser	YD-264

3 PREVENTIVE MAINTENANCE

3.1 GENERAL

Under normal circumstances preventive maintenance every two years is required on the YD-274. This contains visual check and cleaning. If severely dirty environments are encountered, the time between maintenance checks should be shortened accordingly.

3.2 VISUAL CHECK

Visual inspection is the first step in any maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items may save downtime later.

3.3 CLEANING

Cleaning of the YD-274 should be done carefully. Lightly clean dirt with a gauze or applicator moistened with isopropyl alcohol.

CAUTION: The carriage assembly is a factory-adjusted and tested assembly. Do not try to adjust or repair this internal component.

Preventive maintenance items

Parts	Observe	Procedure
Main frame Head Connector Sensor and others	Dirt on head, connector, sensor, etc.	Clean
	Loose screws	Tighten screws
Drive belt	Dirt	Clean
	Frayed or weakened area	Change new belt

4 CHECK, REPLACEMENT & ADJUSTMENT

This chapter contains the detailed maintenance procedure on the assemblies (level 1 & level 2) listed below.

Level 1: Neither special training nor special tools are required.

Level 2: Some training and special tools are required.

Level 1

- 4.1 BELT
- 4.2 PWB
- 4.3 INDEX LAMP ASSEMBLY
- 4.4 MEDIA GUIDE L ASSEMBLY (WITH WRITE PROTECT SENSOR & LAMP)
- 4.5 IN USE LED ASSEMBLY
- 4.6 DRIVE MOTOR ASSEMBLY (WITH MOTOR CONTROL PWB)

Level 2

- 4.7 INDEX SENSOR ASSEMBLY
- 4.8 TROO SWITCH ASSEMBLY
- 4.9 TROO STOPPER
- 4.10 HEAD LOAD SOLENOID ASSEMBLY
- 4.11 CARRIER ASSEMBLY
- 4.12 FRONT DOOR ASSEMBLY
- 4.13 FRONT BEZEL ASSEMBLY
- 4.14 STEPPER
- 4.15 CARRIAGE ASSEMBLY

NOTE: Refer to Chapter 5 PARTS/ASSEMBLIES LOCATIONS and Chapter 6 TEST POINTS/CONNECTOR PIN ASSIGNMENTS.

4.1 BELT (Physical Locations 2 in Chapter 5)

4.1.1 SERVICE CHECK

1. Check dust and dirt on the belt. Check frayed, scratched or weakened area on the surface of belt.

4.1.2 REMOVAL AND REPLACEMENT

1. Remove the belt at the spindle pulley while rotating the pulley slowly by your fingers.
2. Replace a new belt at the motor pulley first and then at the spindle pulley while rotating the pulley.

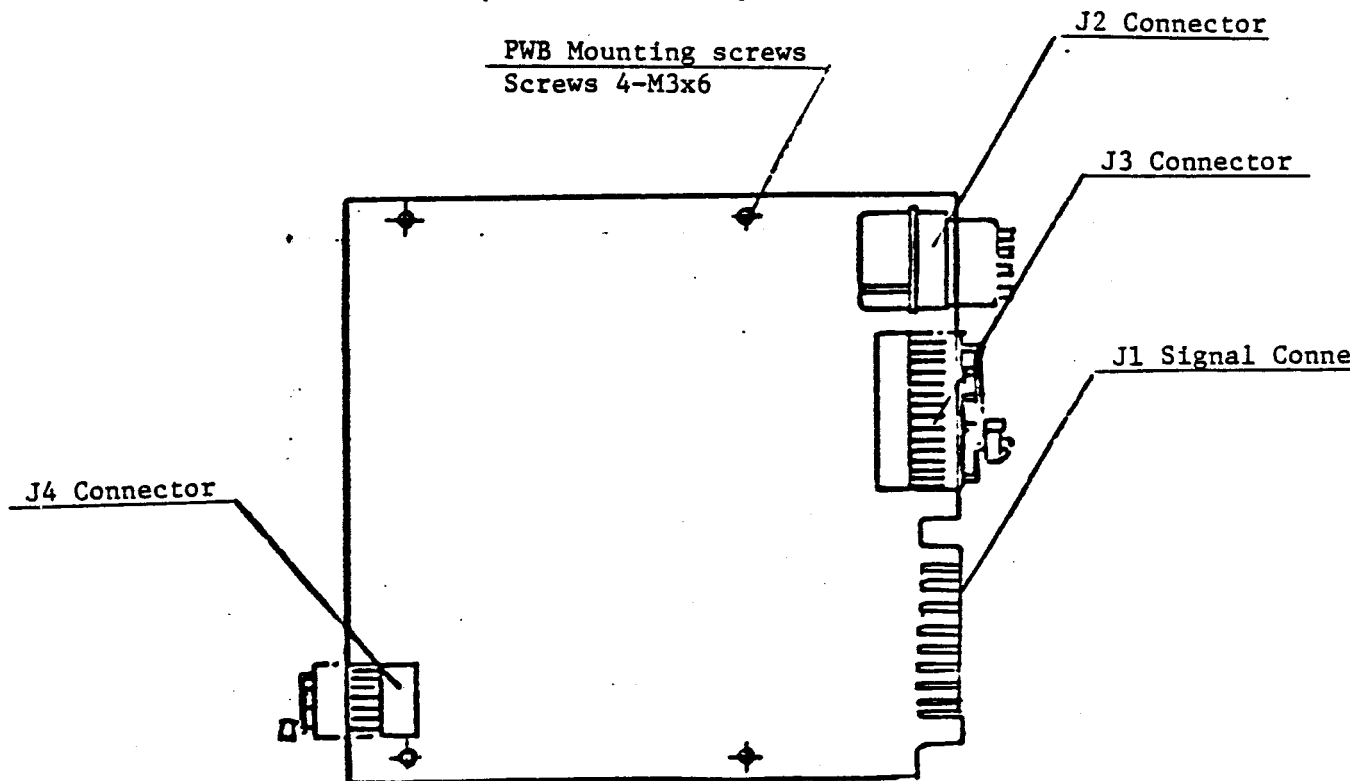
CAUTION: Do not scratch the belt by the flange of motor pulley when removal and replacement.

NOTE: The new belt has no side.

4.2 PWB (Physical Locations 1 in Chapter 5)

4.2.1 PWB REMOVAL AND REPLACEMENT

1. Disconnect four connectors (J1, J2, J3, J4) from PWB.
2. Remove mounting screws.
3. Remove PWB.
4. Reverse the procedure for replacement.



4.3 INDEX LAMP ASSEMBLY (Physical Locations 3 in Chapter 5)

4.3.1 SERVICE CHECK

1. Turn on power.
2. Verify voltage of 1.0 to 1.7 V between "J3-B11" and "G" (GND) on PWB.

4.3.2 REMOVAL AND REPLACEMENT

1. Remove PWB. (See 4.2)
2. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

3. Remove two lamp leads from J3 connector by pushing down on tabs with tweezers. (BLACK to J3-A11, RED to J3-B11)

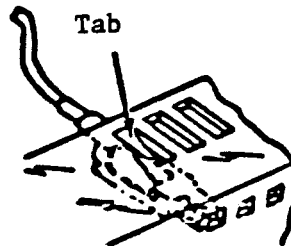


Fig. 4.3.1

4. Cut the index lamp cable clamp.
5. Open the front door.

6. Remove lamp leads from guidance groove on carrier and index lamp assembly with fingers and tweezers.

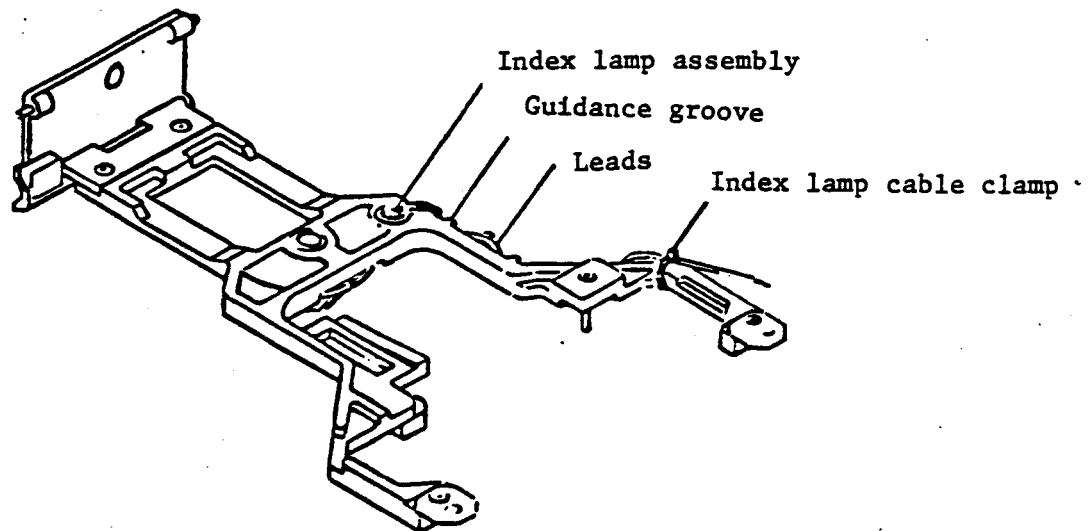


Fig. 4.3.2

7. Reverse the procedure for replacement.

NOTE: When installing the assembly, insert the LED after the LED holder.

8. Service check. (See 4.3.1)

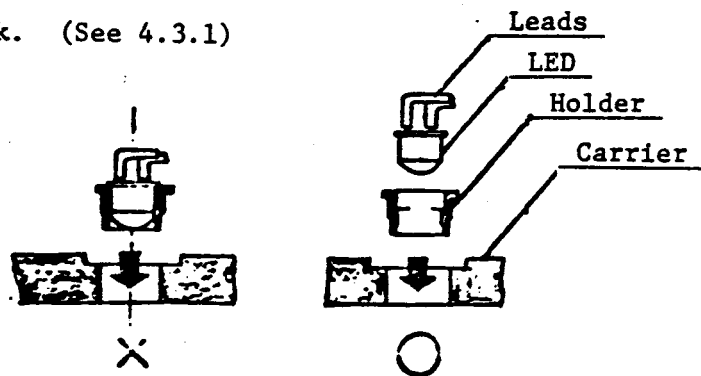


Fig. 4.3.3

4.4 MEDIA GUIDE L ASSEMBLY (WITH WRITE PROTECT SENSOR & LAMP) (Physical Locations 3 in Chapter 5)

4.4.1 SERVICE CHECK

1. Turn on power.
2. Verify the followings without a diskette.
 - a) Write protect lamp
Voltage of 1.0 to 1.7 V between "J3-B13" and "G"(GND) on PWB.
 - b) Write protect sensor
Voltage of 0 to 0.5 V between "J3-B14" and "G"(GND) on PWB.
3. Insert a write-protect diskette (a diskette with a write-protect seal on the write-protect notch), close the door and verify the following.
 - a) Write protect sensor
Voltage of 2.5 to 5.25 V between "J3-B14" and "G"(GND) on PWB.

4.4.2 REMOVAL AND REPLACEMENT

1. Remove PWB. (See 4.2)
2. Open the front door.
3. Remove four leads of write protect assembly from J3 connector by pushing down on tabs with tweezers.
(BLACK to J3-A13, YELLOW to J3-B13, BLACK to J3-A14, ORANGE to J3 B14)

NOTE: Remove leads with the lead clamp and lead stopper slightly open. (See physical locations 3 in chapter 5.)

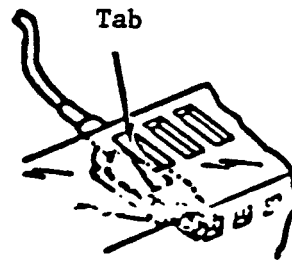


Fig. 4.4.1

- Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

- Remove the media guide L assembly mounting screws and the media guide L assembly.
- Reverse the procedure for replacement.

NOTE: When installing the media guide L assembly, push it against the main frame stop.

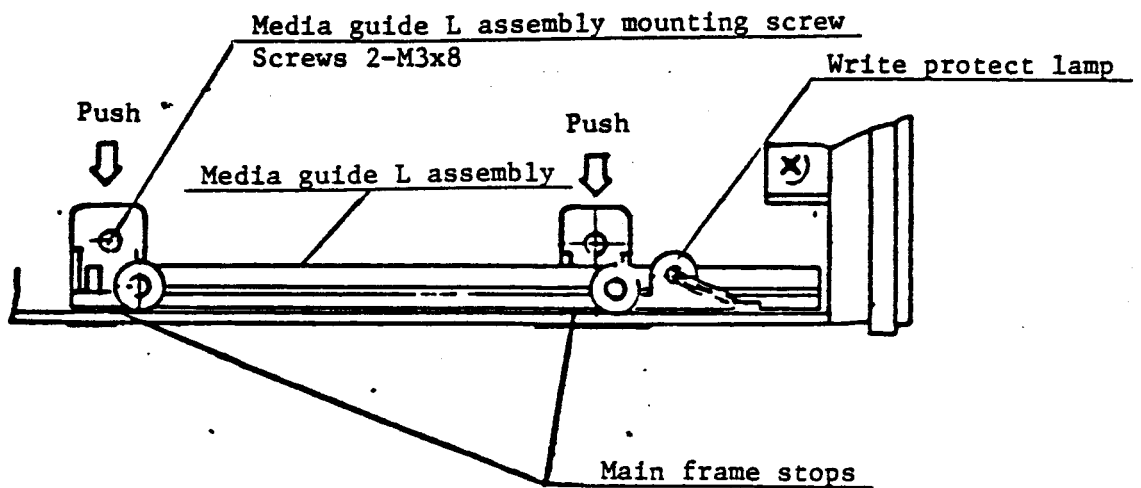


Fig. 4.4.2

- Service check. (See 4.4.1.)

4.5 IN USE LED (Physical Locations 5 in Chapter 5)

4.5.1 SERVICE CHECK

1. Turn on power.
2. Set the DRIVE SELECT 0 on the interface "LOW level" and insert a short plug onto the short pin DS0.
3. Check the LED lamp lighted.

NOTE: The voltage between "J3-B10" and "G"(GND) reads 1 to 2 V when LED on.

4.5.2 REMOVAL AND REPLACEMENT

1. Remove PWB. (See 4.2.)
2. Open the front door.
3. Remove two leads of in use LED from J3 connector by pushing down on tabs with tweezers. (BLACK to J3-A10, RED to J3-B10)

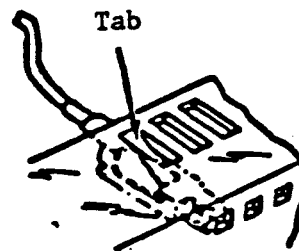


Fig. 4.5.1

4. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

5. Remove the front bezel.

6. Remove the holder 2 by tweezers in the direction shown below. Take the LED holder out in front.
7. Take the LED out of LED holder.
8. Reverse the procedure for replacement.
9. Service check. (See 4.5.1.)

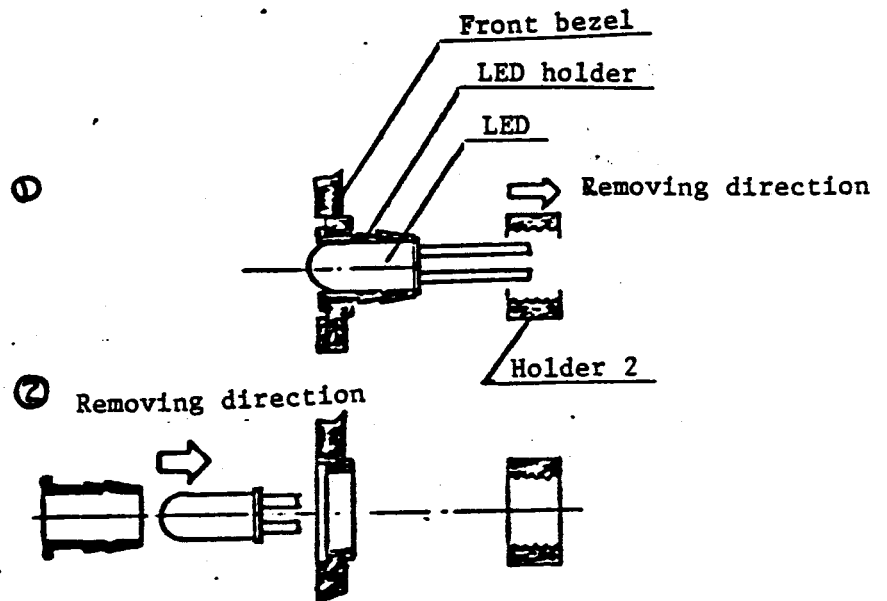


Fig. 4.5.2

4.6 DRIVE MOTOR ASSEMBLY (Physical Locations 2 & 3 in Chapter 5)

4.6.1 SERVICE CHECK

1. Turn on power.
2. Rotate the motor with the interface signal MOTOR ON "LOW level".
3. Insert a diskette and close the door.
4. Load the head.
5. Check the dark lines on the spindle pulley appear motionless. For 50 HZ fluorescent lighting use the inside ring of lines for 60 HZ observe the outside ring.

NOTE: When the dark lines appear to move one line a second, rotating speed error is
1% at 50 HZ
or 0.8% at 60 HZ.

When using a frequency counter, check the index pulse period (TP3 on PWB) for reading of 197 to 203 m sec.

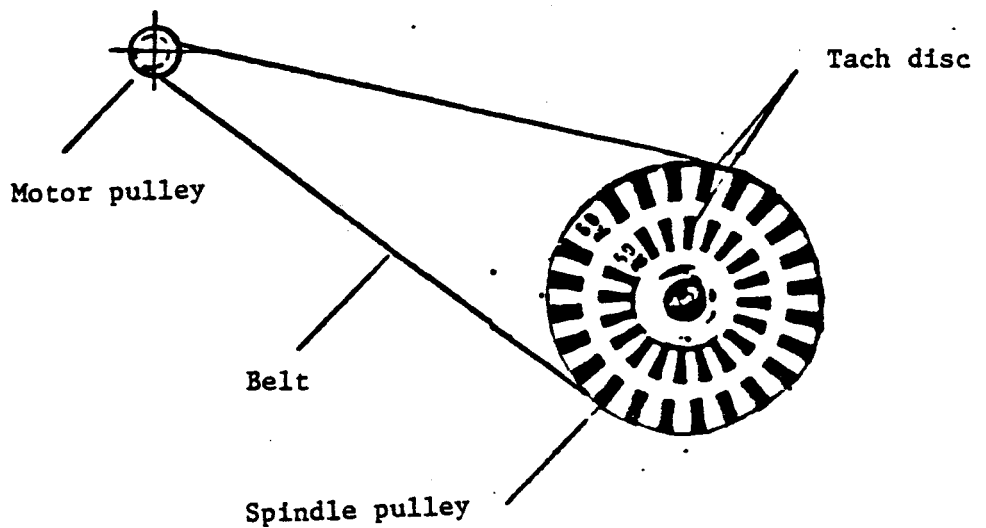


Fig. 4.6.1

4.6.2 REMOVAL AND REPLACEMENT

1. Remove the belt. (See 4.1.)
2. Cut the J3 cable clamp and motor cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

3. Remove three leads from J3 connector by pushing down on tabs with tweezers. (BLUE to J3-A1, RED to J3-B1, BLACK to J3-B2)

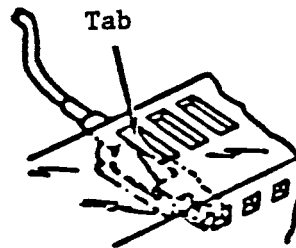


Fig. 4.6.2

4. Remove the motor control PWB mounting screws.

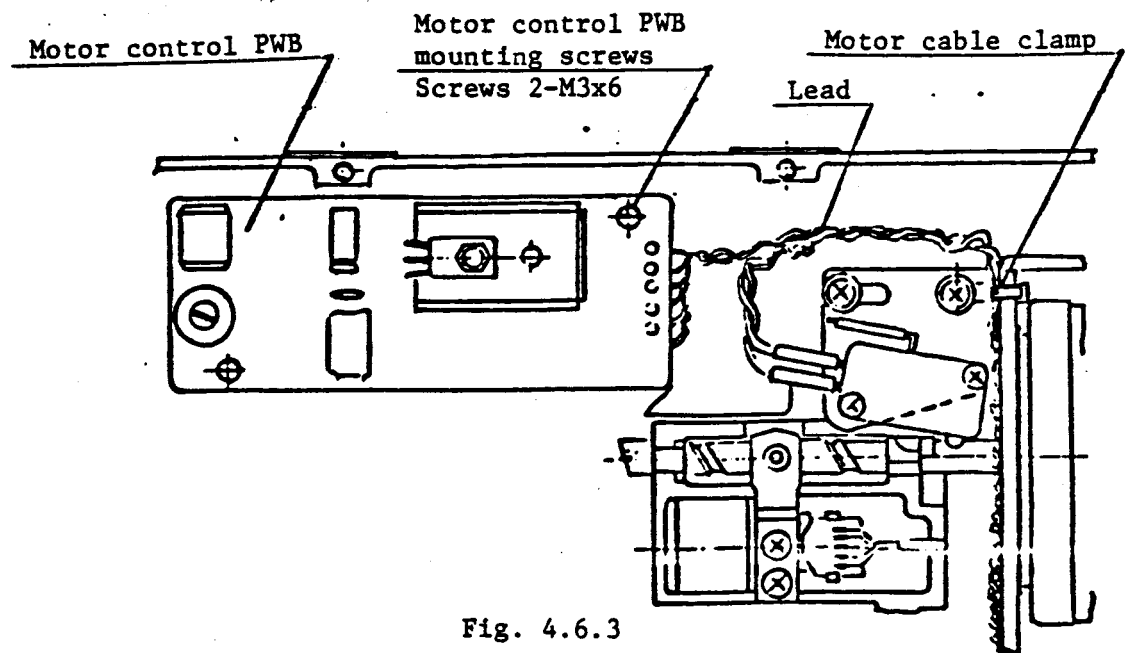


Fig. 4.6.3

5. Remove the drive motor and motor control PWB from the main frame by removing the drive motor mounting screws.
6. Reverse the procedure for replacement.

NOTE: Replace the drive motor by applying the spindle pulley - motor pulley center adjustment gauge (P/N 141038-01).

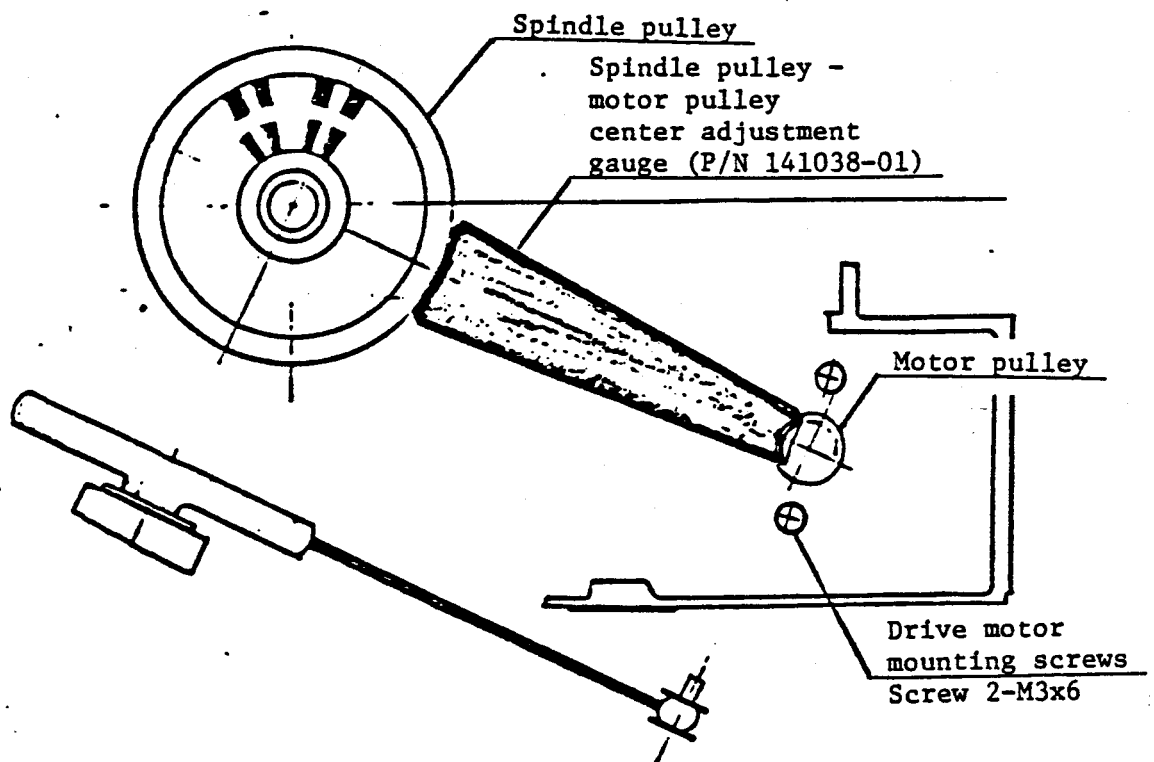


Fig. 4.6.4

7. Service check. (See 4.6.1.)

4.6.3 ADJUSTMENT

1. After service check in 4.6.1, turn the pot located on the motor control PWB with a slot screwdriver until the dark lines on the spindle pulley appear completely motionless.

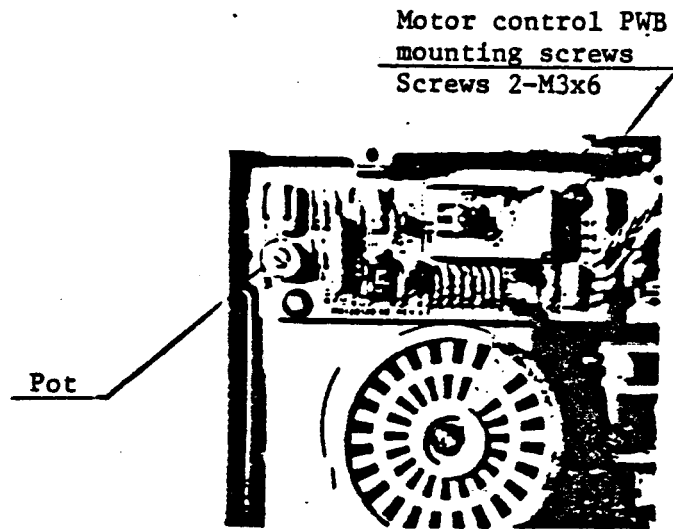


Fig. 4.6.5

NOTE: When using a frequency counter, check the index pulse period (TP3 on PWB) for reading of 197 to 203 m sec.

4.7 INDEX SENSOR ASSEMBLY (Physical Locations 4 in Chapter 5)

4.7.1 SERVICE CHECK

1. Turn on power.
2. Verify the voltage of 0 to 0.5 V when door closed without a diskette and 2.5 V to 5.25 V when a diskette inserted backward and door closed, between "J3-B12" and "G"(GND) test points on PWB.
3. Do 4.7.3 adjustment when service check of index timing needed.

4.7.2 REMOVAL AND REPLACEMENT

1. Remove the PWB. (See 4.2.)
2. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

3. Remove two leads of index sensor assembly from J3 connector by pushing down on tabs with tweezers. (BLACK to J3-A12, BLUE to J3-B12)

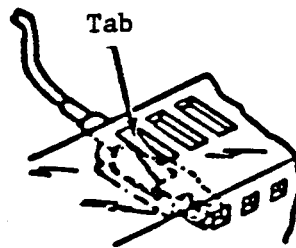


Fig. 4.7.1

NOTE: Remove leads with the lead clamp slightly open.

4. Open the front door.
5. Remove the index sensor assembly by removing its mounting screws.

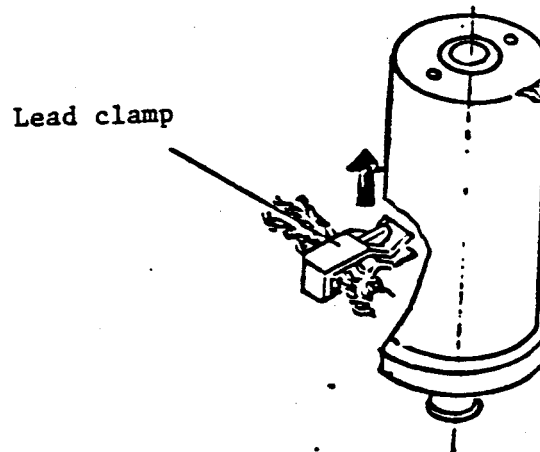


Fig. 4.7.2

6. Reverse the procedure for replacement.
7. Do 4.7.3 service check for replacement.

4.7.3 ADJUSTMENT (INDEX SENSOR)

1. Loosen the mounting screws of the sensor by 1/4 turn.
2. Turn power on.
3. Connect test points "TP1A", "TB1B" and "TP3" with an oscilloscope, one probe (CH1) to "TP1A", another (CH2) to "TB1B" and external trigger to "TP3".
Set the oscilloscope as follows.

INPUT COUPLING MODE	AC
VERT MODE	ADD
INVERT	ON
TIME/DIV	0.1 msec
VOLTS/DIV (CH1, CH2)	100 mV

4. Insert a CE disk and close the door.
5. (Adjustment) After loading the head and moving the carriage to TR01, observe the timing between the leading edge of index signal (TP3) and the burst signal (TP1A, TP1B) of read output (SIDE 0). This should be 300 to 500 μ sec.

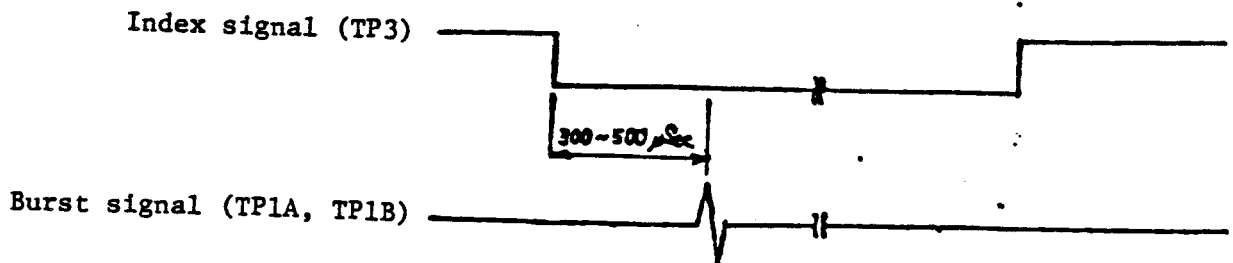


Fig. 4.7.3

To adjust this, move the index sensor with a phillips screwdriver as shown in fig. 4.7.4.

6. (Service check). Verify the burst signal for 0 to 800 μ sec on SIDE 0 and 1 of track 01 and 34. If the time is not within tolerance, continue on with the adjustment in the above 5 and 6.

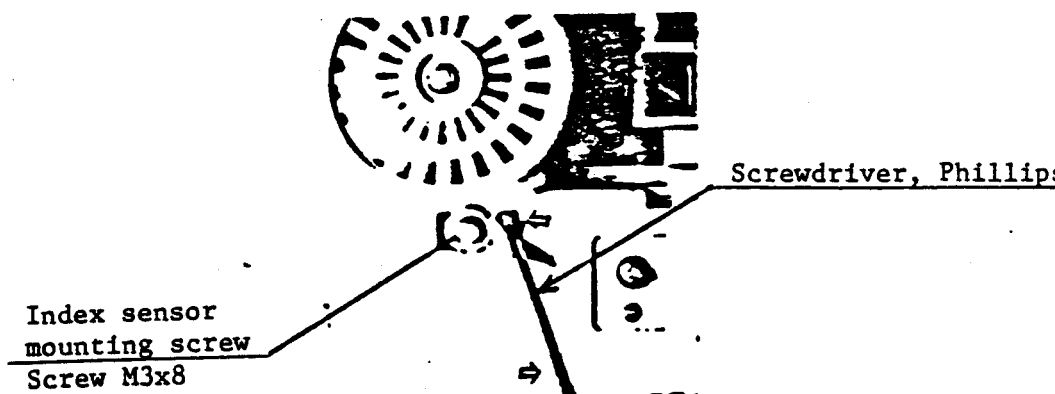


Fig. 4.7.4

NOTE: Movement of index sensor assembly in the direction shown in fig. 4.7.4 delays the start of burst signal from the leading edge of index signal.

4.8 TROO SWITCH ASSEMBLY (Physical Locations 2 in Chapter 5)

4.8.1 SERVICE CHECK (1): TROO SWITCH (MICROSWITCH) CHECK

1. Turn on power.
2. Push down on the button of TROO switch (microswitch) with a finger.
3. Verify the voltages between "J3-A8" (NC) and "G" (GND) and between "J3-A9" (NO) and "G" (GND) on PWB for 3 to 5.25 V and 0 to 0.1 V respectively.
4. Release the finger from pressing the button.
5. Verify the voltages between "J3-A8" (NC) and "G" (GND) and between "J3-A9" (NO) and "G" (GND) on PWB for 0 to 0.1 V and 3 to 5.25 V respectively.

SERVICE CHECK (2): TROO SWITCH POSITION CHECK

1. Turn on power.
2. Move the carriage until the track 00 signal goes low (0 to 0.4 V) by feeding pulses to STEP signal with the DIRECTION signal high.
3. Verify the carriage to hit the TROO stopper by one step outward from track 00.
4. Verify the carriage to return inward (TROO) and the TROO signal (J1-26) to go low (0 to 0.4 V) by another step pulse to move outward.
5. Verify the TROO signal to go high (2.4 to 5.25 V) by stepping the carriage by one to position at track 01 and to remain high (2.4 to 5.25 V) by stepping one more to position at track 02.
6. If service checks 3, 4 & 5 are not good, adjust the TROO switch assembly (See 4.8.3.).

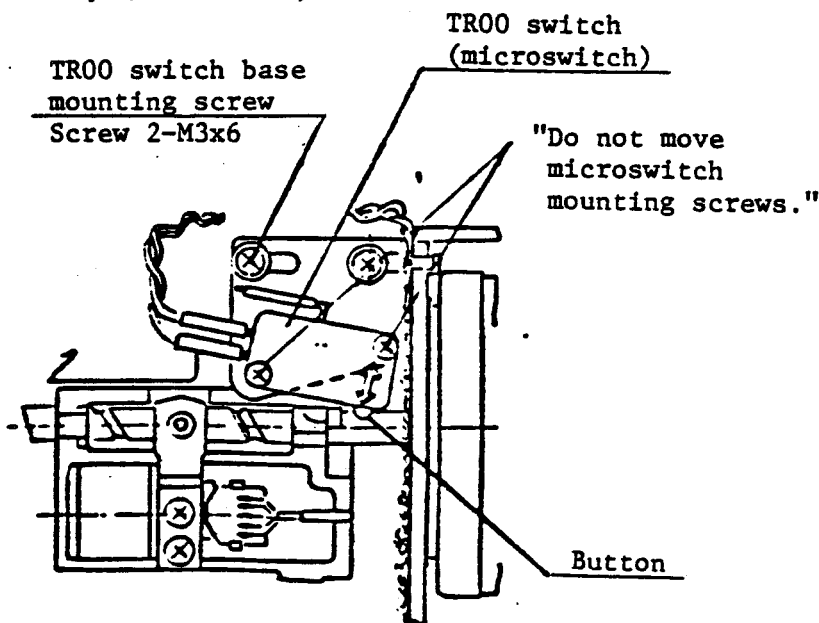


Fig. 4.8.1

4.8.2 REMOVAL AND REPLACEMENT

1. Remove J3 connector from PWB.
2. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

3. Remove three leads of TR00 switch from J3 connector by pushing down on tabs with tweezers. (YELLOW to J3-A8, GREEN to J3-A9, WHITE to J3-B9)

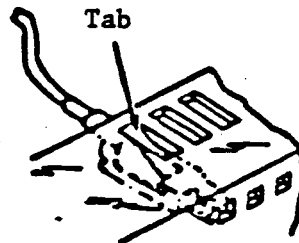


Fig. 4.8.2

4. Remove the TR00 switch assembly by removing TR00 switch base mounting screws.

CAUTION: Do not remove microswitch mounting screws.
(See fig. 4.8.1.)

5. Reverse the procedure for replacement.
6. Adjustment (See 4.8.3.)

4.8.3 ADJUSTMENT

CAUTION: Adjust the carriage positioning before this if there is carriage positioning error.
(See 4.15.3.)

1. Loosen two mounting screws of TROO switch base and move the TROO switch assembly innermost.
2. Turn on power.
3. Connect "TP1A", "TP1B" and "TP3" on PWB with an oscilloscope, one probe (CH1) to "TP1A", the other (CH2) to "TP1B" and the external trigger to "TP3".
Set the oscilloscope as follows.

INPUT COUPLING MODE	AC
VERT MODE	ADD
INVERT	ON
TIME/DIV	20 msec
VOLTS/DIV (CH1, CH2)	50 mV

4. Insert a CE disk and close the door.
5. Move the carriage inward by 10 steps.
6. Load the head and move the carriage outward until TROO read output of CE disk appears.
7. Verify the voltages between "J3-A8"(NC) and "G"(GND) and between "J3-A9"(NO) and "G"(GND) on PWB for 3 to 5.25 V and 0 to 0.1 V respectively when the TROO switch is activated while moving slowly the TROO switch assembly inward.
8. Move the carriage inward by one step (TRO1) and verify the voltages between "J3-A8"(NC) and "G"(GND) and between "J3-A9"(NO) and "G"(GND) on PWB for 0 to 0.1 V and 3 to 5.25 V respectively.
9. Check the switch on at track 00 and off at track 01.
If not, repeat 7 to 9.
10. Make the TROO stopper service check (4.9.1).

4.9 TROO STOPPER (See figures 4.9.1 and 4.9.2.)

CAUTION: When there is error in carriage positioning and TROO switch actuating position, adjust them before this.

4.9.1 SERVICE CHECK

1. Turn on power.
2. Move the carriage until the TROO signal goes low (0 to 0.4 V) by feeding pulses to the STEP signal with the DIRECTION signal high.
3. Verify the carriage to hit the TROO stopper by one step outward from track 00.
4. Verify the carriage to return inward (TROO) and the TROO signal (J1-26) to go low (0 to 0.4 V) by another step outward.

4.9.2 ADJUSTMENT

1. Turn on power.
2. Move the carriage to track 00.
3. Move the drive motor leads so the TROO stopper adjustment gauge can go into.
4. Push the TROO stopper adjustment gauge (P/N 141037-01) in while slightly loosening the TROO stopper mounting screw.
5. Tighten the TROO stopper mounting screw by the torque screwdriver (P/N 141036-01) set at 4 kg-cm.
6. Service check. (See 4.9.1.)

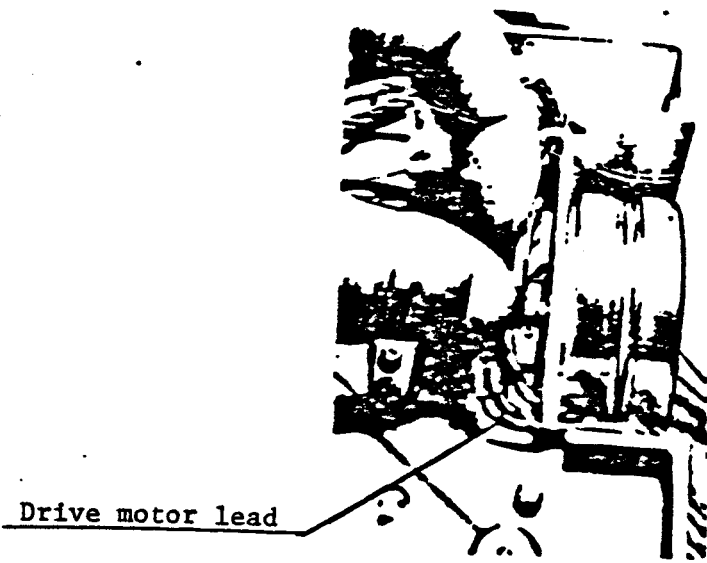


Fig. 4.9.1

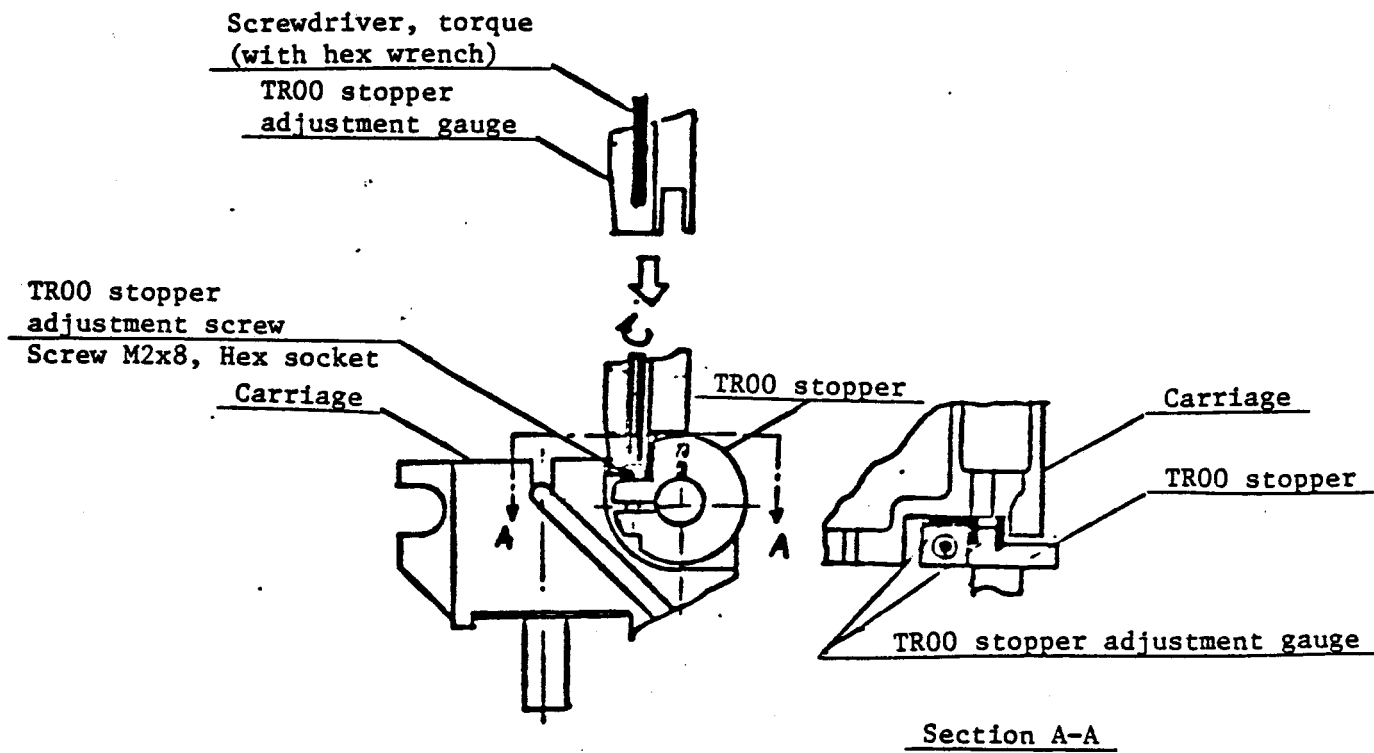


Fig. 4.9.2

4.10 HEAD LOAD SOLENOID

4.10.1 SERVICE CHECK

1. Check the pad under the bail for any damage through the opening for diskette in the front bezel.
2. Turn on power.
3. Insert a diskette and close the door.
4. Load the head.
5. Verify there is a gap between the bail and the carriage arm tab throughout carriage travel.
6. Turn off power.
7. Remove the diskette and close the door.
8. Look for a clearance of 0.3 to 0.7 mm between head surfaces. Visually check this clearance through the diskette opening in the front bezel. Perform adjustment in 4.10.3 if necessary.

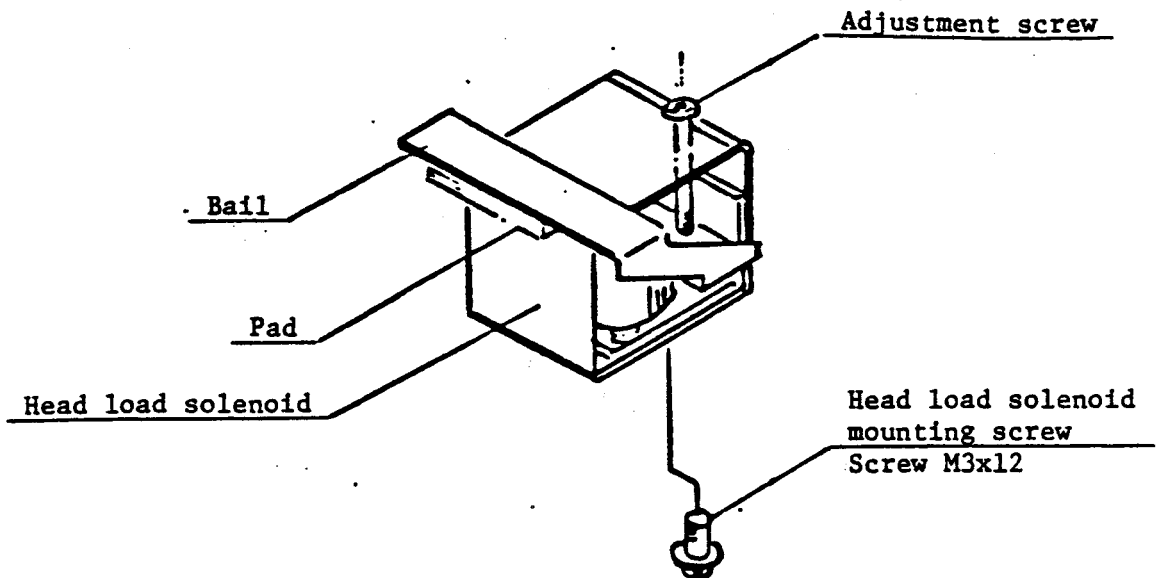


Fig. 4.10.1

4.10.2 REMOVAL AND REPLACEMENT

1. Remove the PWB. (See 4.2.)
2. Remove the carrier by removing the carrier assembly

NOTE: Keep carrier leads as they are.

3. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

4. Remove two leads of head load solenoid from J3 connector by pushing down on tabs with tweezers. (GREEN to J3-A4, WHITE to J3-B4)

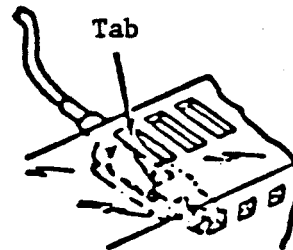


Fig. 4.10.2

5. Remove the media guide L assembly by removing its mounting screw.

NOTE: Do not remove leads of media guide L assembly.

6. Insert a piece of clean paper between the head surfaces.
7. Remove head load solenoid mounting screws on the back side of frame and slightly lift the carriage arm tab by a finger. Remove the head load solenoid while turning it as shown in fig. 4.10.3.
8. Reverse the above procedure for replacement.

CAUTION: Ensure that the bail is under the carriage arm tab.

9. Perform adjustment. (See 4.10.3.)

4.10.3 ADJUSTMENT

1. Adjust the gap between heads for 0.3 to 0.7 mm by turning the adjustment screw on the carrier. A clockwise turning of adjustment screw decreases the gap between heads and a counterclockwise turning increases it.
2. Do service check. (See 4.10.1.)

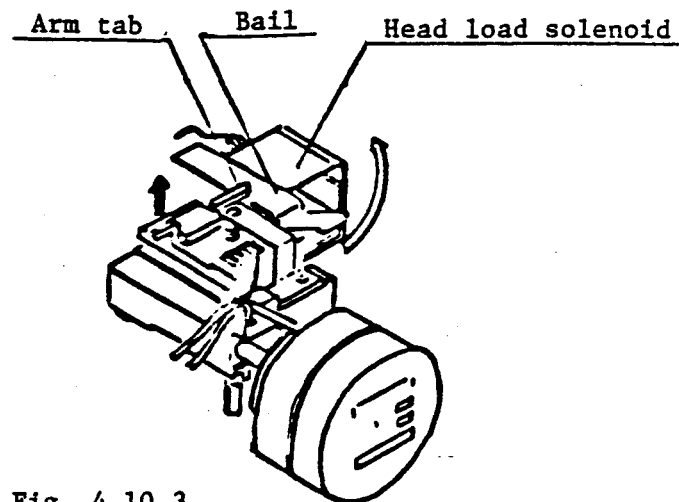


Fig. 4.10.3

4.11 CARRIER ASSEMBLY (Physical Locations 3 in Chapter 5)

4.11.1 REMOVAL AND REPLACEMENT

1. Remove the PWB. (See 4.2.)
2. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

3. Remove two leads of index lamp from J3 connector by pushing down on tabs with tweezers. (BLACK to J3-A11, WHITE to J3-B11)

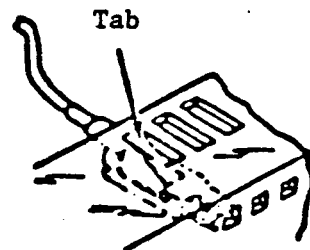


Fig. 4.11.1

4. Remove the head cable while slightly opening its clamp.
5. Remove the carrier assembly by removing its mounting screw.

CAUTION: Remove the carrier gently to avoid stress against head arm tab.

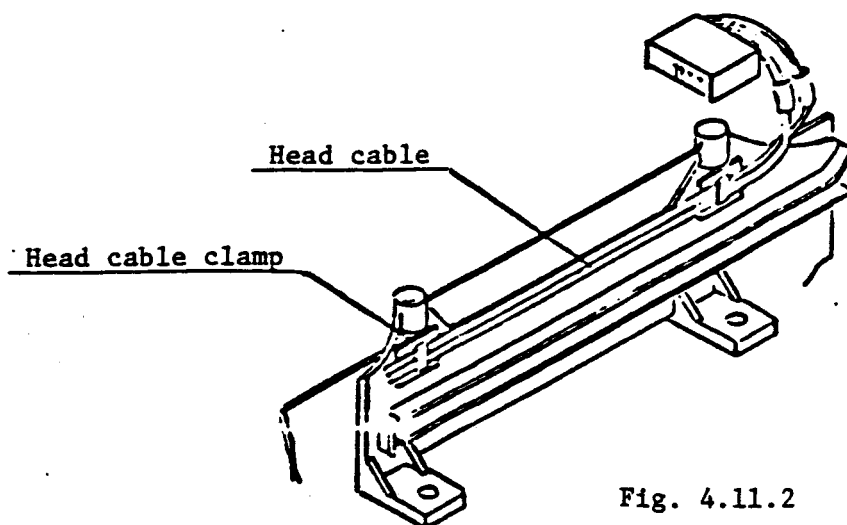


Fig. 4.11.2

6. When replacing, put front door pins into front bezel guide grooves.
7. Mount the carrier temporarily by carrier mounting screws.
8. Close the door, position and fix the carrier so that the gap between front bezel and front door be uniform.

CAUTION: Be sure the carrier is under the head arm tab.

9. Insert leads while lifting the tab of J3 connector.
10. Dress the J3 cable clamp.
11. Adjust the bail of head load solenoid. (See 4.10.3.)

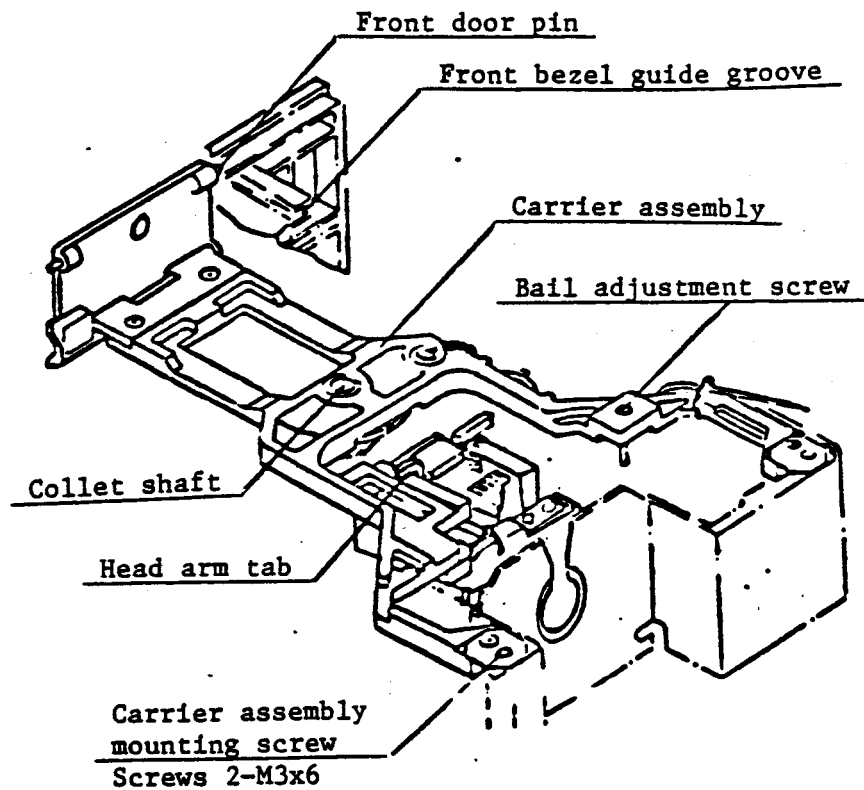


Fig. 4.11.3

4.12 FRONT DOOR ASSEMBLY

4.12.1 REMOVAL AND REPLACEMENT

1. Remove the PWB. (See 4.2.)
2. Close the door.
3. Remove front door mounting screws while holding down on the carrier upside with fingers and pull out the front door assembly toward the backside of door.

CAUTION: Do not lift the carrier by a finger to avoid stress against the head arm.

4. For replacement put the front door assembly into the front bezel guide grooves from the back- and upside of front bezel while holding down on the carrier upside with fingers.
5. Remount front door assembly mounting screws.
6. Remount the PWB. (See 4.2.)

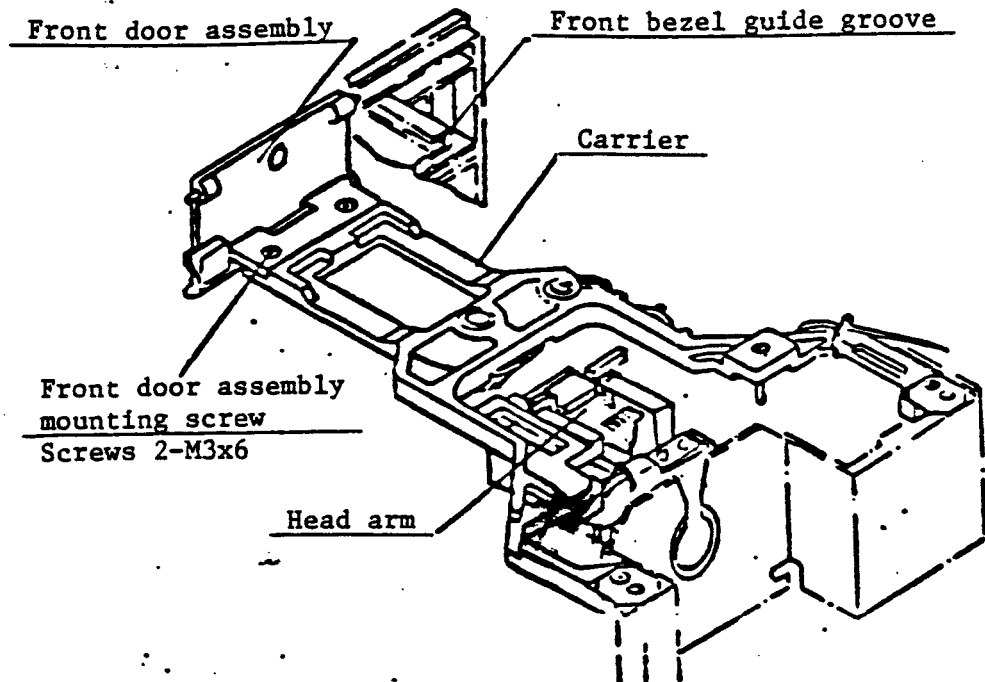


Fig. 4.12.1

4.13 FRONT BEZEL ASSEMBLY (Physical Locations 4 in Chapter 5)

4.13.1 REMOVAL AND REPLACEMENT

1. Remove the PWB. Reference section 4.2.
2. Open the front door.
3. Remove two leads of in use LED from J3 connector by pushing down on tabs with tweezers. (BLACK to J3-A10, RED to J3-B10)

NOTE: Remove leads with the lead clamp and lead stopper slightly open.

4. Remove the front bezel mounting screws and pull out the front bezel assembly in front.
5. Reverse the above procedure for replacement.

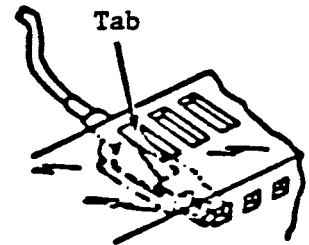


Fig. 4.13.1

NOTE: When installing the front bezel assembly, push it against the main frame and the main frame stopper.

CAUTION: Do not lift the carrier by fingers to avoid stress against the head arm.

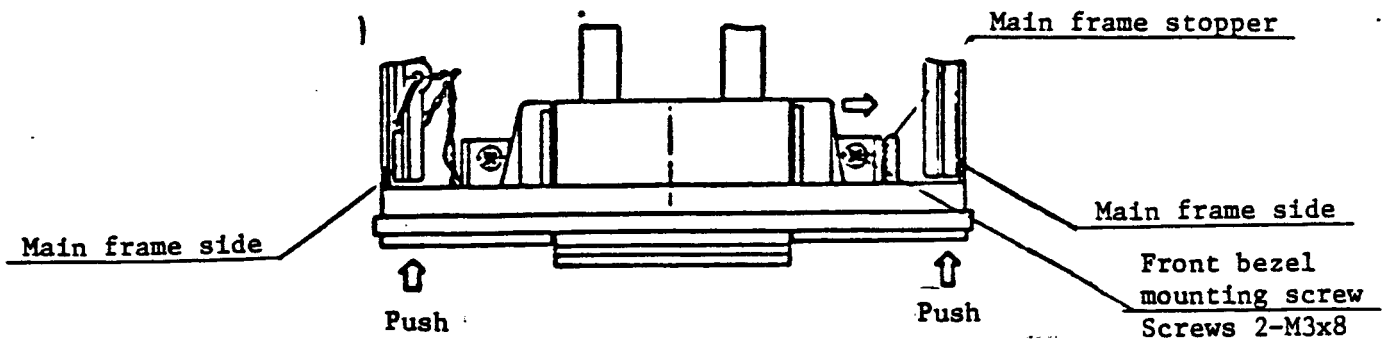


Fig. 4.13.1

4.14 STEPPER (Physical Locations 3 in Chapter 5)

4.14.1 SERVICE CHECK

1. Turn on power.
2. Verify carriage seek to be correct by applying DIRECTION and STEP signals.

4.14.2 REMOVAL AND REPLACEMENT

1. Remove the PWB. Reference section 4.2.
2. Bring the carriage assembly as close to the frame as possible by turning the TROO stopper.
3. Remove the head cable of carriage assembly with the head cable clamp of door guide R slightly open.
4. Cut the J3 cable clamp.

CAUTION: Avoid damage to the lead covering when cutting the cable clamp.

5. Remove six leads of stepper from J3 connector by pushing down on tabs with tweezers.
(BLACK to J3-A5, YELLOW to J3-A6, BROWN to J3-A7, RED to J3-B5, RED to J3-B6, ORANGE to J3-B7)

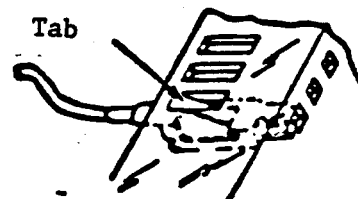


Fig. 4.14.1

6. Remove the ball spring set (retainer, filter, leaf spring and ball) by removing leaf spring mounting screws.
- CAUTION: Do not lose the ball.
7. Loosen the stepper mounting screws until the stepper turns easily.
 8. Pull out the stepper while turning it and holding the carriage assembly by hand.
 9. Remove TROO stopper from stepper shaft by loosening the hex socket setscrew of TROO stopper.
 10. Reverse the above procedure for replacement.

CAUTION: Give a few drops of lubricant (Apollo first oil) to the groove and surface of stepper shaft and the felt.

11. Adjust carriage assembly positioning. (Reference section 4.15.3.)
12. Adjust TROO stopper.

4.14.3 ADJUSTMENT

1. Adjust carriage assembly positioning. (Reference section 4.15.3.)

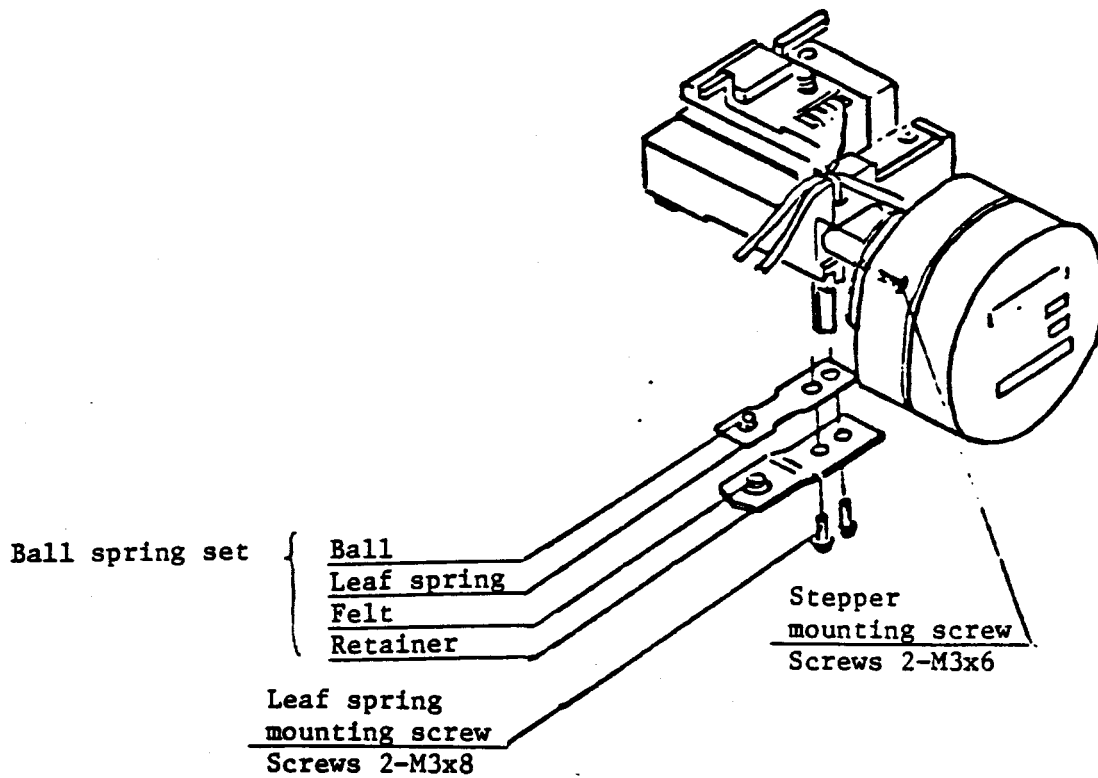


Fig. 4.14.2

4.15 CARRIAGE ASSEMBLY (Physical Locations 4 in Chapter 5)

CAUTION: The carriage assembly is factory-adjusted and tested. Do not, for any reason, try to disassemble or adjust this internal component.

4.15.1 POSITIONING SERVICE CHECK

1. Turn on power.
2. Connect oscilloscope to "TP1A", "TP1B" and "TP3", one probe (CH1) to "TP1A", the other (CH2) to "TP1B" and the external trigger to "TP3".
Set the oscilloscope as follows.

INPUT COUPLING MODE	AC
VERT MODE	ADD
INVERT	ON
TIME/DIV	20 msec
VOLTS/DIV (CH1, CH2)	50 mV

3. Insert a CE disk and close the door.
4. Load the head and step outward until TR00 signal (J1-9) goes low (0 to 0.4 V).
5. Step the carriage from track 00 to track 16 and observe read output on oscilloscope as shown in figure 4.15.1.

When B is larger than A,

$$A/B > 0.6$$

When A is larger than B,

$$B/A > 0.6$$

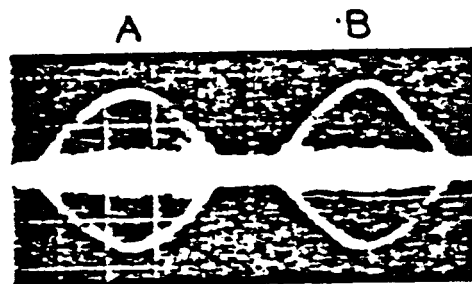


Fig. 4.15.1

6. Step the carriage from track 34 to 16 and verify read output is as in step 6.

4.15.2 REMOVAL AND REPLACEMENT

1. Remove the PWB. (Reference section 4.2.)
2. Remove the carrier assembly. (Reference section 4.11.)
3. Remove the stepper. (Reference section 4.14.)
4. Pull out the carriage assembly.
5. Reverse the above procedure for replacement.

CAUTION: Give a few drops of lubricant to the stepper shaft and move the carriage throughout travel one or two times.

Lubricant: Apollo first oil

4.15.3 POSITIONING

1. Adjust the clearance between head surfaces for 0.3 to 0.7 mm. (Reference section 4.10.3.)
2. Connect oscilloscope to "TP1A", "TP1B" and "TP3" on PWB, one probe (CH1) to "TP1A", the other (CH2) to "TP1B" and the external trigger to "TP3".
Set the oscilloscope as follows.

INPUT COUPLING MODE	AC
VERT MODE	ADD
INVERT	ON
TIME/DIV	20 msec
VOLTS/DIV (CH1, CH2)	50 mV

3. Insert a CE disk and close the door.
4. Load the head and look for a track around track 16 to have the positioning signal as shown in figure 4.15.3.
5. Press the button of TROO switch assembly microswitch. Proceed to step 7 if TROO signal (J1-26) goes low (0 to 0.4 V).
6. If TROO signal does not go low, move one step inward and turn the stepper clockwise until the positioning signal appears when the relative locations of stepper flange and stepper mounting screws are as in figure 4.15.2 (a). Move one step outward and turn the stepper counterclockwise until the positioning signal appears when as in figure 4.14.2 (b).

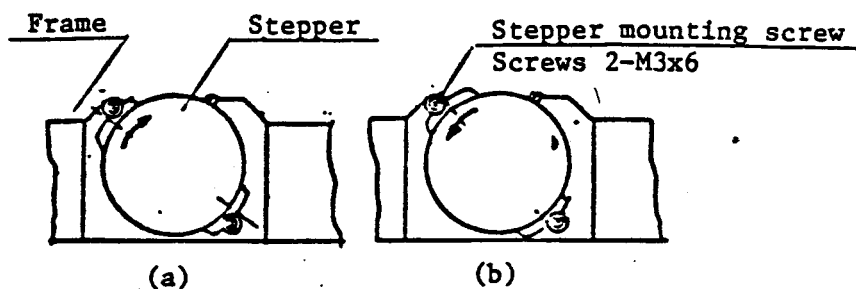


Fig. 4.15.2

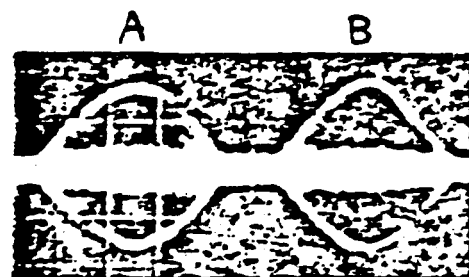
7. Rotate the stepper until A/B or B/A of SIDE 0 read output is within 1.0 to 0.9 and tighten the stepper mounting screws.
8. Step the carriage from track 17 to 16 and verify A/B or B/A of read output for 1.0 to 0.6. Repeat step 7 if out of 1.0 to 0.6.

When B is larger than A

$$A/B > 0.6$$

When A is larger than B

$$B/A > 0.6$$

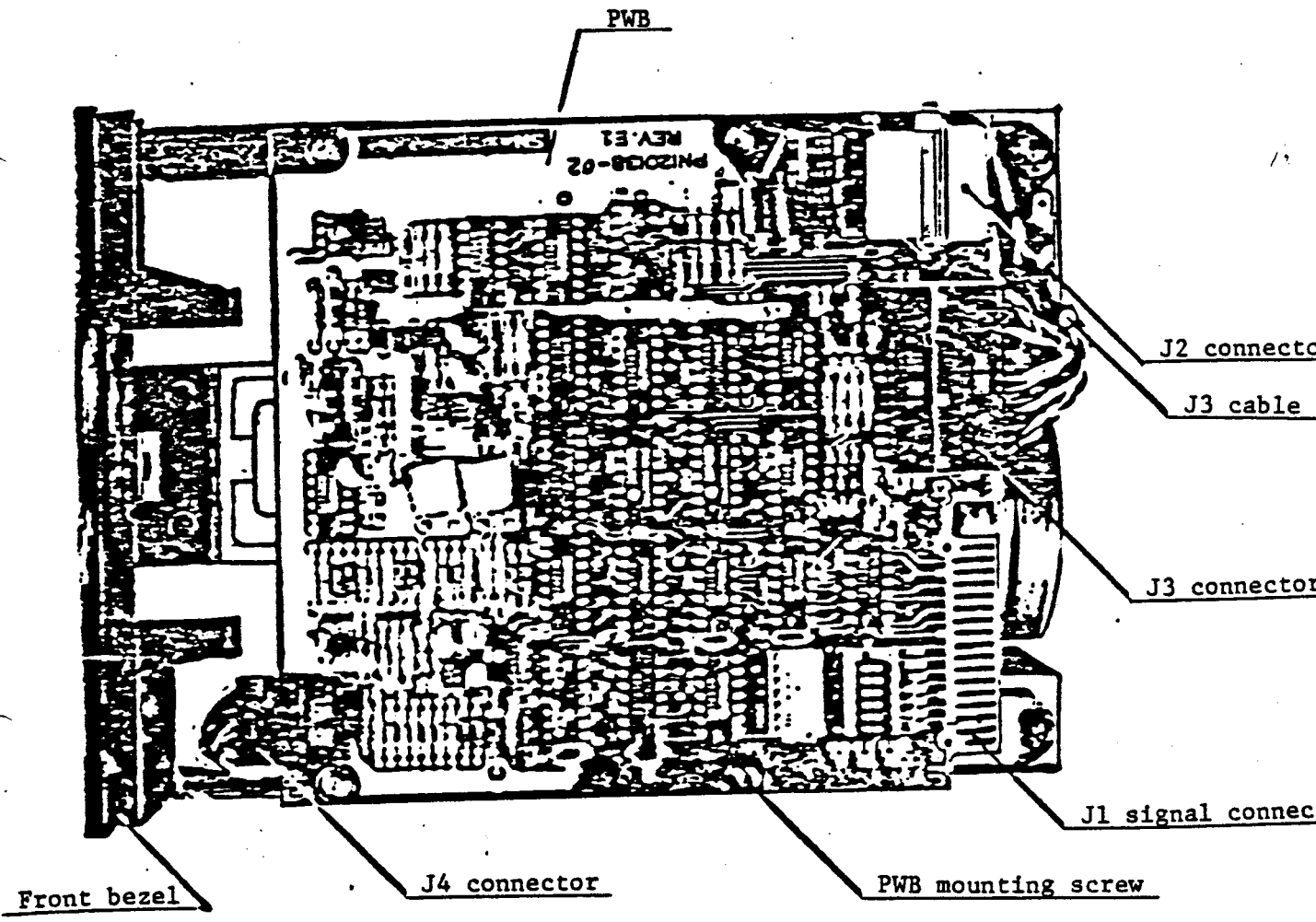


Positioning signal

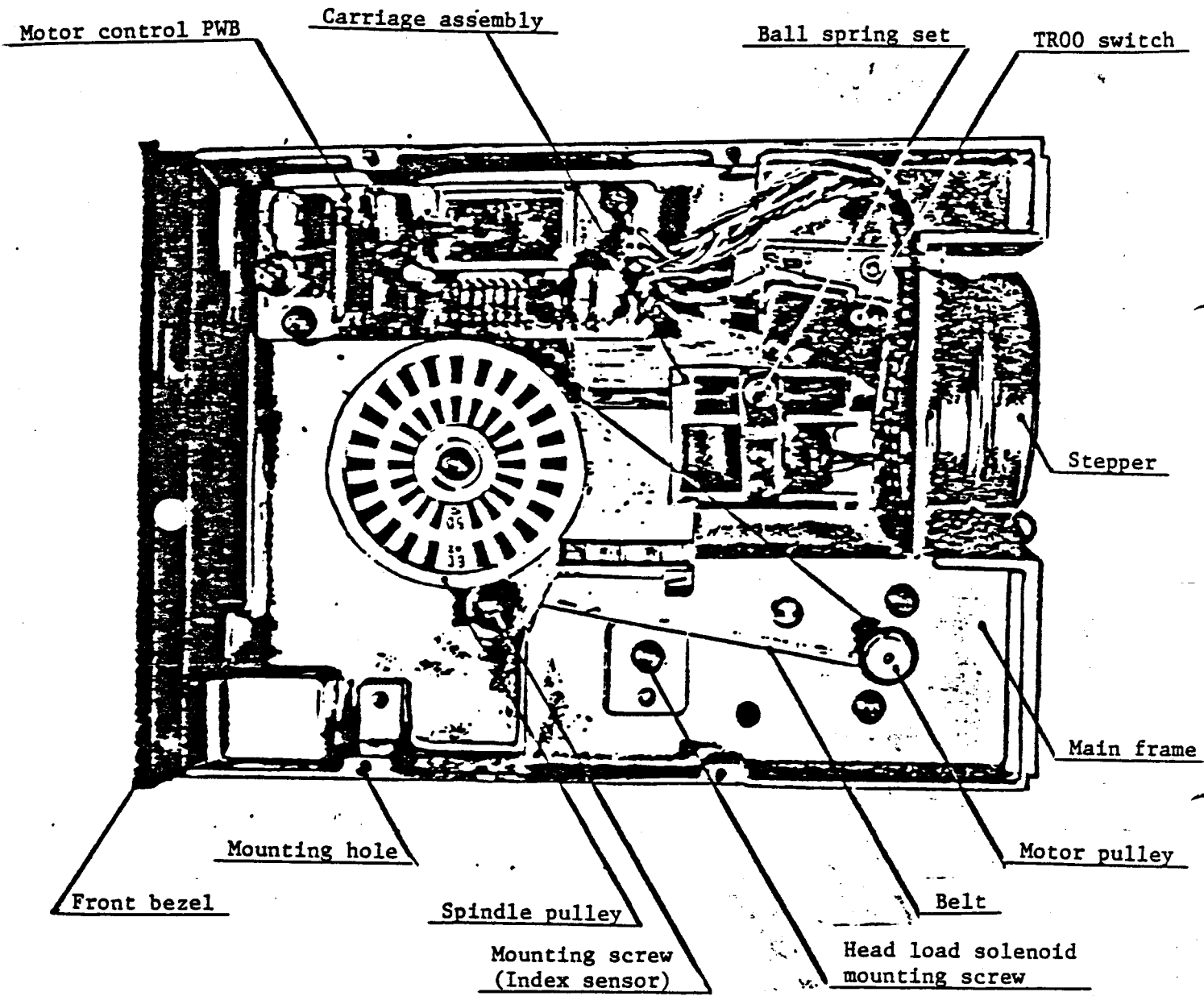
Fig. 4.15.3

9. Perform TROO switch assembly adjustment. (Reference section 4.8.3.)
10. Perform TROO stopper adjustment. (Reference section 4.9.2.)

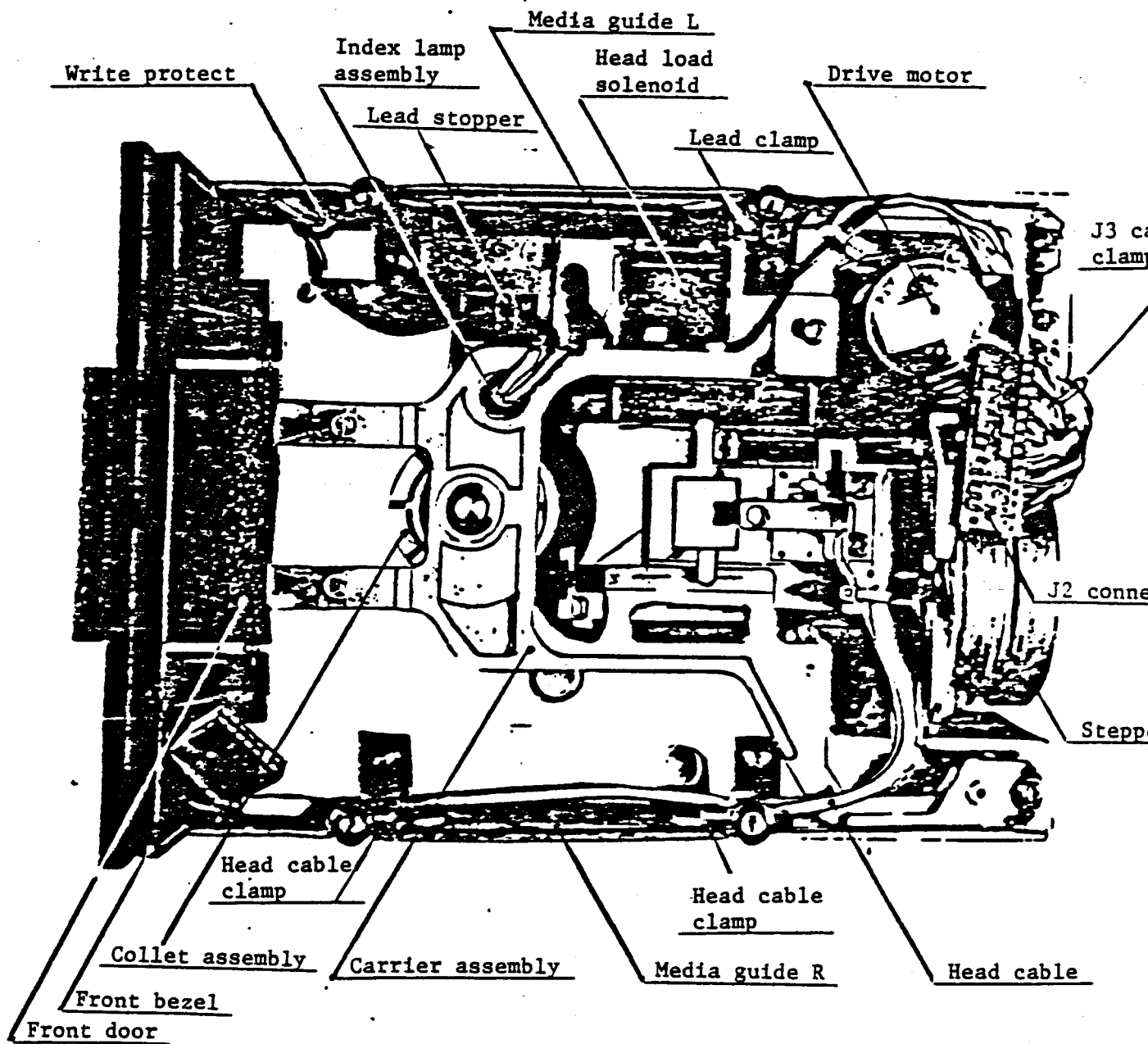
5. PARTS/ASSEMBLIES LOCATIONS



- Top view of YD-274 -
(Physical locations 1)

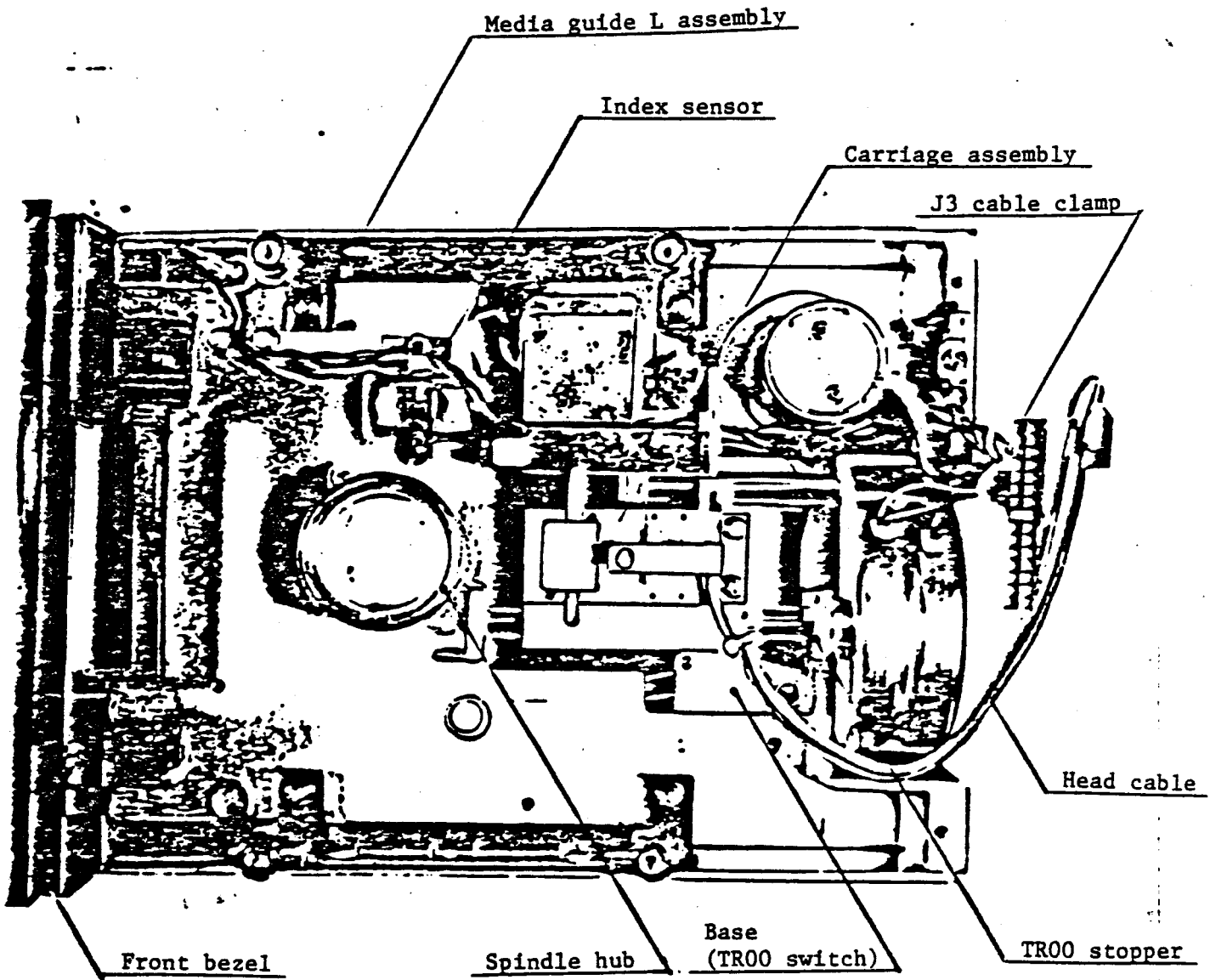


- Bottom view of YD-274 -
 (Physical locations 2)

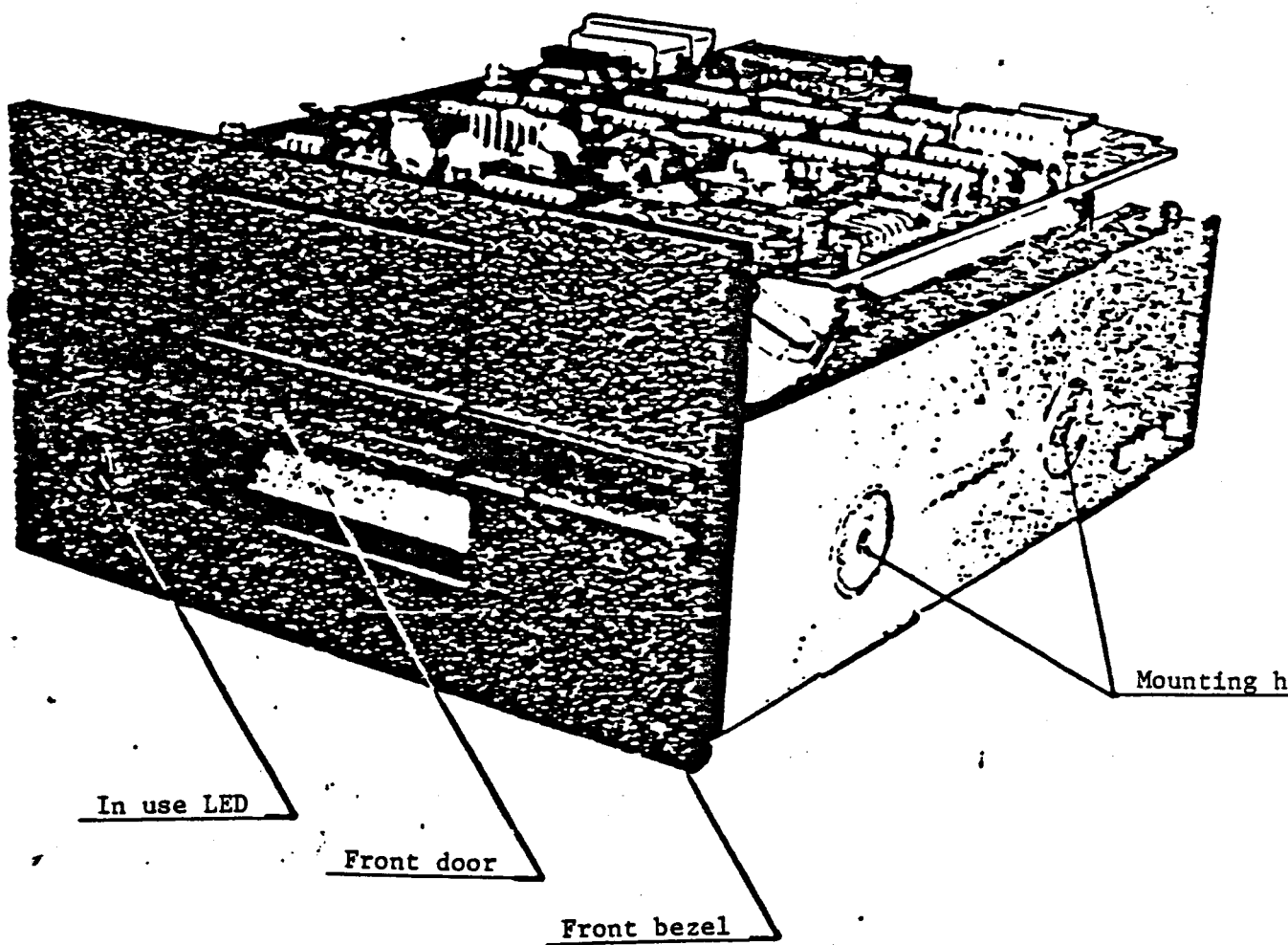


- Top view of YD-274 with PWB removed -

(Physical locations 3)



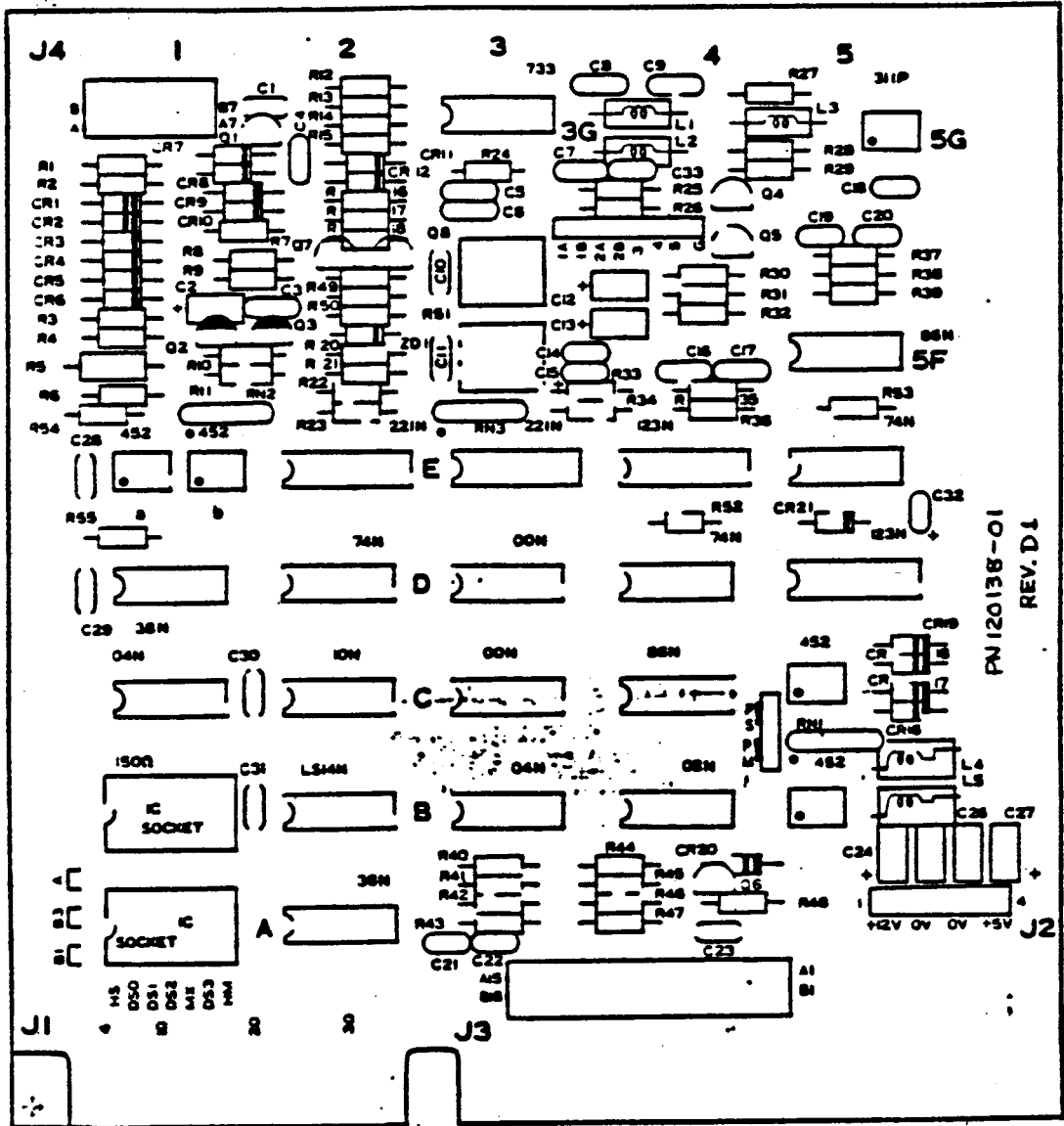
- Top view of YD-274 with PWB removed -
(Physical locations 4)



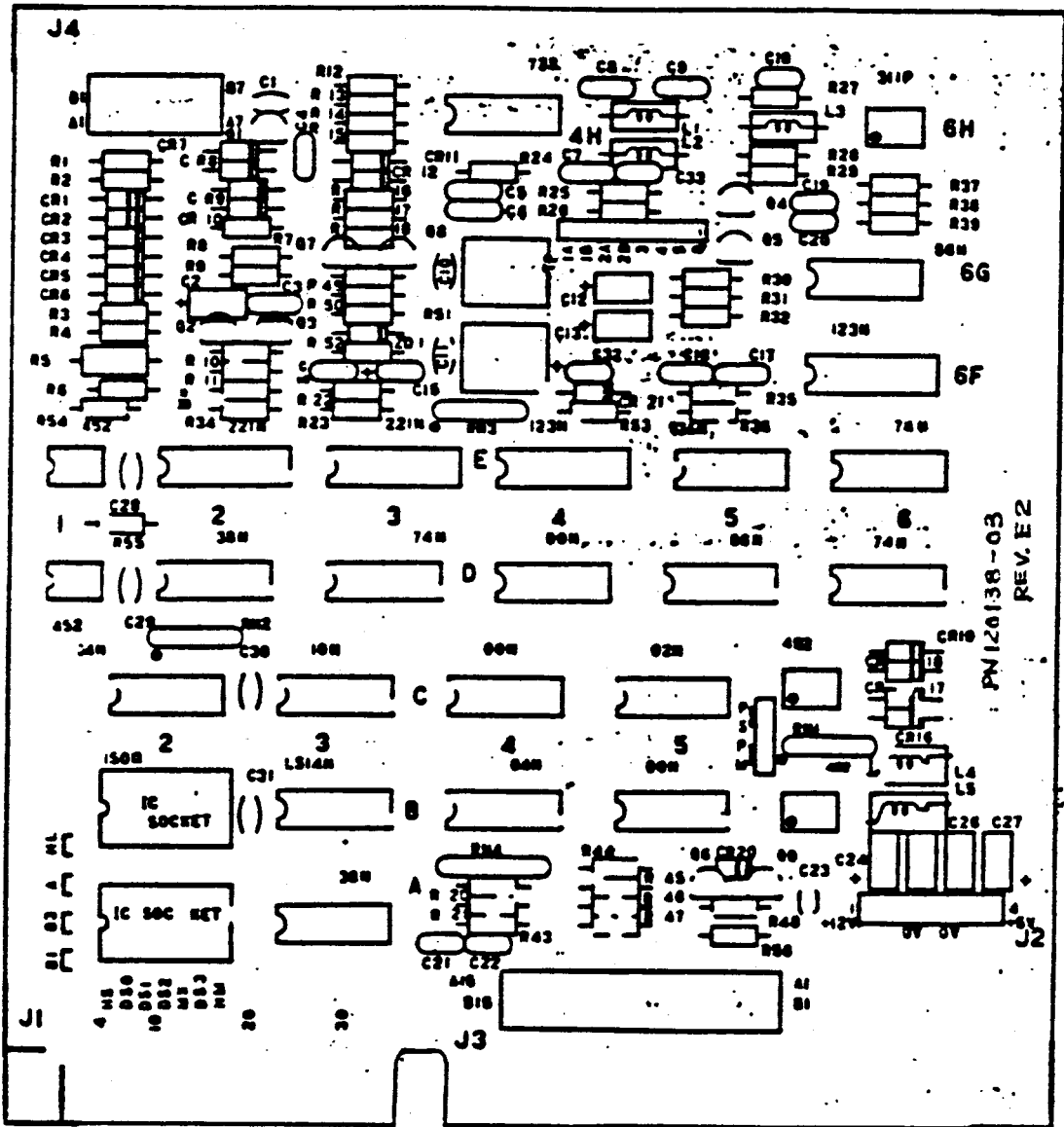
- Front view of YD-274 -
(Physical locations 5)

6. TEST POINTS/CONNECTOR PIN ASSIGNMENTS

PWB for Model 1301 P/N 120138-01



PWB for Model 1303 and 1304 P/N 120138-03



INTERFACE - J1

Pin No.	Signal Name
1	RETURN
2	---
3	RETURN
4	RESERVED
5	RETURN
6	DRIVE SELECT 3
7	RETURN
8	INDEX
9	RETURN
10	DRIVE SELECT 0
11	RETURN
12	DRIVE SELECT 1
13	RETURN
14	DRIVE SELECT 2
15	RETURN
16	MOTOR ON
17	RETURN
18	DIRECTION SELECT
19	RETURN
20	STEP
21	RETURN
22	WRITE DATA
23	RETURN
24	WRITE GATE
25	RETURN
26	TRACK 00
27	RETURN
28	WRITE PROTECT
29	RETURN
30	READ DATA
31	RETURN
32	SIDE ONE SELECT
33	RETURN
34	RESERVED

TRANSDUCER - J3

Pin No.	Signal Name	color
A1	MOTOR ON	blue
B1	+12V (DRIVE MOTOR)	red
A2	FRAME GROUND	brown
B2	+12V RETURN (DRIVE MOTOR)	black
A3		
B3		
A4	HEAD LOAD	green
B4	Head load +12VDC	white
A5	STEPPER A	black
B5	+12V (STEPPER)	red
A6	STEPPER B	yellow
B6	+12V (STEPPER)	red
A7	STEPPER C	brown
B7	STEPPER D	orange
A8	TROO SWITCH(NORMAL CLOSE)	yellow
B8	KEY	
A9	TROO SWITCH(NORMAL OPEN)	green
B9	TROO SWITCH RETURN	white
A10	IN USE LED RETURN	black
B10	+ IN USE LED	red
A11	INDEX LED RETURN	black
B11	+ INDEX LED	white
A12	INDEX PTX RETURN	black
B12	+ INDEX PTX	blue
A13	W/P LED RETURN	black
B13	+ W/P LED	yellow
A14	W/P PTX RETURN	black
B14	+ W/P PTX	orange
A15		
B15		

HEAD - J4

Pin No.	Signal Name	color
A1	SHIELD (HEAD0)	
B1	SHIELD (HEAD1)	
A2		
B2	KEY	
A3	ERASE (HEAD0)	red
B3	ERASE (HEAD1)	red
A4	W/R ERASE RETURN (HEAD0)	green
B4	W/R ERASE RETURN (HEAD1)	green
A5	W/R (HEAD0)	black
B5	W/R (HEAD1)	black
A6		
B6		
A7	W/R (HEAD0)	white
B7	W/R (HEAD1)	white

DC - J2

Pin No.	Signal Name
1	+12VDC
2	+12V RETURN
3	+5V RETURN
4	+5V DC

TEST POINTS

Pin No.	Signal Name
1A	PRE AMP 1A
1B	PRE AMP 1B
2A	PRE AMP 2A
2B	PRE AMP 2B
3	INDEX
4	ERASE
5	TRACK 00
9	GROUND

7. RECOMMENDED SPARE PARTS LIST

Maintenance Level 1

P/N	Part Description
140622-01	Belt
120138-01	PWB (Model 1301)
120138-03	PWB (Model 1303 and 1304)
140630-01	Index Lamp Assembly
120151-01	Media Guide L Assembly (with Write Protect Sensor & Lamp)
140640-01	In Use LED Assembly
130246-01	Drive Motor Assembly (with Motor Control PWB)

Maintenance Level 2

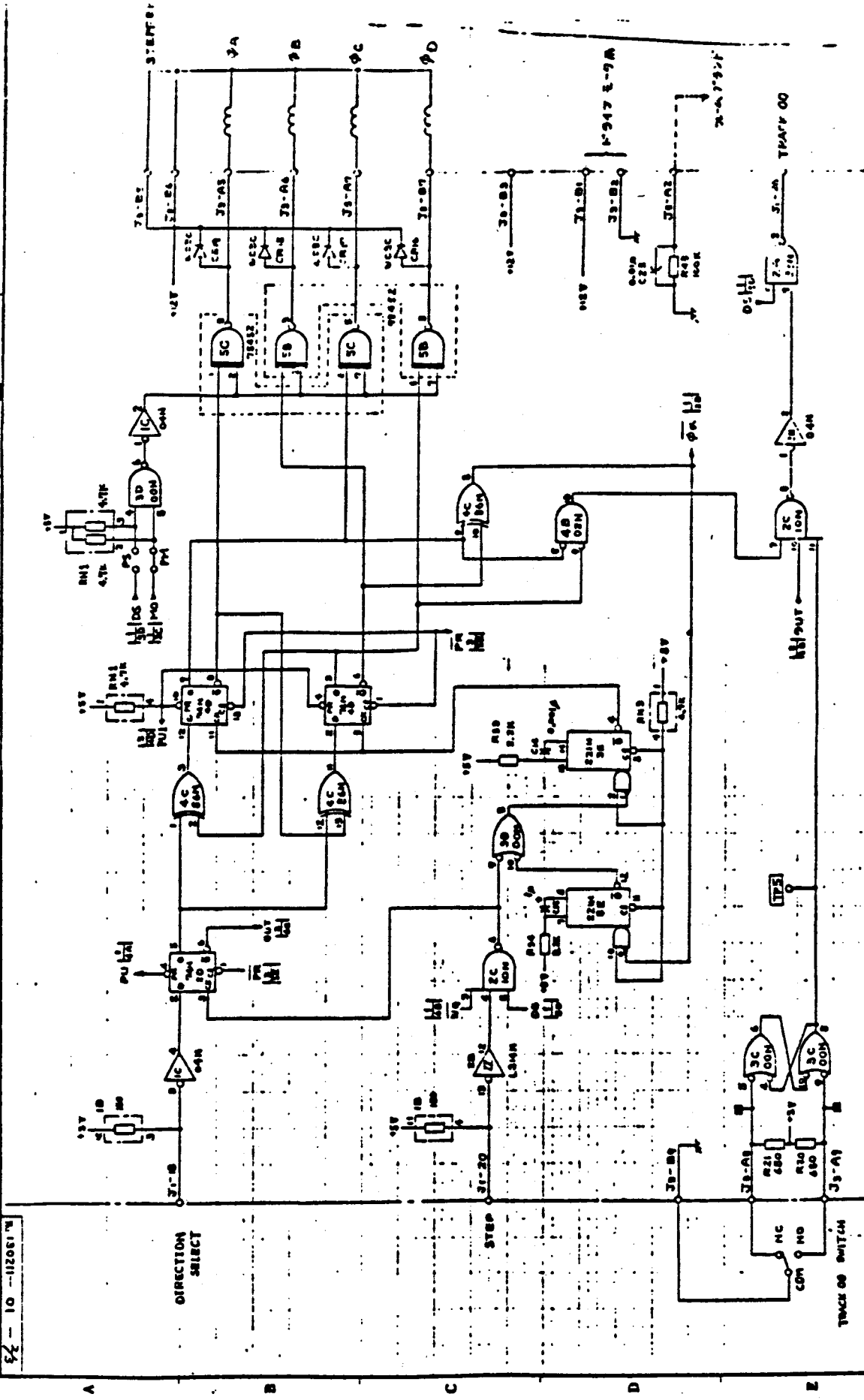
P/N	Part Description
140623-01	Index Sensor Assembly
140621-01	TROO Switch Assembly
130250-01	Head Load Solenoid Assembly
120145-02	Carrier Assembly
130252-01	Front Door Assembly
130253-01	Front Bezel Assembly
130247-01	Stepper
120200-01	Carriage Assembly

8. Schematics

1. Revision of schematics is controlled under revision code and the revision code is printed on the PWB and the schematics.
2. The revision code of attached schematics is as follows.

Model	P/N	Drawing Rev.
1301	PWB 120138-01	130211-01 Rev. D1
	Motor Control PWB 130330-02	130330-02 Rev. B
1304	PWB 120138-03	130211-02 Rev. E2
	Motor Control PWB 130330-02	130330-02 Rev. B

3. For actual maintenance, use the schematics with the same revision as of the specific drive to be maintained.



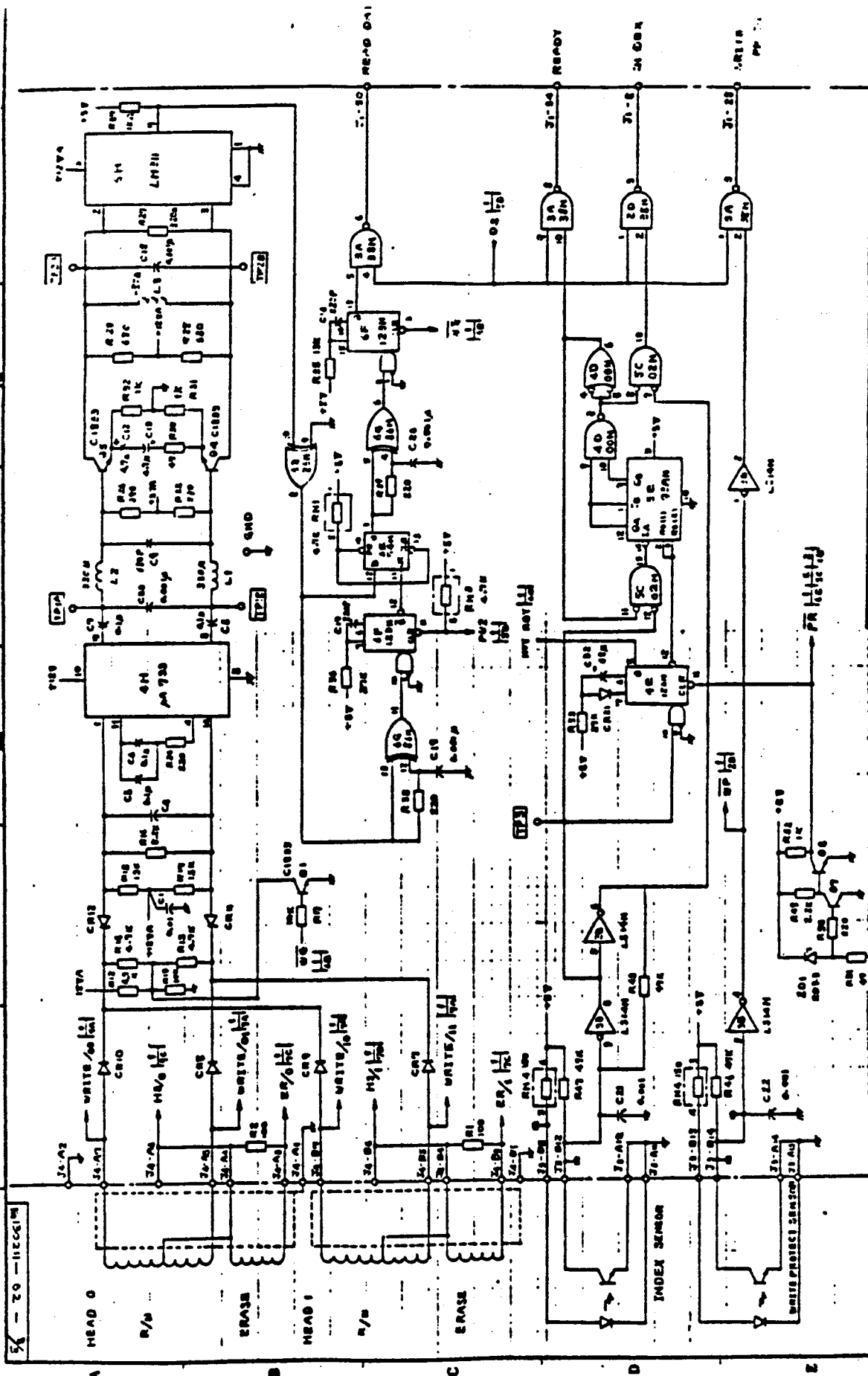
11-11020E-01

APPROVED AND CHECKED BY: [Signature] DATE: 11-11-73

FLOPPY DISK DRIVE

STEPPER

11-11020E-01



APPROVED BY: CHECKED BY: TESTED BY: DESIGNED BY: **Y-E DATA**

REV. A DATE 8 M REVISION DESCRIPTION 8 0 SIGN 9 4 ECO NO. 8888888

MODEL YO-274

READ/INDEX

PP 118

3A 30N 3A 30N 3A 30N

20 20N 20 20N 20 20N

31-50 READ/DATA 31-54 READY 31-5 31-6 31-20 31-22

4KV 4N E2 3/5

100V 40

-180211

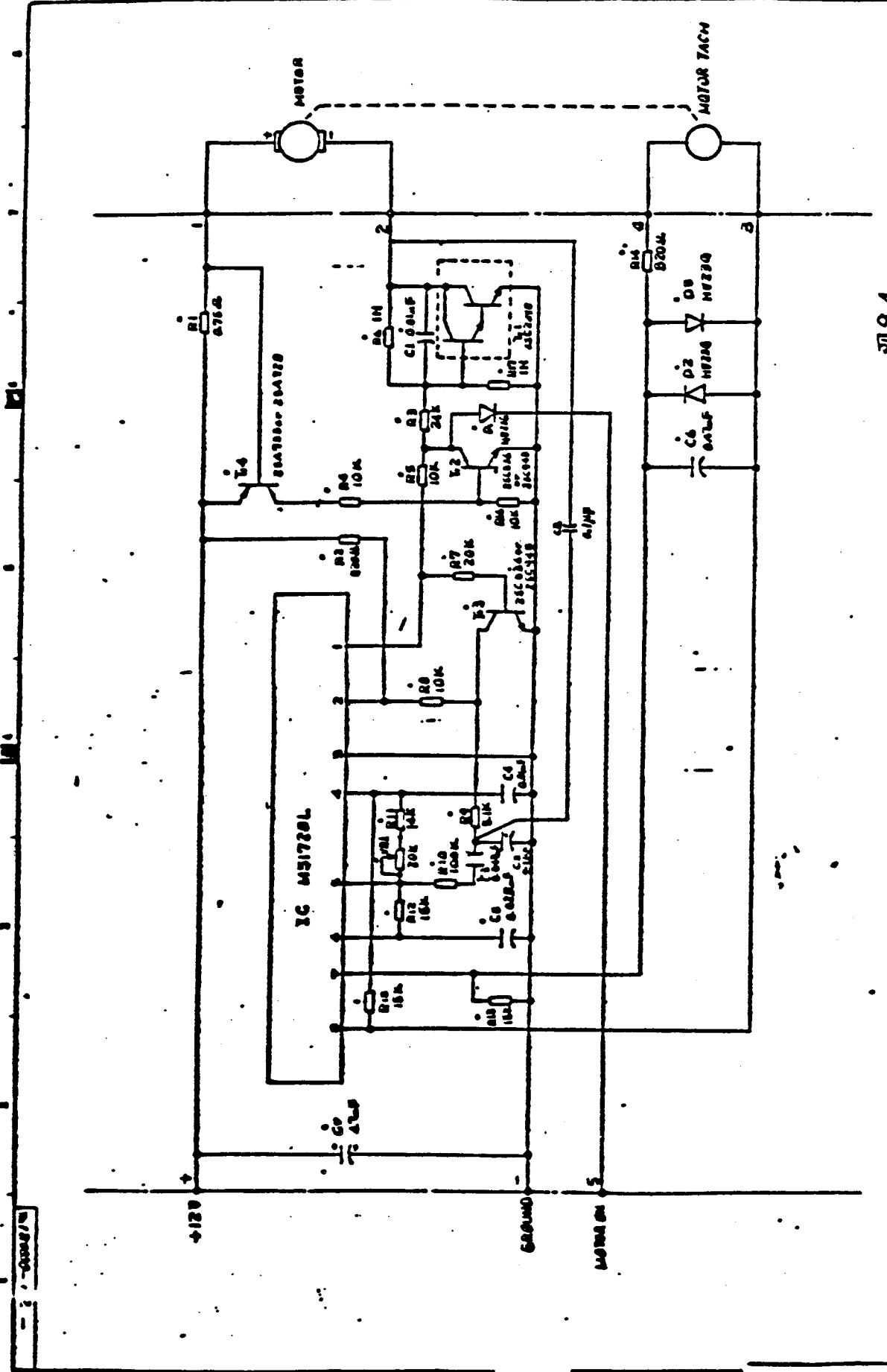


图 8.4

APPROVED BY CHECKED BY VERIFIED BY DESIGNED BY NAME: _____

REV: A1

DATE: 11/11

MODEL: YD-274

U.S. AIR FORCE

Y-E DATA

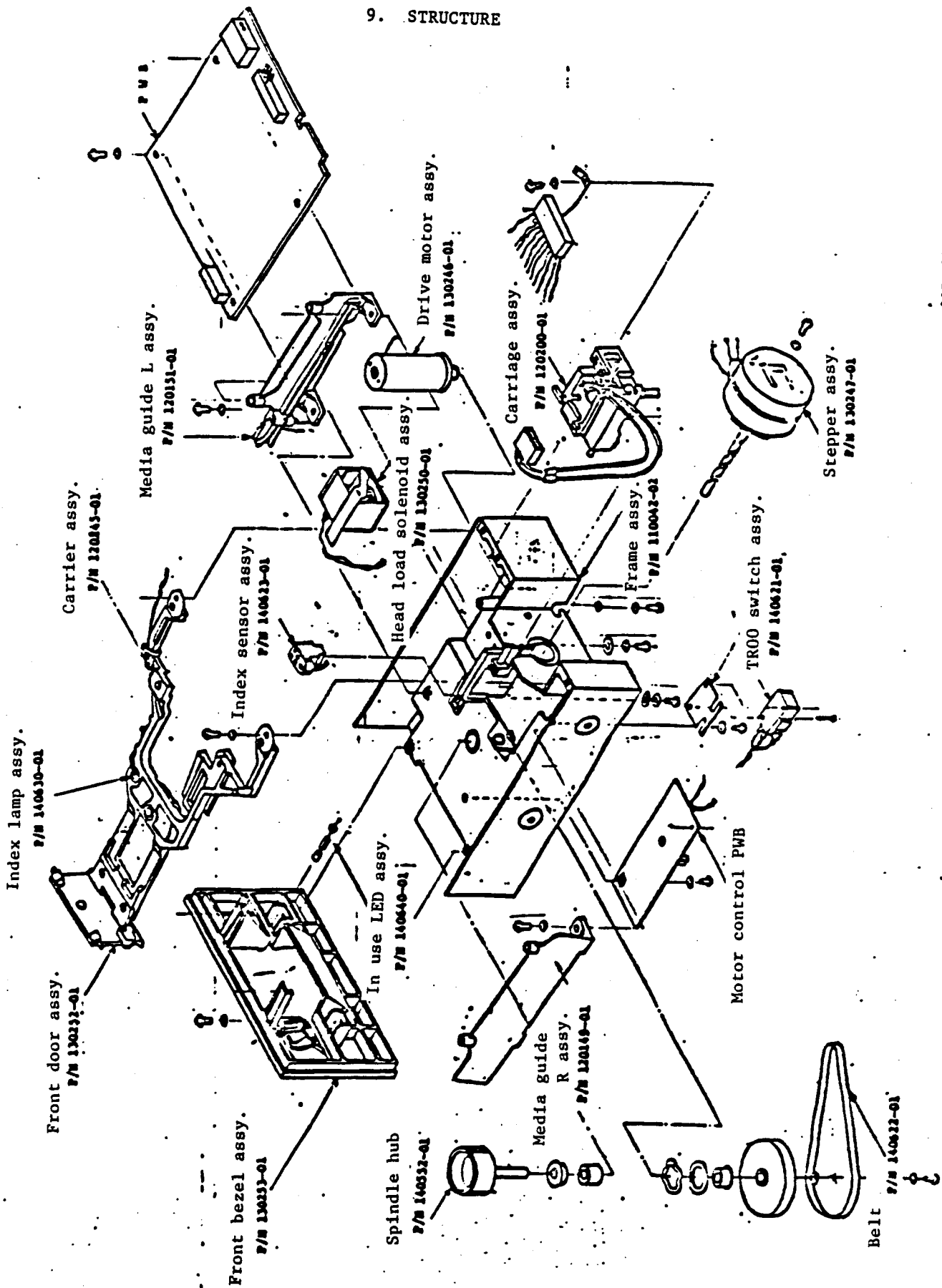
WEST ARMY: _____

130E30-02

REV.	DATE	BY	DESCRIPTION
A1	54-1-27	BMZ/EM	FPC-349317
A	12-2-73	VAH/PLP/EM	FPC-51705Y

通用規格

9. STRUCTURE



RETURN LETTER

Title: TWO-SIDED 5.25 INCH FLOPPY DISK DRIVE RCSL No.: 44-RT1992
YD-274, Maintenance Manual

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: _____ Title: _____

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Thank you

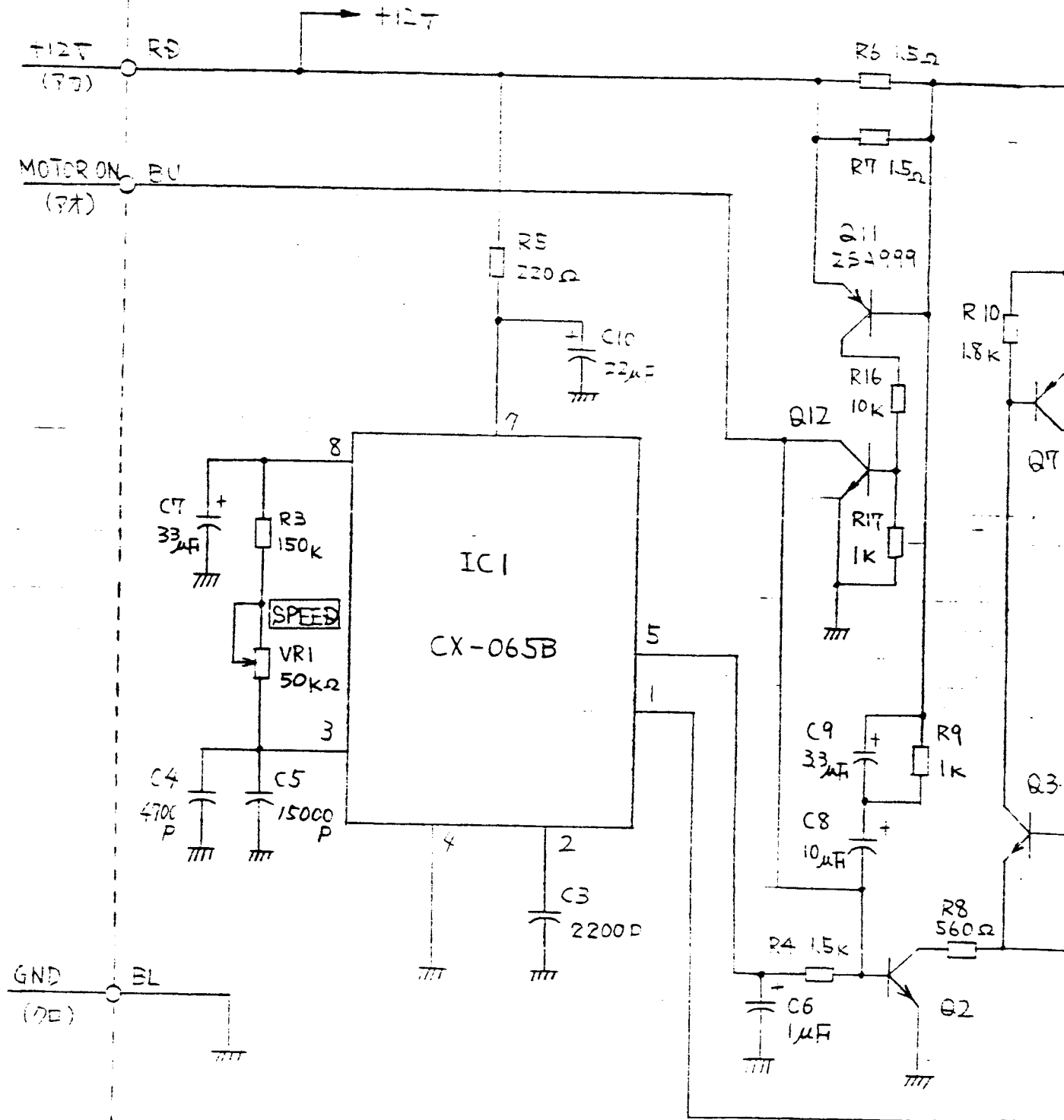
..... **Fold here**

..... **Do not tear - Fold here and staple**

**Affix
postage
here**

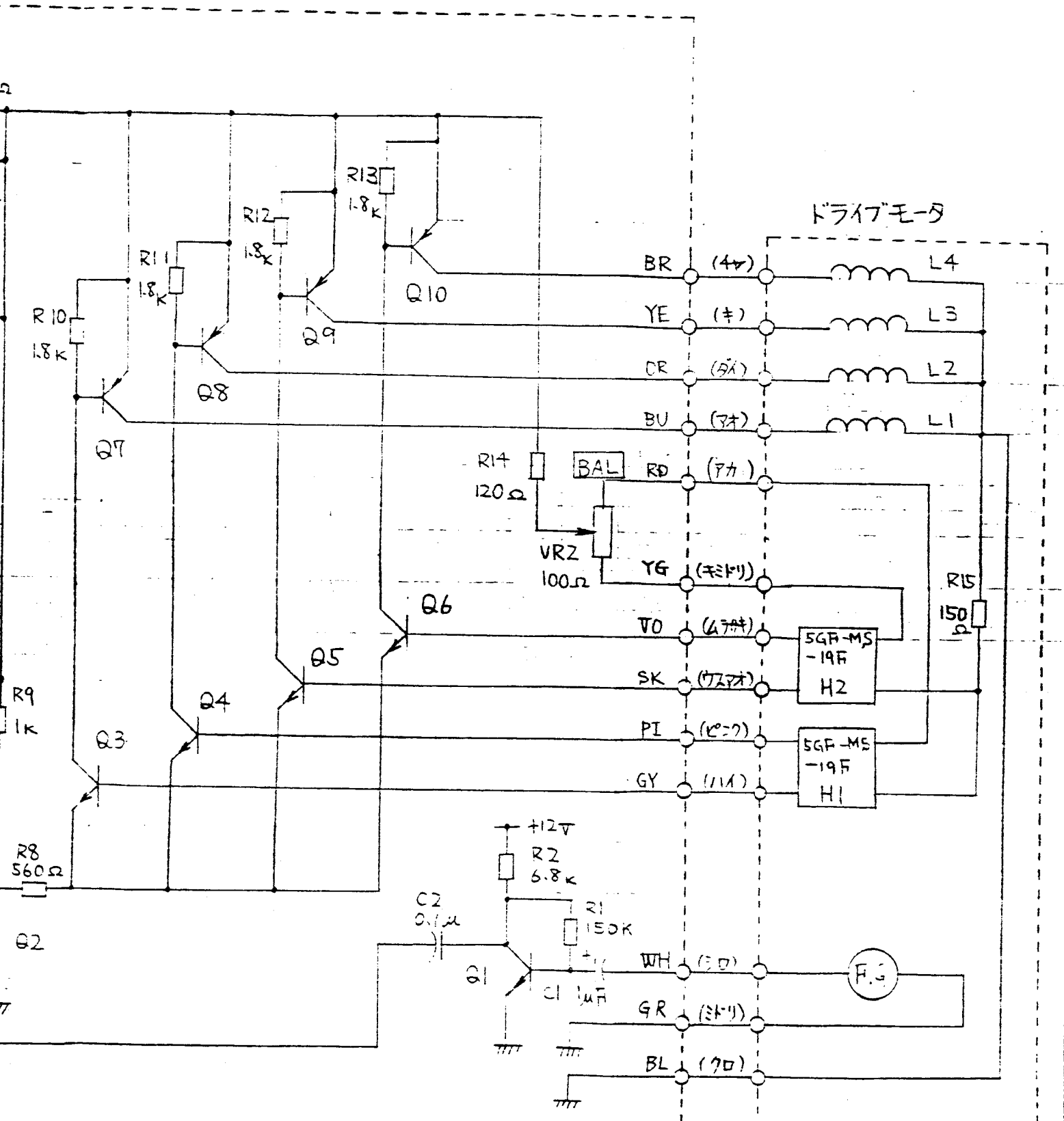
 **REGNECENTRALEN**
af 1979

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DK-2750 Ballerup
Denmark**

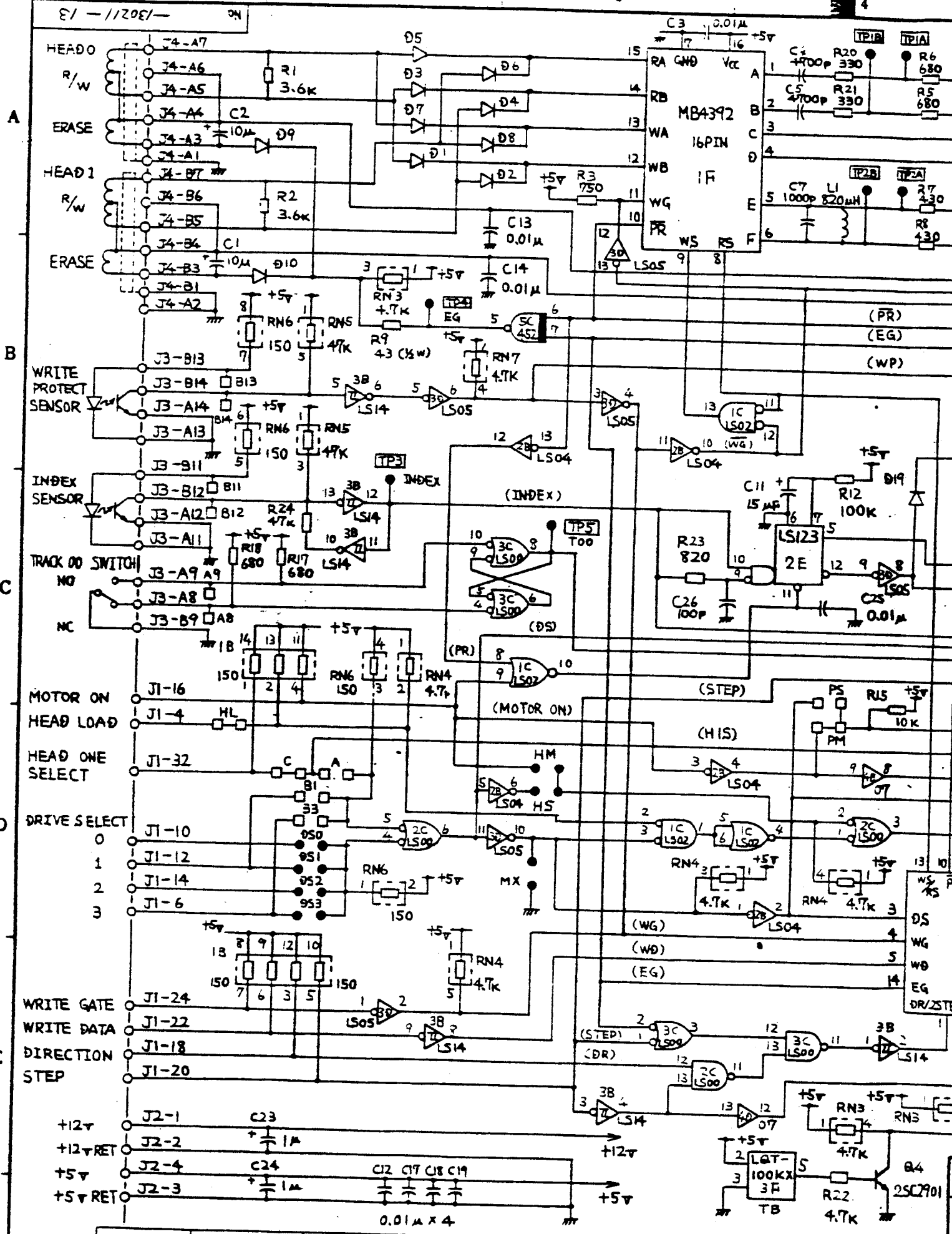


Q1 ~ Q6, Q12 → 2SC2320 又は 2SC945
 Q7 ~ Q10 → 2SA1020 又は 2SB564

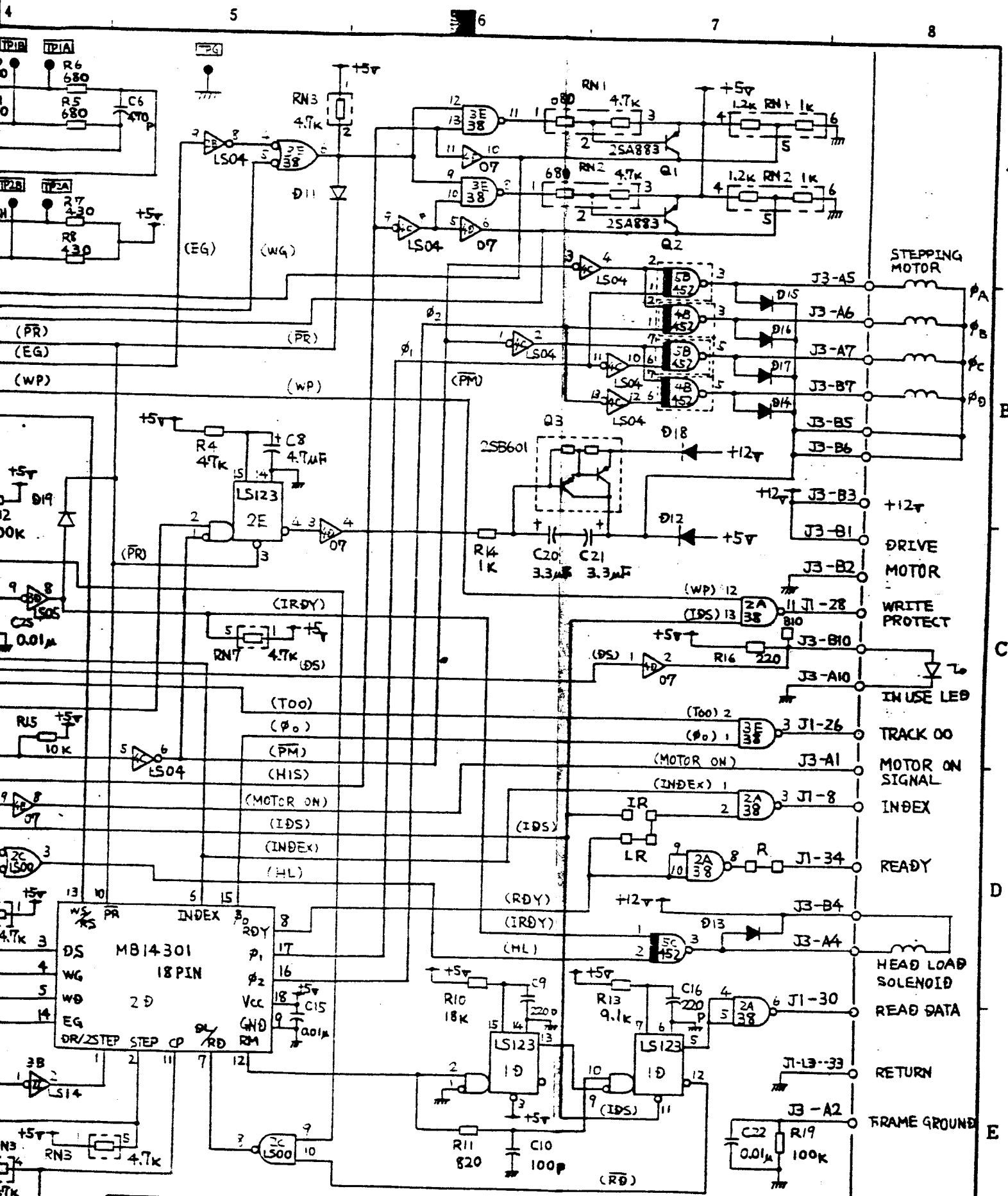
B1	56.4.3	VR1 30KΩ → 50KΩ	→ I)
B	56.1.12	線色: WH/R → YG, WH/BL → GR (回路変更時)	丹上
REV.	DATE	REVISION DESCRIPTION	SIGN 作成 ECO NO.



APPROVED BY	CHECKED BY	TRACED BY	DESIGNED BY	NAME 700k-ディスク装置	NEXT ASSY.
55.12.19	55.12.19	ミヤジ	55.12.19	モータ-コントロール基板	PN 141295-01
回路図				REV. B1	SHEET 1/1
MODEL 形式 YD-274				DWG.NO. 130574-01	
SYSTEM 番号				YED-06-A3	



G		56.11.6					
REV.	改版	DATE	日 月 年	REVISION DESCRIPTION	理由	SIGN	作 者
						ECO NO.	設計變更通知書



APPROVED BY		CHECKED BY		TRACED BY		DESIGNED BY		NAME		NEXT ASSY.	
56.11.16		56.11.14		宮地		56.11.10		70-心-ディスクドライブ		PN 120138-13	
内部接続図								REV. 改版 G		SHEET 1/1	
Y-E DATA								MODEL 形式 YD-274		DWG.NO. 5	
										-130211-13	