AA–P308A–TV

Rainbow™ 100

PC100 System Specification

digital equipment corporation

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PC100 SYSTEM SPECIFICATION

1.0 SYSTEM OVERVIEW

The PC100 system is a low-cost user installable personal business computer used to run applications in the Fortune 1000 marketplace. The PC100 provides hardware and software support for both stand-alone processing and as a terminal emulation for DEC and other computer manufacturer's systems.

The PC100 is designed to be used by users with no prior computer experience. Applications software include packages designed by third party software houses.

2.0 BASE SYSTEM

The base system consists of the following components:

2.1 BA25

The BA25 is the system nucleus. The multi-box is the primary housing for the system, and encloses the following components:

a. **PC100 System Module** - The basic intelligence of the system and provides the means for interconnection of all options. This module includes the following features:

   - o 8088 CPU
   - o Z80A CPU
   - o 64KB shared dynamic memory
   - o 24KB ROM
   - o 256 x 4 NVM
   - o VT100 compatible DC011, DC012 video electronics
   - o Async/Bisync communications port
   - o LA50, LA100, LA12 Printer Port
   - o LK201 Keyboard interface
   - o RX50 Floppy controller
   - o Option expansion capability
   - o Extended communications
   - o Color graphics
   - o Extended memory (64/192KB)

b. **RX50 Mini-Floppy Drive** - A dual platter mini-floppy drive system which is the main storage area for the system.

c. **H7842A Power Supply** - A 140 W switching regulator power supply with a switch selectable 115/230 V primary circuit.

2.2 VR201-A MONITOR

A 12-inch diagonal composite monitor that supplies video information to the user, as well as an interconnect means for the keyboard.

2.3 LK201-AA KEYBOARD

An ergonomic keyboard supporting 105 keys. This is interconnected via a coiled cord terminated in a four-conductor telephone plug.

3.0 SYSTEM MODULES

3.1 MOTHER BOARD

The PC100 includes a two-processor architecture based on the simultaneous operation of an 8088 and a Z80A CPU. These CPUs operate from and transfer data through a shared block of 62KB of RAM. In addition to this block of shared memory, each processor has its own memory and peripheral circuitry.

Note

> Because the floppy controller module is an integral part of the system, it is included in the mother board section.

In addition to running application/user software, each processor supports a portion of the needed functions of the computer. The Z80A processor performs the functions required to read/write the floppy disks. The 8088 handles the video output, keyboard I/O, printer port and the communications as well as any other options.

3.1.1 Mother Board Block Diagram

The Mother Board Block Diagram is shown in Figure 1.

```
   +---------------------INTERRUPT-----------------------------------+
   |                                                                 |
+---------+     +------+     +----------+                +---------+ |
|         |     |      |     |  SHARED  |------DMA-------|EXTENDED | |
|  Z80A   |-----|      |-----|  62 KB   |   +------+     | COMMS   | |
|         |     |      |     |   RAM    |---|      |     | OPTION  | |
|         |     |  8   |     +----------+   |      |     +---------+ |
+---------+     |      |     |   2 KB   |   |      |                 |
                |  B   |     | UNSHARED |---|  8   |                 |
                |  I   |     |   RAM    |   |      |     +---------+ |
+---------+     |  T   |     +----------+   |  B   |     |         | |
|  2 KB   |     |      |                    |  I   |-----|  8088   |-+
|UNSHARED |-----|  D   |                    |  T   |     |         |
|  RAM    |     |  A   |     +----------+   |      |     |         |
+---------+     |  T   |     |  24 KB   |---|  D   |     +---------+
                |  A   |     |   ROM    |   |  A   |
                |      |     +----------+   |  T   |
+---------+     |  B   |                    |  A   |     +---------+
|  RX50   |     |  U   |                    |      |     |         |
|  DISK   |-----|  S   |     +----------+   |  B   |-----|KEYBOARD |
|  DRIVE  |     |      |     | OPTIONAL |   |  U   |     |   I/F   |
|  I/F    |     |      |     |   RAM    |---|  S   |     |         |
+---------+     |      |     |(64 KB OR |   |      |     +---------+
                |      |     | 192 KB)  |   |      |
                +------+     +----------+   |      |     +---------+
                                            |      |     | ASYNC/  |
                             +----------+   |      |-----| BISYNC  |
                             | DC 11/12 |   |      |     | COMMS   |
                             |  VIDEO   |---|      |     +---------+
                             |CONTROLLER|   |      |
                             +----------+   |      |     +---------+
                               |    |       |      |     |         |
                               | +------+   |      |     | PRINTER |
                               | | 4 KB |   |      |-----|  PORT   |
                               | |SCREEN|---|      |     |         |
                               | | RAM  |   |      |     +---------+
                             +---+------+   |      |
                             |   4 KB   |   |      |     +---------+
                             |ATTRIBUTE |---|      |     |         |
                             |   RAM    |   |      |-----|  COLOR  |
                             +----------+   |      |     |GRAPHICS |
                                            |      |     |         |
                                            +------+     +---------+
```

Figure 1. Mother Board Block Diagram

3.1.2 8088 System

The 8088 microprocessor on the module controls nearly everything except the floppy disk. The 8088 runs from a clock of 4.815 MHz and controls the following:

- o Video
- o Keyboard
- o Printer
- o Communication line
- o Optional graphics board
- o Optional extended communications board

The 8088 also controls the Z80A's RESET line, as it can start/stop the Z80A at will. The clock time on the 8088 is approximately 208 nanoseconds. Contention from either the Z80A or refresh can cause wait states.

3.1.3 8088 Memory

The 8088 has several different types of memory available for its use:

a. 64KB dynamic memory (62KB shared)

b. 24KB ROM

c. 4KB video screen memory (static)

d. 4KB video attribute memory (static)

e. 256X4 NVM with shadow RAM

f. 64KB or 192KB optional unshared dynamic memory

3.1.3.1 Shared Memory - The standard 64KB bank of memory is shared Shared Memory with the Z80A processor. However, the Z80A is unable to address (and therefore can't modify) the first 2KB portion of this bank. Therefore, the 8088 keeps its interrupt vectors and some other information safe from being molested by a Z80A application. No parity generation/detection is implemented with the 64KB shared RAM.

If there is no contention for the shared RAM at the time of an 8088 access, no wait states are required for the cycle. If the RAM is busy due to a refresh cycle or a Z80A memory cycle, which was initiated prior to the 8088's request, wait states will occur until the request can be filled. Refresh has the highest priority for memory cycles. The 8088 has approximately equal priority with the Z80A.

3.1.3.2 **ROM** - There is 24KB of ROM (three sockets) on the module which is addressable by the 8088. The 24KB of ROM contains Z80A code and 8088 code for diagnostics, bootstrap, and VT102 emulation. The code for the Z80A must be moved into shared memory by the 8088 in order to be executed by the Z80A. No wait states are required when the 8088 accesses this memory; however, because the circuitry assumes that all memory is dynamic RAM, wait states will be excecuted whenever refresh cycles are in progress. Supported ROMs are of the 2732/2764 pinout variety, with access times <= 450 nsec.

3.1.3.3 **4KB Screen Memory And 4KB Attribute Memory** - There is screen and attribute memory available to the 8088 which allows it to control what is on the CRT display. This memory is available to the 8088 90 percent of the time. In the remaining ten percent, the DC011 and DC012 have access to this memory and prohibit the 8088 from access. Wait states to the 8088 occurs during refresh cycles and while the DC011 and DC012 are using the memory. The worst case time in which the 8088 can be held in a wait state due to contention with the DC011 and DC012 is approximately 120 microseconds.

3.1.3.4 **256 X 4 NVM With Shadow RAM** - The PC100 mother board contains 1024 bits of non-volatile storage that is organized 256 x 4. The NVM, as it is called, is located on the 8088 CPU bus at address 0ED000H through 0ED0FFH and the data path to the device is through data bits 0, 1, 2, and 3. Phantom images of the NVM exist from address 0ED100H through 0EDFFFH.

The device contains a 256 x 4 bit static RAM that performs as any other static memory. The device also contains a 256 x 4 bit non-volatile memory that is overlaid with the 256 x 4 bit static memory. On initialization, the 8088 does a RECALL of the NVM which places that data into the static memory. At this time, any read or write to the memory occurs to the static memory. The RECALL is done via a bit in the Diagnostic Write register. On power-up, this bit is set to a 0, and must be set to a 1 by firmware before data from the NVM RAM is available.

To perform a RECALL, the bit is set to a 0 and then set back to 1. The minimum width for this pulse is 450 ns. The data is available immediately after the RECALL bit is reset. The data that is in the static memory portion can be stored in the NVM by the 8088 CPU via the PROGRAM NVM bit also located in the Diagnostic Write register. This bit is also set to a 0 on power-up. To perform a PROGRAM NVM operation, the bit is set to a 1 and then back to a 0. This pulse has a minimum width of 100 ns. Once the PROGRAM NVM bit has met the minimum pulse width it can be removed, however, the device cannot be accessed by the CPU for 10 ms. At this time the device is in the process of storing the data into the NVM. There is no indication to the CPU that the device is done other than 10 ms has passed. If another operation is done on the device during those 10 ms, it will be ignored. Once the operation is started, it cannot be terminated unless the power is turned off. In this case, data in the device is not valid.

3.1.3.5 Unshared Dynamic Memory (Optional) - The module can optionally be expanded with 64KB or 192KB of memory for use by the 8088. If installed, this memory is always available and never requires wait states (except when the memory cycle contends with a refresh cycle).

3.1.3.6 8088 I/O Map - The 8088 I/O map follows:

PORT H	FUNCTION	
00H	Interrupts Z80A Flop (Write)	
00H	Clears 8088 Interrupt Flop (Read)	
02H	Communications and LED Register	WO
02H	General Communications Status	RO
04H	DC011 Write Register	WO
06H	Communications Bit Rate Register	WO
0AH	Maintenance Port	WO
0AH	Maintenance Port	RO
0CH	DC012 Write Register	WO
0EH	Printer Bit Rate Register	WO
10H	Keyboard Data Register(8251A)	RO/WO
11H	Keyboard Control/Status Register(8251A)	RO/WO
20H-2FH	Ext. Comm. Option/Option Select 1	
40H	Comm Data Reg. (7201)	RO/WO
41H	Printer Data Reg. (7201)	RO/WO
42H	Comm Control/Status Reg. (7201)	RO/WO
43H	Printer Control/Status Reg. (7201)	RO/WO
50H-5FH	Graphics Option Select	R/W
60H-6FH	Ext. Comm. Option/Option Select 2	

3.1.3.7 8088 Memory Map - The 8088 memory map is shown in Figure 2.

	FFFFF
ROM 2 (BOOT)	
	FE000
ROM 1	
	FC000
ROM 0	
	FA000
	F0000
ATTRIBUTE RAM	
	EF000
SCREEN RAM	
	EE000
NVM SHADOW	
	ED040
NVM	
	ED000
NVM SHADOW	
	EC000
	40000
OPTION RAM	
	10000
SHARED RAM	
	0

Figure 2. 8088 Memory Map

3.1.3.8 **8088 Interrupts** - The following table lists the 8088 interrupts.

Priority	Interrupt Source	Interrupt Type (Hex)	Vector Address (Hex)
Highest	Vertical Frequency Interrupt	20	80
↑	Graphics	22	88
	DMA Controller Interrupt (from Optional Extended Comm. Board)	23	8C
	Comm./Printer (7201) Interrupt	24	90
	Extended Comms Interrupt (optional)	25	94
	Keyboard (8251A) Interrupt	26	98
Lowest	Interrupt from Z80A	27	9C

3.1.3.9 **Video Subsystem: 8088** - The video subsystem resides on the mother board and is controlled by the 8088. The subsystem provides fully VT100-compatible video features.

3.1.3.9.1 **General Video Features** - The video subsystem supports the following features:

a. 24 line x 83 column display
b. 24 line x 137 column display
c. Smooth scrolling (full screen and split screen)
d. Double height lines
e. Double width lines
f Reverse video
g. Bold
h. Blinking
i. Underline
j. RS170 "like" composite video output
k. 256-character set

The software on the 8088 is able to vary the speed of the smooth scrolling, (e.g., 3, 6, 12, or 18 lines/sec). The double height and double width attributes may be selected on a line by line basis. The other attributes (reverse, bold, blink, and underline) may be selected on a character by character basis.

3.1.3.9.2 **Video Memory** - The video subsystem has 4KB of screen RAM and 4KB of attribute RAM. Only the four LSBs of the attribute RAM are actually looked at by the video subsystem.

3.1.3.9.3 **Video Processor (DC011 And DC012)** - When accessing the screen RAM, the video processor generates the 12-bit address for a particular byte in the lower 4KB bank (character RAM). The corresponding byte in the upper

4KB bank (attribute RAM) is selected also. The two bytes are passed to the video processor in parallel.

The video processor uses the character code to index into a character generator and uses the attribute information to modify the video data.

The contents of the screen RAM directly control the display of the lines and characters. This region of memory contains the displayable characters, their attributes the line attributes, and the addresses that link one line to the next. The microprocessor modifies and updates this information in the intervals between the video processor's DMAs.

The video processor begins reading the screen RAM at the start of RAM (location 0EE000H) following each vertical reset. Three bytes of control data are located at the end of each line of characters. The first byte, called the terminator, is FF hex and is a unique character that the video processor recognizes as the end of the line. The next two bytes form an address (low byte followed by high byte) which points to the first character of the next line to be displayed. The byte of attributes that corresponds to the low byte of the address contains three bits of line attributes which are applied to the line being pointed to.

Attribute RAM	Attribute Data	No Attrib.	Line Attribute No Attrib.
Character RAM	Character Data	Terminator	Address of Next Line

The bits are assigned in the following manner:

	D7	D6	D5	D4	D3	D2	D1	D0
Char. Attrib.	Unused	Unused	Unused	Unused	Not Under Line	Not Blink	Not Bold	Rev. Video
Char. Data	Alt. Char Set	Code for Character						
Line Attrib.	Unused	Unused	Unused	Unused	Unused	Double Width	Double Height	Scroll Region

(Smooth) scroll region - if set, this line scrolls: if not set, it doesn't

Double Height	Double Width	Result
0	0	bottom half double height
0	1	top half double height
1	0	double width
1	1	normal height, normal width

3.1.3.9.4 DC011 Programming Information - The DC011 video-timing chip can be accessed by the 8088 (WRITE-ONLY) at I/O address 4. The DC011 must be programmed with the desired refresh rate and column mode on power-up and after any mode changes. To program the DCC11, write two of the following four codes:

Code	Configuration
00	80 column mode sets
10	132 column mode interlaced mode
20	60 Hz mode resets
30	50 Hz mode interlaced mode

Interlaced/non-interlaced mode is determined by the order in which 80/132 column and 50/60 Hz are set. Every time the DC011 is programmed, its internal timing chain is reset. Since this causes the screen to jump, the DC011 should be programmed only if absolutely necessary. For example, the following two instructions set the DC011 to 80-column, 60 Hz, no interlace:

```
MOV AX,2000H
OUT  DC011,AX
```

Note

> When 80 column mode is selected, the video processor is actually capable of displaying 83 columns in single width mode or 41 columns in double width/height mode. When 132-column mode is selected, 137 columns can be displayed in single width mode or 68 columns in double width/height mode.

3.1.3.9.5 **DC012 Programming Information** - The DC012 video control chip can be accessed by the 8088 (WRITE-ONLY) at I/O address 0CH. The following codes are defined for the DC012:

Code	Result
00	Set scroll latch LSB's to 00
01	Set scroll latch LSB's to 01
02	Set scroll latch LSB's to 10
03	Set scroll latch LSB's to 11
04	Set scroll latch MSB's to 00
05	Set scroll latch MSB's to 01
06	Set scroll latch MSB's to 10
07	Set scroll latch MSB's to 11
08	Toggle blink flip flop
09	Clear vertical frequency interrupt
0A	Set reverse field on
0B	Set reverse field off
0C	Not supported
0D	Set basic attribute to reverse video with 24 lines and set blink flip flop off
0E	Not supported
0F	Set basic attribute to reverse video w/48 lines and set blink flip flop off

On power-up, the DC012 can be programmed to bring it to a known state. Typically, codes 0C, 04, 09, 0B, and 0D will be programmed at power-up time.

The value to which the scroll latch is set determines which scan row the first line of a scrolling region starts on. Likewise, it determines the last scan row displayed for the last line in a scrolling region.

For example, when the latch is set to zero (the degenerate case), the first line of the scroll region starts at scan row zero (so the line is completely visible). The last line of the scrolling region terminates at scan row 9 (so this line is also completely visible).

When the scroll latch is non-zero, for example 5, the first line of the scrolling region starts with scan row 5 (so only the bottom half of the line is visible). The last line of the scrolling region terminates at scan row 4 (so only the top half of the line is visible).

If the scroll latch is incremented from 0 through 9 and back to 0 again once each frame, the screen appears to smooth scroll from bottom to top (assuming that line linkages and line attributes are properly handled). On the other hand, if the scroll latch is decremented from 0 to 9 then down through 0, the screen appears to smooth scroll from top to bottom (again assuming that all line linkages and line attributes are properly handled).

A scrolling region is defined as a group of lines with their scrolling attributes set, surrounded by lines whose scrolling attribute is not set. Note that the scrolling attribute for a line resides in the line pointer information at the end of the previous line. Also, the first line on the screen (the one at RAM location 0), has its scrolling attribute reset by definition. Also note that the definition of a scrolling region does not preclude the definition of more than one scrolling region per screen, although that is of dubious value.

Whenever the scroll latch is non-zero, each scrolling region on the screen requires an extra (scrolling) line to be linked in. For example, if the scrolling region is 10 lines long, when the scroll latch is set non-zero there will have to be an eleventh line linked in. If scrolling up (incrementing the scroll latch), the line must be linked in at the bottom. When the scroll latch is incremented back to 0 again, the top line of the scrolling region must be unlinked. When scrolling down (decrementing the scroll latch), new lines must be linked in at the top of the scroll region and unlinked down at the bottom. All line linking/unlinking should be done during the vertical blanking interval (after the vertical frequency interrupt is rung). In 60-Hz mode, there are two blanked lines at the beginning of the screen (the line at RAM location 0, and the line that it points to).

The first line (at location 0) is guaranteed to have been read by the time that the interrupt service routine is entered; any changes to this line will not affect the screen until the next frame time.

However, the second line will not be read for over 500 usec. after asserting the interrupt.

If it is to be changed, it must be changed very soon after entering the interrupt service routine in order to guarantee that the change will be visible in the current frame.

Therefore, if the first visible line on the screen is involved in the scroll region and is being either linked in or unlinked, then the vertical interrupt routine must guarantee that its pointer (which resides in the second invisible line) is changed within approximately 500 usec after the ringing of the interrupt.

The modification of the scroll latch is much less time critical than this. Because the scroll latch is loaded by the DC012 by the vertical reset at the beginning of each frame, the only requirement is that the scroll latch be modified before the next frame begins. Note that the scroll latch value is the value that will be used during the next frame rather than the current frame.

3.1.3.10 Keyboard Interface - The interface to the keyboard is a RS423 full-duplex connection. The interface runs at 4800 bits per second asynchronous, with an 8-bit no parity character format. The UART used on the mother board is an 8251A. It must be set up in asynchronous mode with a 16 times clock and 8-bits no parity The recommended setup procedure is to output the following sequence to port 11 (hex):

(all values in hex)

0,0,0,40,4E,15

DURING THE INITIALIZATION, CONSECUTIVE WRITES MUST NOT BE SPACED ANY CLOSER THAN 3 MICROSECONDS.

The Status Read Format of the 8251A (input from Port 11 Hex) follows:

D7	D6	D5	D4	D3	D2	D1	D0
DSR	SYNDET/ BRKDET	FE	OE	PE	TxEMPTY	RxRDY	TxRDY

Note 1

SAME DEFINITIONS AS I/O PINS

PARITY ERROR - The PE flag is set when a parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit operation of the 8251A.

OVERRUN ERROR - The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction. OE does not inhibit operation of the 8251A, however, the previously overrun character is lost.

FRAMING ERROR (Async only) - The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the 8251A.

DATA SET READY - Indicates that the DSR is at a zero level. Used to read a manufacturing jumper. TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by -CTS and TxEN; the latter is conditioned by both -CTS and TxEN. i.e., TxRDY status bit = DB Buffer Empty TxRDY pin out = DB Buffer Empty (-CTS=0) (TxEN=1)

Note 2

TxE (Transmitter Empty) - When the 8251A has no characters to send, the TxEMPTY output will go "high". It resets upon receiving a character from the CPU if the transmitter is enabled. TxEMPTY remains low when the transmitter is disabled if it is actually empty.

RxRDY (Receiver Ready) - This output indicates that the 8251A contains a character that is ready to be input to the CPU. RxRDY is connected to the interrupt structure of the CPU. For polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

TxRDY (Transmitter Ready) - This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin is used as an interrupt to the system, since it is masked by TxEnable. For Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of -WR when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is not masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data Input Register.

Parity errors should not occur. A hardware or software problem exists if parity errors do occur. The keyboard generates an interrupt to the 8088 when either the TxRDY pin or the RxRDY pin is asserted. The interrupt is a type 26 Hex.

3.1.3.11 Printer Port Interface - This is a general purpose printer port which provides an RS423 interface compatible with DEC printers. EIA signals supported are:

- o Transmit Data
- o Receive Data
- o Data Terminal Ready
- o Data Set Ready asserted

Software programmable bit rates supported are:

o 75	o 1200
o 150	o 2400
o 300	o 4800
o 600	o 9600

Printer bit rates are selected by writing the following to 8088 port 0EH:

Data Bit 0-2	Bit Rate
0	75
1	150
2	300
3	600
4	1200
5	2400
6	4800
7	9600

Note

Bit 3 controls the communications port clock.

Software-programmable character formats supported are 5-8 bits/character with 1, 1-1/2, or 2 stop bits/character. Parity may be selected as odd, even or none. Software should support XON/XOFF restraint protocol for this port. The D-type 25-pin female EIA printer connector physically resides on the mother board in the normal printer port location and attaches directly to a printer. DSR and CTS are always asserted.

3.1.4 MPSC Overview

The 7201 Multi-Protocol Serial Controller is a microcomputer peripheral device that supports Asynchronous (Start/Stop), Byte Synchronous (Monosync, IBM Bisync), and Bit Synchronous (ISO's HDLC, IBM's SDLC) protocols. This controller's flexible architecture allows implementation of many variations of these three protocols with low software and hardware overhead.

The Multi-Protocol Serial Controller (MPSC) implements two independent serial receiver/transmitter channels. The printer port uses one channel and the communications port uses the other channel.

As implemented on the mother board, the MPSC supports two microprocessor interface options: Polled and Interrupt.

3.1.4.1 Asynchronous Operations - General - For operation in the asynchronous mode, the MPSC must be initialized with the following information:

- o character length (WR3; D7, D6 and WR5; D6, D5)
- o clock rate (WR4; D7, D6)
- o number of stop bits (WR4; D3, D2)
- o odd, even or no parity (WR4; D1, D0)
- o interrupt mode (WR1, WR2)
- o receiver (WR3; D0) or transmitter (WR5; D3) enable

When loading these parameters into the MPSC, WR4 information must be written before the WR1, WR3, WR5 parameters/commands.

For transmission via a modem or RS423 interface, the Request To Send (RTS) (WR5; D1) and Data Terminal Ready (DTR) (WR5; D7) bits must be set along with the Transmit Enable bit (WR5; D3). Setting the Auto Enables (WR3; D5) bit allows the programmer to send the first character of the message without waiting for a clear to send (CTS).

Both the Framing Error and Receive Overrun Error flags are latched and cause an interrupt.

If the External/Status Interrupt bit (WR1; D0) is enabled, Break Detect (RR0; D7) and Carrier Detect (RR0; D3) will cause an interrupt. Reset External/Status Interrupts (WR0; D5, D4, D3) will clear Break Detect and Carrier Detect bits if they are set.

A status read after a data read will include error status for the next word in the buffer. If the Interrupt on First Character (WR1; D4, D3) is selected, then data and error status are held until an Error Reset command (WR0; D5, D4, D3) is given.

If the Interrupt on Every Character Mode bit (WR1; D4, D3) is selected, the interrupt vector is different if there is an error status in RR1. When the character is read, the error status bit is set and the Special Receive Condition vector is returned if Status Affects vector (WR1B; D2) is selected.

In a polled environment, the Receive Character Available bit (RR0; D0) must be monitored so that the CPU can determine when data is available. The bit is reset automatically when the data is read. If the X1 clock mode is selected, the bit synchronization must be accomplished externally.

Refer to Figure 3.

	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 b/CHAR 11 RX 8 b/CHAR		AUTO ENABLES	0	0	0	0	RX ENABLE
WR4	00 X1 CLOCK 01 X16 CLOCK 10 X32 CLOCK 11 X64 CLOCK		0	0	00 ENABLE SYNC MODES 01 1 STOP BIT 10 1.5 STOP BIT 11 2 STOP BITS		EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 b/CHAR 01 TX 7 b/CHAR 10 TX 6 b/CHAR 11 TX 8 b/CHAR		SEND BREAK	TX ENABLE	0	RTS	0

Figure 3. Asynchronous Mode Register Setup

3.1.4.2 Communications Port - This port is used to communicate to another computer. It has full modem support and supports the same signals as the VT102. U.S. and European full- and half-duplex modems can be supported by this port. The port has ASYNC as well as BISYNC modes with a RS423 (V.24/V.28) physical interface conforming to CCITT V.21, V.22 and V.23. Break detection by this port is supported. Bit rates supported are:

- o 50
- o 75
- o 110
- o 134.5
- o 150
- o 200
- o 300
- o 600
- o 1200
- o 1800
- o 2000
- o 2400
- o 3600
- o 4800
- o 9600
- o 19200

Communications bit rates are selected by writing the following to 8088 port 06H:

Nibble Data	Bit Rate	Percent Error
0 H	50	0
1 H	75	0
2 H	110	0
3 H	134.5	0
4 H	150	0
5 H	200	0
6 H	300	0
7 H	600	0
8 H	1200	+.14
9 H	1800	0
A H	2000	0
B H	2400	-.17
C H	3600	+.46
D H	4800	+.46
E H	9600	+.46
F H	19200	-2.04

The low nibble of the data written to port 06H sets the transmit clock while the high nibble sets the receive clock.

For example: Data 0AH written to 8088 port 06H would set the receive bit rate to 50 and the transmit bit rate to 2000.

Bit 3 on port 0EH selects the comm port clocks (RxC, TxC). External when set; internal when reset.

Note

Bit 0-2 on port 0EH controls the printer port bit rates.

All bit rates are software selectable. Transmit and receive bit rates may be selected independently from the available bit rates. The ROM code supports VT102 emulation on this port.

Signals supported are:

1. Receive Data
2. Transmit Data
3. Secondary Transmit Data
4. Request to Send
5. Secondary Request to Send
6. Clear to Send
7. Secondary Clear to Send
8. Receive Line Signal Detect
9. Secondary Receive Line Signal Detect/Speed Indicator (Bell 212A)
10. Ring Indicator
11. Data Set Ready
12. Speed Select

3.1.4.3 Synchronous Operation -- Mono Sync, Bi Sync -- General - The MPSC must be initialized with the following parameters:

- o odd or even parity (WR4; D1, D0)
- o X1 clock mode (WR4; D7, D6)
- o 8- or 16-bit sync character (WR4; D5, D4)
- o CRC polynomial (WR5; D2)
- o Transmitter Enable (WR5; D3)
- o Interrupt modes (WR1, WR2)
- o Transmit character length (WR5; D6, D5)
- o Receive character length (WR3; D7, D6

WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7. The data is transmitted on the falling edge of the Transmit Clock (TxC) and is received on the rising edge of Receive Clock (RxC). The X1 clock is used for both transmit and receive operations for all three sync modes: Mono, Bi and External.

	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 b/CHAR 11 RX 8 b/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	0	SYNC CHAR LOAD INHIBIT	RX ENABLE
WR4	0	0	00 8 BIT SYNC 01 16 BIT SYNC 11 EXT SYNC		0	0	EVEN/ ODD PARITY	PARITY ENABLE
WR5	DTR	00 TX 5 b/CHAR 01 TX 7 b/CHAR 10 TX 6 b/CHAR 11 TX 8 b/CHAR		SEND BREAK	TX ENABLE	1 (SELECT CRC-16)	RTS	TX CRC ENABLE

Figure 4. Synchronous Mode Register Setup -- Monosync, Bisync

3.1.4.4 Synchronous Operation -- SDLC -- General - Like the other synchronous operations the SDLC mode must be initialized with the following parameters:

- o SDLC mode (WR4; D5, D4)
- o SDLC polynomial (WR5; D2)
- o Request to Send, Data Terminal Ready, transmit character length (WR5; D6, D5)
- o Interrupt modes (WR1; WR2)
- o Transmit enable (WR5; D3)
- o Receive enable (WR3; D0)
- o Auto enable (WR3; D5)
- o External/status interrupt (WR1; D0)

WR4 parameters must be written before WR1, WR3, WR5, WR6 and WR7.

	D7	D6	D5	D4	D3	D2	D1	D0
WR3	00 RX 5 B/CHAR 01 RX 7 B/CHAR 10 RX 6 b/CHAR 11 RX 8 b/CHAR		AUTO ENABLES	ENTER HUNT MODE	RX CRC ENABLE	ADDRESS SEARCH MODE	0	RX ENABLE
WR4	0	0	0 1 (SELECTS SDLC/HDLC MODE)		0	0	0	0
WR5	DTR	00 TX< 6b/CHAR 01 TX 7 b/CHAR 10 TX 6 b/CHAR 11 TX 8 b/CHAR		0	TX ENABLE	0 (SELECT SDLC CRC)	RTS	TX CRC ENABLE

Figure 5. Synchronous Mode Register Setup -- SDLC/HDLC

3.1.5 Z80A System

The following describes the section of the system controlled directly by the Z80A

3.1.5.1 Z80A CPU - The module includes one Z80A microprocessor, which runs from a clock of 4.012 MHz. The Z80A alone has access to the floppy disk interface and thus is responsible for controlling the floppy (via programmed I/O) for all applications.

3.1.5.2 Z80A Shared Memory - The Z80A has available to it 64KB RAM, which is divided into 62KB shared and 2KB unshared memory. Accesses to the shared portion of memory select the corresponding address in the standard bank of 64KB RAMS. Accesses to the unshared memory select a private 2Kx8 byte-wide static RAM.

3.1.5.3 Z80A Private RAM - The unshared RAM may be accessed by the Z80A at any time without any wait states. If the shared RAM is "busy" at the time of a Z80A access, the Z80A will execute wait states until the RAM is free. The RAM is considered "busy" when an 8088 cycle or a refresh cycle is in progress or is pending. In addition to wait cycles due to contention, all M1 cycles from the shared RAM have one extra wait cycle due to the timing for this sort of machine cycle. In any case, the Z80A is held in a wait state for no longer than approximately two microseconds. If both processors are executing out of the shared memory, the Z80A cannot reliably access the floppy disk (i.e., lost data errors will often result).

3.1.5.4 Z80A I/O Map - The following is the Z80A I/O map.

PORT	FUNCTION	
00H	Clear Interrupt to Z80A (Read)	
00H	Interrupts 8088 (Write)	
21H	Disk Diagnostic Read Register	RO
21H	Disk Diagnostic Write Register	WO
40H	Disk Control Read Register	RO
40H	Disk Control Write Register	WO
60H	FDC Status Register	RO
60H	FDC Control Register	WO
61H	FDC Track Register	R/W
62H	FDC Sector Register	R/W
63H	FDC Data Register	R/W

Note

The above Z80A I/O ports are remapped within their own pages and are also remapped starting at 80H. Writing Diagnostic Write Register at address 21H will reset ZFLIP. Writing the Diagnostic Write Register at address [illegible] will set ZFLIP.

3.1.5.5 Z80A Memory Map - The Z80A memory map follows:

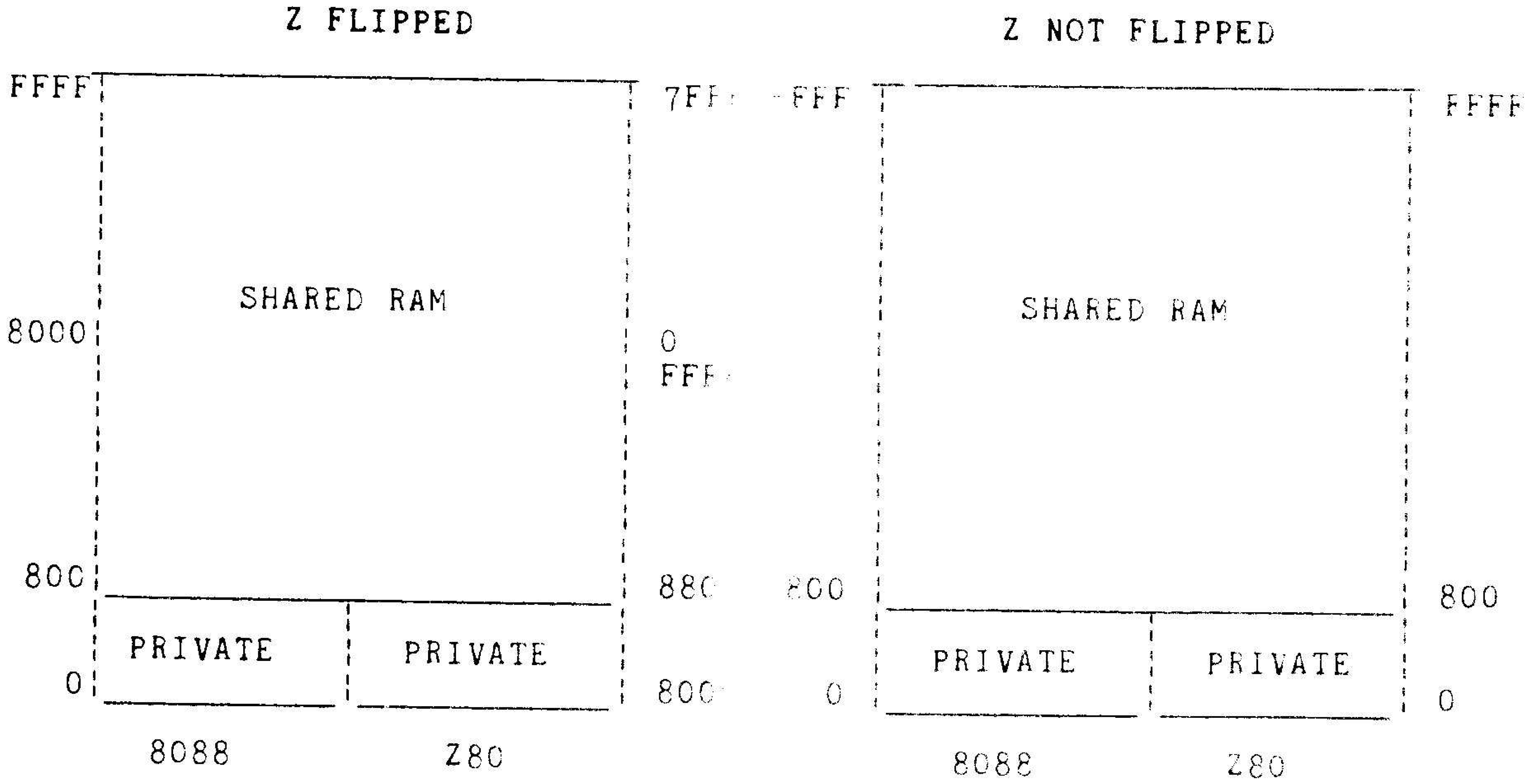


Figure 6. Z80A Memory Map

3.1.5.6 Z80A Cycle Time - The clock time on the Z80A is approximately 250 ns. Unshared memory accesses have no wait states. Shared memory accesses have wait states on M1 cycles and for cycles in which there is contention between devices accessing the shared RAM. Contention exists because of refresh cycles and 8088 cycles.

3.1.5.7 Z80A Interrupts - The only interrupts are interprocessor interrupts from the 8088 CPU. The vector placed on the bus is F7 (hex) which causes a RST 30 instruction to be executed in interrupt mode 0.

3.1.5.8 Floppy Controller Module - The floppy controller module is not optional. It is a separate module that connects to the mother board via J7. The interface is designed to control up to four 5-1/4 inch platters with one or two surfaces.
The controller supports soft-sectored double-density diskettes using a PLL circuit. Single- or double-sided drives are supported. The interface adheres to drive capability and signal definition of the ANSI standard interface for mini-floppy drives.

The floppy controller block diagram is shown in Figure 7.

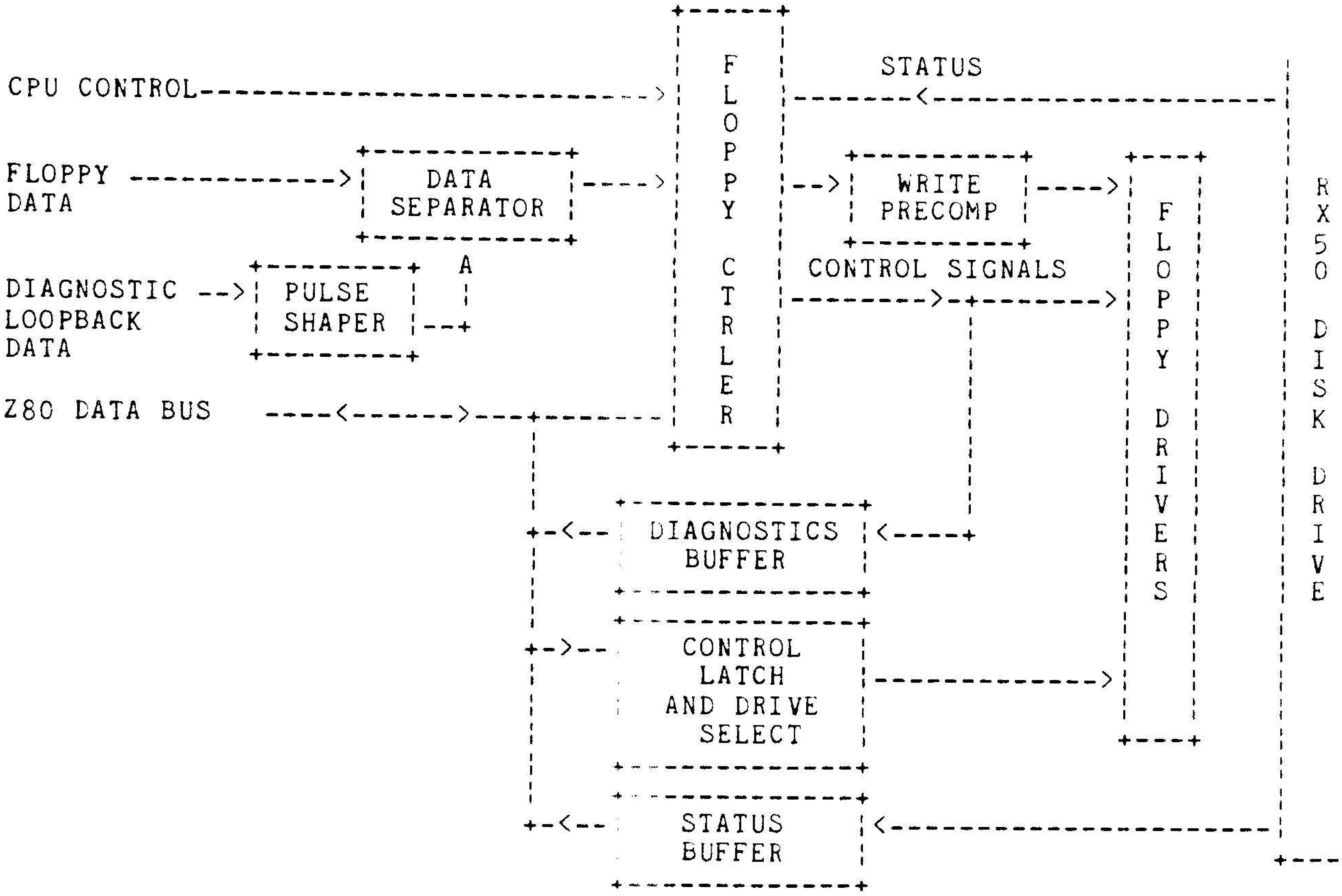


Figure 7. Floppy Controller Block Diagram

3.1.5.8.1 Floppy Disk Controller Registers: Z80A -

1. **Command Register (Write Only) (Port Address 60 Hex)**

   This 8-bit write-only register is loaded by the program with the command that is to be executed by the drive. A command summary follows.

Table 1. Command Summary

Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	v	r(1)	r(0)
I	Seek	0	0	0	1	h	v	r(1)	r(0)
I	Step	0	0	1	u	h	v	r(1)	r(0)
I	Step In	0	1	0	u	h	v	r(1)	r(0)
I	Step Out	0	1	1	u	h	v	r(1)	r(0)
II	Read Sector	1	0	0	m	0	e	0	0
II	Write Sector	1	0	1	m	0	e	0	a(0)
III	Read Address	1	1	0	0	0	e	0	0
IV	Force Interrupt	1	1	0	1	I(3)	I(2)	I(1)	I(0)

Note

Read Track and Write Track are not supported.

Flag Summary

Type I Commands

h = Head Load Flag (Bit 3)
v = Verify Flag (Bit 2)
r1,r0 = Stepping Motor Rate (Bits 1-0)
u = Update Flag (Bit 4)

Type II and III Commands

m = Multiple Record Flag (Bit 4)
a0 = Data Address Mark (Bit 0)
e = 30 msec delay

Type IV Commands

Ii = Interrupt Condition Flags

For more detailed information on the meaning and purpose of these bits, refer to the System Module Functional Specification.

Floppy Command Summary

This module accepts 9 commands for floppy disk control. (See Table 1 for a command summary.) Commands should only be loaded into the command register when the Busy status bit is off. The one exception is the Force Interrupt command. The Busy status bit is set when a command is executed.

Type I Commands

Type I commands are for head positioning. The stepping rate of these commands are dictated by the drive. R1 = 0 and R0 = 0 (6 ms) is the recommended stepping rate for the RX50 drive.

The head load flag determines if the head is loaded at the beginning of the command. Otherwise, the head is loaded at the end of a command.

The verification flag allows a verification operation to take place on the destination track. The verification consists of reading the first encountered ID field off of the disk.

The track address of the ID field is compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete. If not valid, the Seek error status bit in the FDC is set.

The Step, Stepin, and Stepout commands contain an update flag for updating the track register when this bit is set after the step has been completed.

Type II Commands

The Type II commands are to read and write sectors to the disk. Prior to loading the Type II command into the Command register, the Sector register must be loaded with the desired sector number.

Upon receipt of the command, the Busy status bit is set. If the e flag is set (normal case), the head is loaded and the HLT signal is sampled after 30 ms; otherwise, no delay is incurred after a command.

The HLT does not become active until 500 ms after the head is loaded to allow the spindle motor to have time to accelerate. The FDC then attempts to find the ID field with the specified track and sector.

If the desired field is not found within five revolutions of the disk, the Record Not Found status bit is set. Otherwise, the command is executed by the FDC generating Data Requests (DRQ) for servicing the data register.

Each of the Type II commands contain an m flag which determines if multiple sectors are to be read or written depending on the command. When set, multiple sectors are read or written with the sector register internally updated for address verification on the next track.

The FDC continues to do the transfers until the sector register exceeds the number of sectors on the track or until a force interrupt command is loaded into the command register.

Note

> If the command is not terminated by software, the 1793 continues looking for five index pulses after the last sector on the disk has been read or written.

If the Sector register exceeds the number of sectors on the track, the Record Not Found Status bit is set. When the head is loaded, the Busy status bit is set, and when an ID field is encountered that has the correct track, sector, side numbers and correct CRC, the data field is presented to the computer (read) or presented by the computer (write).

At the end of the Read operation, the type of Data Address Mark encountered is recorded in the Status register (Bit 5). On a Write operation, the a0 flag (Bit 0) determines the type of Data Address Mark to be written onto the disk. If set, a deleted data mark is written else a data mark is written.

Type III Commands

The Read Address command is to read in the six bytes of the ID field (track number, side number, sector address, sector length, and two bytes of CRC).

Type IV Command

This command is to terminate an operation upon the specified condition in Bits 3-0. See Table 1, Command Summary, for descriptions of the termination conditions.

Type I Command Bit Description

1. **Bit 0,1 - Stepping Rate Bits** - These bits control the rate at which the stepping pulses are sent to the drive. Check the specifications for the drive in use to determine the drive's proper step rate. See the table above for stepping rate breakdown.

2. **Bit 2 - Track Verify Bit** - This bit determines if there is a verification operation to take place on the destination track. During verification, the head is loaded and after a 30-ms delay, the HLT input is sampled. After a 500-ms motor start up time, the HLT input becomes active. When HLT is true, the first ID field is read off the disk. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete and an interrupt is generated. If not valid, the seek error status is set.

3. **Bit 3 - Head Load Flag** - This bit determines if the head is to be loaded at the beginning of a command. If the head is loaded then the head remains loaded until either the FDC receives a command that specifically disengages the head or 15 revolutions of the disk have passed with the busy bit = 0.

4. **Bit 4 - Update Bit (Step Commands)** - When set, the track register is updated by one for each step, otherwise the track register is not affected.

5. **Bits 5-7** - Determine the command to be executed.

Type II Commands Bit Description

1. **Bit 0 - Data Address Mark Bit** - When set upon a write sector command, this bit defines a Data Mark (0FBH) to be written on the disk. If the bit is not set then a Deleted Data Mark (0F8H) is written onto the disk. When writing valid data on the disk this bit should be set.

2. **Bit 1** - Always 0.

3. **Bit 2 - 30 Millisecond Delay Bit** - When set during a command, there is a 30-ms delay before reading begins. For maximum controller through-put, this bit should be 0. It should be set if the last command was a seek or new drive select.

4. **Bit 3** - Always 0.

5. **Bit 4** - Multiple Sector Bit - When set, this bit allows multiple sectors to be transferred.

6. Bits 5-7 - Determine the command to be executed.

Type III Command Bit Description

1. **Bits 0,1** - Always set to 0.

2. Bit 2 - Same as Bit 2 for Type II commands.

3. **Bits 3-7** - Determine the command to be executed.

Type IV Command Bit Description

This command can be loaded into the register at any time. If there is a current command under execution, the command is terminated. See Table 1 for a description of conditions upon which the command is terminated.

2. Status Register (Read Only) (Port Address 60 Hex)

This read only register also resides at the same address as the command register. It contains the 8-bit status resulting from the completion of a command. A description of the status bits follows.

Type I Status Bit Description

```
7   6   5   4   3   2   1   0
|   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |__ Busy
|   |   |   |   |   |   |______ Index
|   |   |   |   |   |__________ Track 0
|   |   |   |   |______________ ID Field CRC Error
|   |   |   |__________________ Seek Error
|   |   |______________________ Head Loaded
|   |__________________________ Write Protect
|______________________________ Not Ready
```

1. **Bit 0 - Busy Bit** - When this bit is true (1), the FDC is currently executing a command. Only a Type IV command can be issued when this condition exists.

2. **Bit 1 - Index Bit** - When this bit is true (1), the index pulse is currently occurring.

3. **Bit 2 - Track 0 Bit** - When this bit is true (1), the read/write head is currently positioned at track 0.

4. **Bit 3 - ID Field CRC Error Bit** - When true, this means that there was a CRC error of the ID field.

5. **Bit 4 - Seek Error Bit** - When true, a seek error was encountered meaning that the destination track address was not found.

6. **Bit 5 - Head Loaded Bit** - This bit reflects the current status of the head. When set, the head is loaded and the HLT input is asserted.

7. **Bit 6 - Write Protect Bit** - When set, the bit means that the current disk is write protected. An attempt to write a sector generates an interrupt if the device interrupt enable bit is set.

8. **Bit 7 - Not Ready Bit** - When set, the bit indicates that the drive is not ready. This could mean that the drive is not up to speed, the disk is in upside down, or the door is open. This bit must be clear before any commands are issued to the FDC.

Type II Read Sector Status Bit Description

```
7   6   5   4   3   2   1   0
:   :   :   :   :   :   :   :
:   :   :   :   :   :   :   '__ Busy
:   :   :   :   :   :   '______ Data Request
:   :   :   :   :   '__________ Lost Data
:   :   :   :   '______________ ID/Data Field CRC Error
:   :   :   '__________________ Record Not Found Error
:   :   '______________________ Record Type
:   '__________________________ 0
'______________________________ Not Ready
```

1. **Bit 0 - Busy Bit** - Same as Type I status.

2. **Bit 1 - Data Request Bit** - This bit means that the data register is full and it is waiting for the CPU to read the register.

3. **Bit 2 - Lost Data Bit** - When set, it means that the data register had not been serviced within 27.0 microseconds and the data in the data register is not valid.

4. **Bit 3 - ID/Data Field CRC Error Bit** - When set, an error is found in one or more ID fields or the data field. This bit is reset when updated.

5. **Bit 4 - Record Not Found Error Bit** - When equal to one, this bit means that a Data Address Mark was not found within 43 bytes of the last ID field CRC byte or it can indicate that the desired track, sector or side was not found.

6. **Bit 5 - Record Type Bit** - This bit reflects the type of Data Mark that was encountered during the read. When set a Deleted Data Mark was found. If clear, a Data Mark was encountered.

7. **Bit 6** - Always set to 0.

8. **Bit 7 - Not Ready Bit** - Same as Type I Not Ready Status Bit.

Type II Write Sector Status Bit Description

```
7   6   5   4   3   2   1   0
|   |   |   |   |   |   |   |
|   |   |   |   |   |   |   '__ Busy
|   |   |   |   |   |   '______ Data Request
|   |   |   |   |   '__________ Lost Data
|   |   |   |   '______________ CRC Error
|   |   |   '__________________ Record Not Found Error
|   |   '______________________ Write Fault
|   '__________________________ Write Protect
'______________________________ Not Ready
```

1. **Bit 0 - Busy Bit** - Same as Type I status Busy Bit.

2. **Bit 1 - Data Request Bit** - This bit means that the data register is empty and it is waiting for the CPU to write the register.

3. **Bit 2 - Lost Data Bit** - When set, it means that the data register had not been written within [illegible].0 microseconds and the data on the disk is not valid (zero bytes are substituted for data lost).

4. **Bit 3 - CRC Error Bit** - When set, this bit indicates an error in one or more ID fields. This bit is reset when updated.

5. **Bit 4 - Record Not Found Error Bit** - When equal to one, this bit indicates that the desired track, sector or side was not found.

6. **Bit 5 - Write Fault Bit** - Not implemented; should always be 0.

7. **Bit 6 - Write Protect Bit** - When this bit is set after a write command, then an attempt was made to write on a write protected disk.

8. **Bit 7 - Not Ready Bit** - Same as Type I Not Ready Status Bit

3. **Track Register (Port Address 61 Hex)**

This R/W 8-bit register holds the updated address of the current read/write head. It is incremented by one every time the head is stepped toward the spindle and decremented by one every time the head is stepped away from the spindle. The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations.

4. **Sector Register (Port Address 62 Hex)**

This read/write 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read and write operations.

5. Data Register (Port Address 63 Hex)

For a seek operation, this 8-bit read/write register holds the desired track position. During data transfers, this register is the data buffer for the disk.

3.1.5.8.2 General Control and Status Register Bit Description: Z80A -

This 8-bit register holds various control information for the drive as well as the module. The lowest four bits are read/write while the upper four bits are read only.

3.1.5.9 General Floppy Control Register: Z80A - The following write-only register (Port Address 40 Hex) holds control lines used to select drives and write delay pre-comp values for the floppies.

1. **Bits 0-1** - These bits control the selection of floppy drives. The binary values written to them (0 - 3) selects drive 0 through 3. Only 1 drive can be selected at a given time.
2. **Bit 2** - Diagnostic READY override bit. When set, this bit asserts DRIVE READY to the 1793.
3. **Bit 3** - This bit controls the MOTOR 0 ON bit. Turns on the motor on in the first drive unit.
4. **Bit 4** - This bit controls the MOTOR 1 ON bit. Turns on the motor on in the second drive unit.
5. **Bit 5** - This bit selects the SIDE of the disk to be accessed. For single-sided drives, this bit is always set to a 0 for side 0.
6. **Bits 6-7** - These binary bits are used to control the write delay pre-comp values. The following table lists the values for all tracks:

(TG43)	PC1	PC0	TRACK
0	0	0	0 - 9
0	0	0	10 - 19
0	0	0	20 - 29
0	0	0	30 - 39
1	0	0	40 - 49
1	0	0	50 - 60
1	0	1	61 - 69
1	0	1	70 - 79

3.1.5.9.1 Drive Select Light Operation - The drive select logic is set up so that none of the drives are enabled on power-up. When a disk is installed, the door is closed, the drive is selected and either HEAD LOAD or MOTOR ON is asserted. Then the drive active indicator light illuminates, the head loads and the motor turns on. Only one drive can be selected at a time.

The drive motors, on the other hand, are not gated with any signals. Each motor on signal can be activated independent of any other condition. The software never turns on both motors simultaneously. It is necessary to delay the start of the second selected motor for 500 ms after the start of the first motor.

CAUTION

> When both drive motors are off, a MOTOR ON override must not be generated for the unselected drive. Due to a hardware idiosyncrasy, this causes both drive motors to turn on simultaneously.

3.1.5.10 General Floppy Status Register: Z80A - The following read-only register (Port Address 40 Hex) holds the status of the RX50 drive lines coming from the 1793 FDC and going to the floppy drive.

1. Bits 0-1 - These bits read back the status of Bit 0 and 1 from the general floppy control register. They indicate which drives have been selected.
2. Bit 2 - This bit reflects the status of the TRACK GREATER THAN 43 signal from the 1793 going to the floppy.
3. Bit 3 - This bit reflects the status of MOTOR ON 0 line at the floppy connector. The signal, when read as 0, indicates that the MOTOR ON 0 bit is set.
4. Bit 4 - This bit reflects the status of MOTOR ON 1 line at the floppy connector. The signal, when read as 0, indicates that the MOTOR ON 1 bit is set.
5. Bit 5 - This bit reflects the status of the side select signal at the floppy connector.
6. Bit 6 - This bit reflects the status of the INTERRUPT REQUEST signal coming from the 1793. This is used to indicate that a status bit has changed.
7. Bit 7 - This bit reflects the status of the DATA REQUEST signal from the 1793. Used to indicate that the 1793 has read data to be transferred or requires new write data.

3.1.5.10.1 Floppy Disk Controller Required Delays - The following list describes required delays from one operation to the next operation:

Operation	Next Operation	Delays Required (microseconds)
Write to Command Register	Read Busy Bit (status bit 0)	12
Write to Command Register	Read Status Bits [illegible]	28
Write to Any Register	Read from Different Register	0
Write to Track, Sector or Same Register	Read from Data Register	8
Write to Any Register	Write to Another Register	14
Interrupt Request	Read Status Register	4

3.1.5.10.2 Floppy Disk Motor Speed-up Detection - While writing to a sector on a disk, the opening or closing of the OTHER DRIVE'S door will cause a transient in the floppy spindle motor speed. This transient can make any sector being written at the time of the opening or closing to be not readable in all situations. The following procedure is recommended and is implemented in the BIOS of CP/M-86/80:

Just prior to writing a sector on the disk, the drive being written to is de-selected. The other drive in THE SAME RX50 disk assembly is then selected and the condition of the Ready bit is sampled. The disk being written to is then selected again and the write operation is performed.

After the sector has been completed, the same operation is performed; the disk drive being written to is de-selected and the sister drive is selected. Ready is again sampled. If the condition of this bit had changed from the previous sample taken, then the sector must be re-written.

3.1.5.10.3 Floppy Controller Head Load Timer Activation - The Head Load Timer can be fired only in the following circumstance: The Head Load Timer must not be already timing. This means that neither MOTOR ON bits (M0, M1) are active, nor is the HEAD LOAD bit (HLD). Upon the next occurance of any of these three bits, and the state of the drive is READY, then the Head Load Timer will be actuated. This timer puts a 500-ms delay prior to HLT going true.

3.1.6 Mother Board Physical Dimensions

The mother board is a modified quad module with the following connectors:

J1	Communications Connector	25-pin	D-male
J2	Printer Connector	25-pin	D-female
J3	Video/Keyboard Connector	15-pin	D-male
J4	Extended Comms Connector	40-pin	HEADER
J5	Extended Comms Connector	40-pin	HEADER
J6	Memory Option Connector	52-pin	HEADER
J7	Graphics Option Connector	40-pin	HEADER
J8	Power Connector	13-pin	
J9	Floppy Controller Pin	40-pin	
J10	A/B Floppy Board	34-pin	
J11	C/D Floppy Board	34-pin	

3.2 OPTION MODULES

The following option modules will be supported by the Rainbow system:

3.2.1 Memory Option

Description/Features - The memory option for the PC100 allows the user to upgrade the system with an additional 64K or 192K bytes of memory. Additionally, two 64K byte stacks can be added to the option for a total of 192K bytes on the option. Along with the 64K bytes already on the system module, a total of 256K bytes of available memory for the PC100 is possible.

The 64KB and 192KB variants use the same 50 class etch. The 64KB board is not user upgradable.

If installed, this memory is always available and never requires wait states (except when the memory cycle contends with a refresh cycle).

The option is equipped with parity generation and a parity error detect circuit to notify the 8088 CPU in the event of a memory error. If such an error occurs, the memory option interrupts the 8088 CPU through a non-maskable interrupt. At this point the firmware takes the proper action to notify the user.

3.2.2 Extended Communications Option - Description/Features

The extended communications option card is a major component of the PC100 system and is connected to the PC100 main module via standoffs. The purpose of the option is to add a second communications port to the PC100 with bit and byte synchronous capability. It also gives the PC100 a separate high-speed serial communications port to support clustering and the addition of a high-speed file server. It has two 40-pin connectors through which it plugs into the system.

The extended communications option functions in the following ways within the PC100:

1. By means of the 8237 DMA Controller, block transfers data bidirectionally between memory and the high-speed communications link (7201 shared MPSC) while maintaining full interrupt support. The transfer to memory is into the PC100's shared RAM only and not into optional memory.

2. Distinguishes bit protocols at a clock rate of 880 kHz by means of the 7201 MPSC.

3. Provides an optional bisync port (7201 MPSC) that is a subset of the PC100's communication port.

4. Provides two complete serial communications controllers in a single 7201 MPSC package to:

   a. Convert parallel data (from the processor) to serial data, as required by various protocols.

   b. Convert serial data streams of the protocols back to parallel data for the processor.

   c. Buffer incoming and outgoing data, allowing the processor time to respond.

   d. Insert and delete framing bits and characters.

   e. Calculate/check parity and check CRC error.

   f. Inform CPU what actions need to be taken and when.

   g. Interface with outside world over discrete modem control lines.

5. Uses a 7201-Bus Interface Controller to provide:

   a. Bus Control Logic (BCL), which determines the internal source or destination of data and control transfers between the MPSC and the processor bus.

   b. Interrupt Control Logic (ICL), which prioritizes internal input requests and places information on the data bus during an Interrupt Acknowledge cycle (provided the MPSC vectored interrupt feature has been enabled)

   c. DMA Control Logic (DMACL), which enables the MPSC to make a data transfer without interrupting the processor. DMACL accepts service requests (if they are prioritized) and, like ICL (in b above), places information on the data bus at appropriate times. DMACL also accepts information from the data bus. When enabling the MPSC, DMACL activates an external controller to move data directly from the MPSC to memory or vice versa.

d. Clock and Reset Logic (C&RL), which controls timing states in the MPSC and is (usually) connected to the processor clock.

The extended communications option consists of the following main components mounted on a printed circuit board:

1. A 5 MHz 8237 Direct Memory Access Controller (DMAC).
2. A 7201 Multi-Protocol Serial Controller (MPSC) with the following features:

   a. A high-speed synchronous serial communications port with external clocks and RS422 differential drive capability.

   b. A general-purpose synchronous serial communications port, with RS423 drive capability, capable of supporting bisync modes.

Refer to the Extended Communications Option Functional Specification for further information.

3.2.2.1 Reset Sequence For Extended Communications. - The firmware will perform the following RESET function on the Extended Communications option upon power up, and any time that it has to handle an interrupt from the Extended Communications option: A write to 8088 port 27H will reset the option.

3.2.3 Graphics Option - Description/Features

The Graphics option is a bit mapped color graphics option which resides on a daughter board inside the Rainbow system box, and attaches to the Rainbow system board via a 40-pin connector, J7. The Graphics option will emulate VT240 functionality in both graphics and text handling. This includes but is not limited to the funcionality of the VT100, VT102, and VT125.

The Rainbow system with the color graphics option can operate in one of two modes, text only or graphics/text. In text only (VT100 text mode), the graphics option video will be deselected. During this time, the DC11 and DC12 on the system board will be responsible for providing signals to the monitor. During Graphics/text mode, the option will be selected.

3.2.3.1 **Features** - The Graphics option for Rainbow will support the following features:

a. Low resolution mode - 240 X 400 pixels X 4 planes.
b. High resolution mode - 240 X 800 pixels X 2 planes.
c. 16 simultaneous colors from a pallet of 4096.
d. 9600 baud character throughput (HARDWARE ONLY)
e. Smooth and jump split screen scrolling

4.0 RX50 DRIVE

4.1 GENERAL DESCRIPTION

The RX50 subsystem is a 5-1/4-inch flexible diskette drive and a single board controller which enables the PC100 to store or retrieve information on one side of each front-loaded diskette. Each diskette can contain up to 409,600 8-bit bytes (formatted), allowing a total of 819,200 bytes of storage per device.

4.2 DRIVE CHARACTERISTICS

No. of recorded surfaces	2
No. of diskettes/drive	2
No. of tracks/surface	80
No. of sectors/track	10
No. of bytes/sector	512
No. of bits/byte	8
Capacity (formatted)	
per drive	819,200 bytes
per surface	409,600 bytes
per track	5,120 bytes
Access Time, track to track	6 ms, one track
head load time, including settle time	30 ms. max
rotational latency	100 ms typical, 200 ms max.
random access	290 ms average
drive motor start	500 ms max.
Transfer rate	250K bytes/sec (average)
Disk rotation	300 RPM + 1% , -
Size	5.75 in. wide x 3.25 in. high x 8.5 in. deep
Weight	3.8 pounds

4.3 TRACK FORMAT

Each of the tracks is formatted as described below. Each data field is made up of 512 8-bit bytes, with a total of 10 data fields or sectors numbered 01 through 0A (hex) on each track. The following is a description of the track fields.

Description	No. of Bytes	Contents (HEX)
Pre ID gap	47	4E
ID Fields		
Sync	8	00
Mark	3	A1**
Header IDAM	1	FE
Track Address	1	Track no. (00-4F)
Side Number	1	00
Sector Address	1	Sector n. (01-0A)
Bytes/sector code	1	02
CRC	1	Calculated header CRC code
Pose ID gap	22	4E
Data Fields		
Sync	12	00
Mark	3	A1**
Data DAM	1	FB
Data	512	2CH
CRC	2	Calculated data CRC code
Post amble	1	00
Pre-index gap	*70	4E

* This field is written once pe track until an index field is encountered.

** The clock bit is missing between bits 4 and 5.

Fields modified by a WRITE operation are:

1. The DATA SYNC field
2. The DATA MARK field
3. The DATA field
4. The DATA CRC field
5. The POST AMBLE field

4.4 HEADER FORMAT

The diskettes are pre-formatted with header data. The header data fields cannot be modified or re-written by the system. The header field is made up of seven 8-bit bytes as follows:

Byte 1: ID Address Mark (IDAM). FE (hex). This byte coupled with the ID SYNC FIELD and MARK field is decoded by the controller to identify the start of a header.

Byte 2: Track Address. This is the absolute binary track address (00 to 4F hex). Each sector contains track address information to identify its radial position on 1 of 80 separate tracks.

Byte 3: Zeros.

Byte 4: Sector Address. This is the absolute binary sector address (01 to 0A hex). Each sector contains address information to identify its circumferential position on a track. There is no sector 00.

Byte 5: Sector Length 02 hex. This byte specifies the number of bytes contained in one sector. The RX50 drive is formatted with 512 bytes per sector.

Byte 6,7: These two bytes represent the cyclical redundancy check characters that are calculated from the first five header bytes.

5.0 PC100 FIRMWARE

6.0 PRODUCT GOALS

The PC100 firmware includes two variations of VT102 emulation: "terminal" mode and "console" mode. "Terminal" mode enables PC100 to act like a VT102 connected to a host computer via the communications port. The "console" mode enables PC100 to act like a VT102 (without printer port and using FDX data leads only as a protocol) when running programs on the PC100.

The firmware provides services to a "user" for console-out, console-in, console-in-status, enable/disable cursor, line-at-a-time screen data transfers, initialize interrupt vectors, return clock rate, 16-bit "key data", and keyboard LED control. Communications and printer port drivers are supplied the operating system in console mode.

The firmware also provides self-test diagnostics and a minimal bootstrap loader.

6.1 GOALS

The PC100 VT102 emulation runs a firmware program using the 8088 processor and looks to the user like a VT102. It provides subfunctions in modules usable to other programs. These other programs need to be able to execute similar functions. The VT102 emulation processes incoming character strings in the same manner as a VT102. The VT102 emulation also returns characters to the host in a manner similar to that of VT102 given the same SET-UP environment. Differences between VT102 and PC100 emulation are listed below.

VT52 emulation within the VT102 emulator performs as a VT102 (i.e. VT102 emulation of VT52 includes most VT102 functions such as 132 columns, auto-wrap, split screen, double high, double wide, etc.). The basis for VT102 functionality is the VT102 engineering specification REV A (SP VT102-0-02 A) dated 1-Aug-81.

6.1.1 Functional Anomalies

The following is a list of deviations from VT102 functionality, variances with TIA (terminals interface architecture), and other features of the firmware.

1. When printing from the screen in terminal mode and encountering a "blob" character, the VT102 sends ASCII "SUB" to the printer. The PC100 sends the VT100 line-drawing graphics character "blob", bracketed by the appropriate character set selection escape sequences, if required. Also, PC100 assumes the printer is capable of properly receiving 8-bit DEC STD 169 characters.

2. If keyboard is locked, break key does not function. This has been fixed in the 1/18 ROM set. All "Break Key" functions work with keyboard locked, but they also cause the keyboard to unlock.

3. Break Key and its associated control and shift functions do not auto-repeat, as in a VT102.

4. A backspace received when beyond column 127 acts like a carriage return. This has been fixed in the 1/18 ROM set.

5. At the completion of a "print cursor line" operation, PC100 sends the escape string to restore the printer's G0 character set in between the terminating carriage return and line feed. VT102 sends it after the line feed.

6. If a key is auto-repeating and the control key is then pressed, any resulting control character also auto-repeats. This has been fixed in the 1/18 ROM set.

7. Locking and unlocking the keyboard while a key is auto-repeating, or attempting to, has no effect. This has been partially fixed in the 1/18 ROM set. Locking the keyboard does stop an auto-repeat, but unlocking the keyboard does not re-start auto-repeat unless the original key is still the one held down. Any new key must be pressed after the keyboard is unlocked, in order to have it auto-repeat.

8. Escape sequences that move the cursor down and right cause incorrect cursor locations (it disappears) if the parameter plus the current location add up to 0 in an 8-bit value. The terminator and pointer of a screen line can be modified as a result of subsequent actions. This has been fixed in the 1/18 ROM set.

9. When the SET-UP key is pressed to enter SET-UP mode in the PC100, the key-holding buffer is cleared, which causes any unserviced keys to be lost, and SET-UP is immediately honored.

10. When the keyboard buffer fills up, the PC100 ignores further entries and sounds the bell. It does not light the keyboard-locked LED as does the VT102. This has been fixed in the 1/18 ROM set.

11. The printer port baud rate selection and the communications port external clock selection both reside in the same write-only 8088 port. Selecting communications port external clocks can make the printer port baud rate incorrect and selecting printer port baud rates in SET-UP will de-select external clocks for communication. Also, the break control bit for the 7201 is in the same write-only register as the number-of-data-bits. The firmware can read the NVM and set this properly for use with terminal mode. An application cannot do this.

12. PC100 keeps two separate "graphics mode" flags; one for VT52 mode and one for ANSI mode. VT102 keeps only one flag, which applies to both. In the 1/18 ROM set, selecting ANSI or VT52 mode also initializes character sets and selection to non-graphics.

13. PC100 maintains wrap-pending flag unconditionally, and tests it conditionally. VT102 maintains the flag conditionally and tests it unconditionally. This affects where the next character goes when the auto-wrap mode is changed while the cursor is in the "line-filled" position.

14. In PC100, the escape sequences to select alternate ROM and alternate ROM special graphics are parsed but ignored.

15. NVM defaults are not the same as VT102 for the printer port.

16. PC100 executes C1 control codes for index, next line, horizontal tab set, reverse index, single shift 2, single shift 3, and control sequence introducer. Reception of any C1 control code (or 8-bit graphics character) will abort an escape sequence in process (CSI restarts an escape sequence). In the 1/18 ROM set, 8-bit graphic characters will be displayed if received during an escape sequence and will not abort the parsing.

17. PC100 always sets insertion/replacement mode to replacement before saving into NVM.

18. PC100 requires use of the shift key for some of the keyboard-entered control codes. This is due to the uncertainty of character location on various foreign-language keyboards.

19. The PC100 accepts and acts on 8-bit character codes; the VT102 always strips the 8th bit. If 8-bit codes are received in VT52 mode, they will be handled the same as in ANSI mode.

20. Shift out (CTRL/N) and shift in (CTRL/O) in VT52 mode will abort VT52 "graphics" operation if the character set selected is not the "graphics" set.

21. In console mode, with default character set for UK, G2 and G3 are initialized to UK, but G0 and G1 are initialized to U.S. The operator must enter SET-UP and toggle the US/UK default selection to get G0 and G1 into UK. This has been fixed in the 1/18 ROM set to use the correct default character set.

22. Terminal mode print functions are implemented via the "print screen" key on the PC100. VT102 uses the keypad "enter" key. PC100 "print screen" is equivalent to VT102 <shift/enter> and PC100 <control/print screen> is equivalent to VT102 <control/enter>.

23. When hold-screen is in effect, all attempts to "receive" a character will hang until hold-screen is removed. This includes selections from the opening menu, console out requests, data moves to screen display, and terminal mode character reception. In terminal mode, the receive buffer will continue to fill, but will not be emptied. When "full", it will automatically send XOFF if enabled in SET-UP; otherwise, data will be lost if the host does not stop sending. In the 1/18 ROM set, the diagnostic routines in ROM have been given a separate entry to the display process that bypasses the "Hold Screen" test.

24. The PC100 will parse but ignore the escape sequences to set G0 and G1 to the alternate ROM and alternate ROM special graphics (ESC (1 , ESC (2 , ESC) 1 , ESC) 2). It will also parse but ignore the escape sequences to run self-tests (ESC [2 ; Pn y) and the LED control (ESC [Pn q). Also, the device status report request (ESC [5 n) will always cause the ready, no malfunctions reply (ESC [0 n).

25. Serial line SET-UP selections of 7-bit mark and space actually use the 7201 in 8-bit no-parity mode. The mark/space aspect is handled by the firmware drivers in terminal mode. In console mode, the operating system drivers do not make this distinction, and set-ups 7M and 7S are the same as 8N in console mode.

26. The HOLD-SCREEN key on the PC100 does not work the same as the NO SCROLL key on the VT102. On a VT102, it sends an XOFF/XON as it toggles back and forth, and CTRL/S and CTRL/Q typed from the keyboard can be used to get the same effect. In PC100, setting HOLD SCREEN does not necessarily cause an XOFF to be sent. It sets an internal flag that causes the "receive character" process to loop until the flag is cleared. This effectively "hangs" any console output (normal or direct) in console mode. In terminal mode, this "hang" causes the communication receive buffer to fill up until it reaches the high-water mark, at which point it will send an XOFF if enabled by SET-UP. After the HOLD SCREEN is removed, characters are removed from the receive buffer until the low-water mark is reached, which causes XON to be sent if enabled. As a result of this method of implementation, PC100 honors HOLD SCREEN even in "local"; VT102 does not.

27. PC100 resets CAPS LOCK to "lower case" any time the "S" (self test) selection is made from the opening menu.

28. The following keys generate escape sequences that end in characters that cause valid selections at opening menu time: cursor arrow keys will select drives to boot from and PF4 in the keypad will select self-test.

29. The PC100 in VT52 mode honors the origin mode setting; the VT102 in VT52 mode does not.

30. In PC100 escape sequences for erase in line and erase in display, only the first selective parameter is processed if more than one is sent.

31. In PC100, ESC c (reset to initial state) does not reset keypad and cursor keys to their normal modes.

32. In PC100, print screen while screen is "held" is deferred until after "hold" is removed and the character being "held" is processed.

33. In PC100 terminal mode, after using "hold-screen" on incoming data, the last character for display is being "held". Entering SET-UP, switching to local, and exiting from SET-UP does not clear the "hold" state or the character. When "hold" is finally removed, the character originally being "held" is displayed before any locally-generated characters.

34. In PC100, any noise on the printer port DTR line can cause an interrupt that will set a flag indicating a printer was once available.

35. In PC100, cursor key mode and keypad mode are independent. This agrees with the TIA specification, but not the VT102. In the VT102, the cursor keys only send application codes if both cursor and keypad modes are set to "application".

36. In PC100, the TAB character always clears the wrap-pending flag. This agrees with the TIA specification, but not the VT102. As a result, auto-wrap will not be the same if TAB is the 81st character in an 80-character line. Character 82 will not wrap, but character 83 will. In VT102, character 82 will wrap.

37. In PC100 terminal mode, the second XOFF is sent at "buffer-full". In VT102, the second XOFF is sent 12 characters before "buffer-full". Also, the PC100 buffer is 255 characters in size; the VT102 is 128.

38. PC100 allows a tab stop in the first column; VT102 does not.

39. Function keys are not ignored when entering the answerback message, and they produce unpredictable results.

40. PC100 aborts escape sequence parsing when it finds an intermediate character, causing all following characters to be displayed. VT102 aborts the sequence, but continues parsing until it finds a final character, so the intervening part of the escape sequence does not display.

41. Because of differences in implementation and timing, the PC100 and VT102 can have different transient appearances where the cursor is concerned. For example, the cursor may appear momentarily and/or in different locations when the same data is sent to both for display.

42. In terminal mode, local, printer controller mode does not send keyboard characters to the printer.

43. A single-shift 2 or 3 is not preserved across escape sequences. If an intervening escape sequence occurs, the following graphic character set is not affected. This is also true for intervening control sequences and 8-bit control codes.

44. Any printer-related escape sequence (ANSI or VT52) or keyboard entry isignored if the printer DTR signal is not asserted at tne time. After printing begins, the state of the DTR from the printer is ignored.

45. Switching auto-xon/xoff after establishing contact can cause the "Terminal" to hang under the right conditions. Typing an xon (CTRL/Q) in these cases should clear the hung state.

6.2 PERFORMANCE

The performance of the VT102 emulation is at least equal to that of the actual VT102. Using pure text for data in jump scroll mode, the VT102 emulation operates at 9600 baud unrestrained as a terminal. It is a goal for it to operate at 38.4K baud as a console.

6.3 NON-GOALS

The non-goals for this program are:

1. Emulation of bugs in the VT102 software.
2. SET-UP mode identical to that of the VT102.
3. The VT102 firmware excludes all VT131 hooks. There is no support for editing, block mode transmit, protected fields, option ROM linkage, etc.
4. All printer baud rates of VT102 supported.

6.4 GENERAL

The firmware of the PC-100 provides the following services:

1. Power-up initialization of hardware
2. Self-test diagnostics
3. VT102 emulation - available in "terminal" and "console" modes
4. Image of Z80 RAM space to be loaded
5. Boot loader to read track 0, sector 1 of floppy

6. Opening menu selection process
7. Automatic shut-off of screen display after 30 minutes of non-use, and restoration of display on first activity (any keyboard key or received character).

The firmware is organized such that the VT102 emulation primitives form the "console" functionality for use by "applications" through the interface layer. When in "terminal" mode, a background loop is entered which calls on the "console" primitives and adds the necessary functionality to provide full "terminal" mode.

An interface layer is placed over the "console" primitives to provide an "application" with means of accessing those primitives.

Note

> In "console" mode there is no support provided for the printer or the communication ports. This hardware (7201) must be controlled directly by the operating system.

For "applications" that need more immediate control of the hardware, services are provided to obtain "raw" key information, enable/disable cursor, and transfer data directly to screen RAM. The interface between the "application" and the firmware is implemented using a software interrupt, with arguments passed and returned in CPU registers.

This leads to a layered structure as diagramed below. From the firmware view point, the operating system in this example is an "application". It can actually be anything, including another firmware routine.

All entries to firmware routines from external processes are via a software interrupt. This makes the interface release-independent because ROM code loads the proper vectors during initialization.

8088 side

```
             |--------|---------|--------------|
             |        |  NORMAL |              |
             | SU     |   USER  |              |
             |     |----------------|    SU    |
             |     |   OPERATING    |          |
             |     |    SYSTEM      |          |
*************************************          |
*   VT102    *    INTERFACE         *          |
* 'TERMINAL' *      LAYER        X  *          |
*************************************          |
*     VT102 'CONSOLE' PRIMITIVES    *          |
*************************************---|------|
| VIDEO | KBD | PRINTER |     COMM      |  OPT |
| HDWR  |     |  PORT   |     PORT      | HDWR |
|----------------------------------------------|
```

SU indicates sophisticated user; ***** indicates located in ROM

6.4.1 Text Strings

All text strings are located in a single section of the code space so they may be changed with no effect on ROM code (foreign languages). The text strings are accessed by a table of pointers that remains in a fixed location so routines do not need to know the exact text locations. This table and its associated text strings are in one ROM to minimize changes required for other language versions. The keyboard key-to-code mapping tables are also in this same ROM.

The total amount of ROM space allocated to text strings cannot be increased. There is no restriction on individual string size, only total bytes used and order of messages.

6.4.2 Character Sets

As with the VT102, the VT102 emulation supports the following character sets: UK, USASCII, Special graphics.

The character generator ROM also contains the displayable right half of the DEC multinational character set (shown as the DEC supplemental graphic set in DEC STD 169). These characters are accessed by direct writing of data into the screen via interrupt 40 or by reception of the corresponding 8-bit code. The character generator ROM also contains space for 31 additional displayable characters to be determined.

The "console" VT102 accepts 8-bit character codes to display the alternate characters. The "terminal" VT102 accepts 7- or 8-bit codes (depending on communication port parameters) and displays characters based on character set mapping through escape sequences. The "console" also works with escape sequence character set mapping and 7-bit characters.

The PC100 also accepts 8-bit C1 control codes for index, next line, horizontal tab set, reverse index, single shift 2, single shift 3, and control sequence introducer. Any C1 control code will abort an escape sequence in process, and CSI will re-start it.

Table 2 lists the characters and corresponding codes available in the PC100 for display. The codes are actually a part of the address for the bit map of that character in the character generator ROM. They are the upper eight bits of the address; the lower four bits select the proper scan line within the character. There are six unused "scan lines" at the end of each character (uses 10 out of 16).

Note

All undefined and reserved characters are indicated by an upside-down question mark.

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
00	00	ALL	NULL,IGNORED ON RCV, DISPLAYS A BLANK
	5F	SPECL GRAPHICS	BLANK
01	60	SPECL GRAPHICS	DIAMOND
02	61	SPECL GRAPHICS	CHECKERBOARD (BLOB)
03	62	SPECL GRAPHICS	HT (HORIZONTAL TAB)
04	63	SPECL GRAPHICS	FF (FORM FEED)
05	64	SPECL GRAPHICS	CR (CARRIAGE RETURN)
06	65	SPECL GRAPHICS	LF (LINE FEED)
07	66	SPECL GRAPHICS	DEGREE SYMBOL
08	67	SPECL GRAPHICS	PLUS/MINUS SIGN
09	68	SPECL GRAPHICS	NL (NEW LINE)
0A	69	SPECL GRAPHICS	VT (VERTICAL TAB)
0B	6A	SPECL GRAPHICS	LOWER RIGHT CORNER
0C	6B	SPECL GRAPHICS	UPPER RIGHT CORNER
CD	6C	SPECL GRAPHICS	UPPER LEFT CORNER
0E	6D	SPECL GRAPHICS	LOWER LEFT CORNER
0F	6E	SPECL GRAPHICS	CROSSING LINES
10	6F	SPECL GRAPHICS	HORIZONTAL LINE, SCAN 1
11	70	SPECL GRAPHICS	HORIZONTAL LINE, SCAN 3
12	71	SPECL GRAPHICS	HORIZONTAL LINE, SCAN 5
13	72	SPECL GRAPHICS	HORIZONTAL LINE, SCAN 7
14	73	SPECL GRAPHICS	HORIZONTAL LINE, SCAN 9
15	74	SPECL GRAPHICS	LEFT 'T'
16	75	SPECL GRAPHICS	RIGHT 'T'
17	76	SPECL GRAPHICS	BOTTOM 'T'
18	77	SPECL GRAPHICS	TOP 'T'
19	78	SPECL GRAPHICS	VERTICAL BAR
1A	79	SPECL GRAPHICS	LESS-THAN OR EQUAL
1B	7A	SPECL GRAPHICS	GREATER-THAN OR EQUAL
1C	7B	SPECL GRAPHICS	PI SYMBOL
1D	7C	SPECL GRAPHICS	NOT EQUAL SIGN
1E	7D	SPECL GRAPHICS	U.K. POUND STERLING SIGN
	23	UK	
1F	7E	SPECL GRAPHICS	CENTERED DOT
20	20	UK/USASCII	SPACE
		SPECL GRAPHICS	
21	21	UK/USASCII	EXCLAMATION POINT
		SPECL GRAPHICS	
22	22	UK/USASCII	DOUBLE QUOTES
		SPECL GRAPHICS	
23	23	USASCII	NUMBER SIGN (POUND SIGN)
		SPECL GRAPHICS	
24	24	UK/USASCII	DOLLAR SIGN
		SPECL GRAPHICS	

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
25	25	UK/USASCII SPECL GRAPHICS	PER-CENT SIGN
26	26	UK/USASCII SPECL GRAPHICS	AMPERSAND SIGN
27	27	UK/USASCII SPECL GRAPHICS	SINGLE QUOTE
28	28	UK/USASCII SPECL GRAPHICS	LEFT PARENTHESES
29	29	UK/USASCII SPECL GRAPHICS	RIGHT PARENTHESES
2A	2A	UK/USASCII SPECL GRAPHICS	ASTERISK SIGN
2B	2B	UK/USASCII SPECL GRAPHICS	PLUS SIGN
2C	2C	UK/USASCII SPECL GRAPHICS	COMMA
2D	2D	UK/USASCII SPECL GRAPHICS	DASH (MINUS SIGN)
2E	2E	UK/USASCII SPECL GRAPHICS	PERIOD
2F	2F	UK/USASCII SPECL GRAPHICS	SLASH (FRACTION BAR)
30	30	UK/USASCII SPECL GRAPHICS	NUMERAL 0
31	31	UK/USASCII SPECL GRAPHICS	NUMERAL 1
32	32	UK/USASCII SPECL GRAPHICS	NUMERAL 2
33	33	UK/USASCII SPECL GRAPHICS	NUMERAL 3
34	34	UK/USASCII SPECL GRAPHICS	NUMERAL 4
35	35	UK/USASCII SPECL GRAPHICS	NUMERAL 5
36	36	UK/USASCII SPECL GRAPHICS	NUMERAL 6
37	37	UK/USASCII SPECL GRAPHICS	NUMERAL 7
38	38	UK/USASCII SPECL GRAPHICS	NUMERAL 8
39	39	UK/USASCII SPECL GRAPHICS	NUMERAL 9
3A	3A	UK/USASCII SPECL GRAPHICS	COLON

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
3B	3B	UK/USASCII SPECL GRAPHICS	SEMI-COLON
3C	3C	UK/USASCII SPECL GRAPHICS	LEFT ANGLE BRACKET
3D	3D	UK/USASCII SPECL GRAPHICS	EQUALS SIGN
3E	3E	UK/USASCII SPECL GRAPHICS	RIGHT ANGLE BRACKET
3F	3F	UK/USASCII SPECL GRAPHICS	QUESTION MARK
40	40	UK/USASCII SPECL GRAPHICS	AT SIGN
41	41	UK/USASCII SPECL GRAPHICS	CAPITAL A
42	42	UK/USASCII SPECL GRAPHICS	CAPITAL B
43	43	UK/USASCII SPECL GRAPHICS	CAPITAL C
44	44	UK/USASCII SPECL GRAPHICS	CAPITAL D
45	45	UK/USASCII SPECL GRAPHICS	CAPITAL E
46	46	UK/USASCII SPECL GRAPHICS	CAPITAL F
47	47	UK/USASCII SPECL GRAPHICS	CAPITAL G
48	48	UK/USASCII SPECL GRAPHICS	CAPITAL H
49	49	UK/USASCII SPECL GRAPHICS	CAPITAL I
4A	4A	UK/USASCII SPECL GRAPHICS	CAPITAL J
4B	4B	UK/USASCII SPECL GRAPHICS	CAPITAL K
4C	4C	UK/USASCII SPECL GRAPHICS	CAPITAL L
4D	4D	UK/USASCII SPECL GRAPHICS	CAPITAL M
4E	4E	UK/USASCII SPECL GRAPHICS	CAPITAL N
4F	4F	UK/USASCII SPECL GRAPHICS	CAPITAL O
50	50	UK/USASCII SPECL GRAPHICS	CAPITAL P

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
51	51	UK/USASCII SPECL GRAPHICS	CAPITAL Q
52	52	UK/USASCII SPECL GRAPHICS	CAPITAL R
53	53	UK/USASCII SPECL GRAPHICS	CAPITAL S
54	54	UK/USASCII SPECL GRAPHICS	CAPITAL T
55	55	UK/USASCII SPECL GRAPHICS	CAPITAL U
56	56	UK/USASCII SPECL GRAPHICS	CAPITAL V
57	57	UK/USASCII SPECL GRAPHICS	CAPITAL W
58	58	UK/USASCII SPECL GRAPHICS	CAPITAL X
59	59	UK/USASCII SPECL GRAPHICS	CAPITAL Y
5A	5A	UK/USASCII SPECL GRAPHICS	CAPITAL Z
5B	5B	UK/USASCII SPECL GRAPHICS	LEFT SQUARE BRACKETS
5C	5C	UK/USASCII SPECL GRAPHICS	BACK-SLASH
5D	5D	UK/USASCII SPECL GRAPHICS	RIGHT SQUARE BRACKETS
5E	5E	UK/USASCII SPECL GRAPHICS	CIRCUMFLEX
5F	5F	UK/USASCII SPECL GRAPHICS	UNDERLINE
60	60	UK/USASCII	ACCENT GRAVE
61	61	UK/USASCII	LOWER CASE A
62	62	UK/USASCII	LOWER CASE B
63	63	UK/USASCII	LOWER CASE C
64	64	UK/USASCII	LOWER CASE D
65	65	UK/USASCII	LOWER CASE E
66	66	UK/USASCII	LOWER CASE F
67	67	UK/USASCII	LOWER CASE G
68	68	UK/USASCII	LOWER CASE H
69	69	UK/USASCII	LOWER CASE I
6A	6A	UK/USASCII	LOWER CASE J
6B	6B	UK/USASCII	LOWER CASE K
6C	6C	UK/USASCII	LOWER CASE L
6D	6D	UK/USASCII	LOWER CASE M

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
6E	6E	UK/USASCII	LOWER CASE N
6F	6F	UK/USASCII	LOWER CASE O
70	70	UK/USASCII	LOWER CASE P
71	71	UK/USASCII	LOWER CASE Q
72	72	UK/USASCII	LOWER CASE R
73	73	UK/USASCII	LOWER CASE S
74	74	UK/USASCII	LOWER CASE T
75	75	UK/USASCII	LOWER CASE U
76	76	UK/USASCII	LOWER CASE V
77	77	UK/USASCII	LOWER CASE W
78	78	UK/USASCII	LOWER CASE X
79	79	UK/USASCII	LOWER CASE Y
7A	7A	UK/USASCII	LOWER CASE Z
7B	7B	UK/USASCII	LEFT BRACES
7C	7C	UK/USASCII	VERTICAL LINE (BROKEN)
7D	7D	UK/USASCII	RIGHT BRACES
7E	7E	UK/USASCII	TILDE
7F	7F	ALL	RESERVED FOR CHARACTER GENERATOR ROM CHECKSUM
80			DISPLAYS JUNK, SHOULD NOT BE USED UNFILLED RECTANGLE FOR 'AUTO-BLANKED CURSOR'
81			TO BE DETERMINED
82			TO BE DETERMINED
83			TO BE DETERMINED
84			TO BE DETERMINED
85			TO BE DETERMINED
86			TO BE DETERMINED
87			TO BE DETERMINED
88			TO BE DETERMINED
89			TO BE DETERMINED
8A			TO BE DETERMINED
8B			TO BE DETERMINED
8C			TO BE DETERMINED
8D			TO BE DETERMINED
8E			TO BE DETERMINED
8F			TO BE DETERMINED
90			TO BE DETERMINED
91			TO BE DETERMINED
92			TO BE DETERMINED
93			TO BE DETERMINED
94			TO BE DETERMINED
95			TO BE DETERMINED
96			TO BE DETERMINED

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
97			TO BE DETERMINED
98			TO BE DETERMINED
99			TO BE DETERMINED
9A			TO BE DETERMINED
9B			TO BE DETERMINED
9C			TO BE DETERMINED
9D			TO BE DETERMINED
9E			TO BE DETERMINED
9F			TO BE DETERMINED
A0			NOT USED
A1			INVERTED EXCLAMATION POINT
A2			CENT SIGN
A3			U.K. POUND STERLING SIGN
A4			RESERVED (DEC STD 169)
A5			YEN SIGN
A6			RESERVED (DEC STD 169)
A7			SECTION SIGN
A8			GENERAL CURRENCY SIGN
A9			COPYRIGHT SIGN
AA			FEMININE ORDINAL INDICATOR
AB			LEFT ANGLE QUOTATION MARKS
AC			RESERVED (DEC STD 169)
AD			RESERVED (DEC STD 169)
AE			RESERVED (DEC STD 169)
AF			RESERVED (DEC STD 169)
B0			DEGREE SIGN
B1			PLUS/MINUS SIGN
B2			SUPERSCRIPT 2
B3			SUPERSCRIPT 3
B4			RESERVED (DEC STD 169)
B5			MICRO SIGN
B6			PARAGRAPH SIGN, PILCROW
B7			MIDDLE DOT
B8			RESERVED (DEC STD 169)
B9			SUPERSCRIPT 1
BA			MASCULINE ORDINAL INDICATOR
BB			RIGHT ANGLE QUOTATION MARK
BC			FRACTION 1/4
BD			FRACTION 1/2
BE			RESERVED (DEC STD 169)
BF			INVERTED QUESTION MARK
C0			CAPITAL A WITH GRAVE ACCENT
C1			CAPITAL A WITH ACUTE ACCENT
C2			CAPITAL A WITH CIRCUMFLEX ACCENT

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
C3			CAPITAL A WITH TILDE
C4			CAPITAL A WITH UMLAUT
C5			CAPITAL A WITH RING
C6			CAPITAL AE DIPTHONG
C7			CAPITAL C WITH CEDILLA
C8			CAPITAL E WITH GRAVE ACCENT
C9			CAPITAL E WITH ACUTE ACCENT
CA			CAPITAL E WITH CIRCUMFLEX ACCENT
CB			CAPITAL E WITH UMLAUT
CC			CAPITAL I WITH GRAVE ACCENT
CD			CAPITAL I WITH ACUTE ACCENT
CE			CAPITAL I WITH CIRCUMFLEX ACCENT
CF			CAPITAL I WITH UMLAUT
D0			RESERVED (DEC STD 169)
D1			CAPITAL N WITH TILDE
D2			CAPITAL O WITH GRAVE ACCENT
D3			CAPITAL O WITH ACUTE ACCENT
D4			CAPITAL O WITH CIRCUMFLEX ACCENT
D5			CAPITAL O WITH TILDE
D6			CAPITAL O WITH UMLAUT
D7			CAPITAL OE DIPTHONG
D8			CAPITAL O WITH SLASH
D9			CAPITAL U WITH GRAVE ACCENT
DA			CAPITAL U WITH ACUTE ACCENT
DB			CAPITAL U WITH CIRCUMFLEX ACCENT
DC			CAPITAL U WITH UMLAUT
DD			CAPITAL Y WITH UMLAUT
DE			RESERVED (DEC STD 169)
DF			GERMAN SMALL SHARP S
E0			LOWER CASE A WITH GRAVE ACCENT
E1			LOWER CASE A WITH ACUTE ACCENT
E2			LOWER CASE A WITH CIRCUMFLEX ACCENT
E3			LOWER CASE A WITH TILDE
E4			LOWER CASE A WITH UMLAUT
E5			LOWER CASE A WITH RING
E6			LOWER CASE AE DIPTHONG
E7			LOWER CASE C WITH CEDILLA
E8			LOWER CASE E WITH GRAVE ACCENT
E9			LOWER CASE E WITH ACUTE ACCENT
EA			LOWER CASE E WITH CIRCUMFLEX ACCENT
EB			LOWER CASE E WITH UMLAUT
EC			LOWER CASE I WITH GRAVE ACCENT
ED			LOWER CASE I WITH ACUTE ACCENT
EE			LOWER CASE I WITH CIRCUMFLEX ACCENT

Table 2. Displayable Characters and Corresponding Codes

CHAR CODE IN RAM 8 BITS (HEX)	CHAR CODE RCVD 7 BITS	CHAR SET(DEFINES RULES FOR RCVD TO RAM TRANSLATE)	NAME OF CHARACTER
EF			LOWER CASE I WITH UMLAUT
F0			RESERVED (DEC STD 169)
F1			LOWER CASE N WITH TILDE
F2			LOWER CASE O WITH GRAVE ACCENT
F3			LOWER CASE O WITH ACUTE ACCENT
F4			LOWER CASE O WITH CIRCUMFLEX ACCENT
F5			LOWER CASE O WITH TILDE
F6			LOWER CASE O WITH UMLAUT
F7			LOWER CASE OE DIPTHONG
F8			LOWER CASE O WITH SLASH
F9			LOWER CASE U WITH GRAVE ACCENT
FA			LOWER CASE U WITH ACUTE ACCENT
FB			LOWER CASE U WITH CIRCUMFLEX ACCENT
FC			LOWER CASE U WITH UMLAUT
FD			LOWER CASE Y WITH UMLAUT
FE			RESERVED (DEC STD 169)
FF			NOT ALLOWED, THIS IS 'TERMINATION' CODE

6.5 START-UP/SHUT DOWN/RESET

6.5.1 Power-Up Initialization

This process initializes all the hardware, including any indicated EXPANSION RAM options and all the flags, pointers, etc. Power-up must also read in the contents of the NVM and configure itself accordingly. The NVM contains information on memory configuration for use by self-test diagnostics. It shows which 64K memory blocks are installed. The option installer must enter this information at the time of installation. There is a choice in the Set-Up that provides this "RAM Option Configuration" Set-Up service.

The NVM consists of two elements, the non-volatile storage part and a volatile shadow RAM part. A recall operation transfers the contents of the non-volatile storage part to the shadow RAM part. A store operation transfers the contents of the shadow RAM part into the non-volatile storage part, destroying any previous contents. Data can only be transferred to or from the CPU from the shadow RAM part, and only when the NVM is not either in the recall or store modes of operation.

A CRC is calculated and stored along with the shadow RAM data. This CRC is verified after any recall operation. If the CRC does not verify, the recovery procedure is:

1. A second recall is done.
2. If second recall is OK, continue as normal.
3. If second recall is also bad, it could be due to two reasons:
   a. first time ever used, contains random data
   b. bad NVM
4. Put defaults into shadow RAM, store into NVM, and display NVM ERROR, INITIALIZED TO DEFAULTS message and continue as normal.

6.5.2 Power-Off

No attempt to do anything special is made on power-off.

6.5.3 Hardware Resetting

The system resets similar to a VT100. Enter Set-Up mode and press the Ctrl key and the Set-Up key simultaneously. The resetting is accomplished by jumping to a separate location at the start of the self-test diagnostics. Entry at this point distinguishes it from a power-up start.

This assumes the system is still capable of entering Set-Up. If not, the only recovery is to cycle the power off and on.

CAUTION

Leaving interrupts disabled for 100 ms or more in the 8088 CPU causes the hardware failure detect circuitry to be activated.

6.5.4 RAM Parity Error

When the expansion RAM is installed, a parity error activates the NMI input. The NMI causes the message FAILURE, RAM OPTION, CONSULT YOUR USER'S GUIDE to be displayed on the screen and causes the bell to beep. No more options are allowed except to enter Set-Up and reset the system.

If an operating system needs to handle parity errors itself, it takes over the NMI interrupt vector.

6.6 MEMORY-MAPPED VIDEO ACCESS SERVICE

A "sophisticated user" accesses the screen/attribute RAM directly for fast data transfers.

Note

The character stored in the screen RAM by this process is actually a code (not necessarily ASCII). This code is bits 4 - 11 of the address in the character generator ROM for the first scan line of the bit pattern of that character. See subhead 6.4.2.

The screen display is a linked list and there are several related tables, flags, and pointers that must be retained. It is imperative, then, that the "sophisticated user" follow certain restrictions when directly accessing the screen/attribute RAM.

1. In order to guarantee a known starting condition and remove all effects of scrolling, double height, double width line, top and bottom margins, origin mode, and so on, the user must send the escape sequence to set the desired screen width. These also place the cursor at the top, left screen position and clear the screen.
   for 80 columns escape [? 3 l
   for 132 columns escape [? 3 h

   Note

   A lower case l is used here.

2. The standard escape sequences to position the cursor and set double height and width lines can be used. The user is responsible for keeping track of what lines have been modified so no attempt is made to put more characters on a line than it can hold.

   CAUTION

   Each line ends with a termination code and pointer to the next line. Video display hardware uses these in its operation. Destroying these values in either screen display or attribute space causes unpredictable results on the display.

3. Each character (data) screen position has a related attribute. When the screen width escape sequence initializes the screen, these attributes are all set to the "off" condition.
   Bit assignments for character attributes are:

   Bit 0 = Reverse Video
   0 = normal
   1 = reverse video
   Bit 1 = Bold
   0 = bold
   1 = not bold
   Bit 2 = Blink
   0 = blink
   1 = not blink
   Bit 3 = Underscore
   0 = underscore
   1 = not underscore

4. Contents of character locations can be changed at any time. However due to the way the cursor is implemented, attributes at the cursor position cannot be changed at will. When the user wishes to change the attributes of the character at the cursor position, he must use the DISABLE CURSOR function. This removes all cursor-related attribute affects. After the attributes have been changed

as desired, the user must use the ENABLE CURSOR function to restore the cursor to operation. See sections 10.1.5 and 10.1.6 for these functions.

6.7 KEY ACCESS SERVICES

This allows a "sophisticated user" to obtain "raw" key data (e.g. a code for left arrow instead of an escape sequence) to simplify the process of detecting special keys. If no key is waiting for detection a "no data" status is returned.

Two different layers of access are provided. The lowest level (Level 1) gives a unique 16-bit code for any key in combination with any or all of the Shift, Caps Lock, or Ctrl keys. It also identifies the function keys with a unique code (reference table X). The highest level (Level 2) is the same as the VT102 generates, plus additional 8-bit codes for certain keys and foreign keyboards. Certain keys are trapped out for special processing and are never seen in the buffer. The following keys cannot be remapped:

Key	Position
Hold Screen	G99
Set-Up	G01
Control	C99
Caps Lock	C00
Shift Keys	B99,B[illegible]

Any other keys may be re-mapped by a "console" mode user.

7.0 FUNCTIONAL DEFINITION

7.1 OPERATIONAL DESCRIPTION

The VT102 emulation is always resident in the PC100's ROM, and can be used even without working floppy disks.

The VT102 "console" emulator must be completely interrupt driven. The "terminal" VT102 uses a "background" routine to add the additional functions of printer port and modem protocols. The VT102 HDX modem protocols are not supported by the firmware.

The VT102 emulator must operate in two distinct modes. Terminal mode provides VT102 capabilities. Console mode also has VT102 capabilities with these exceptions: no printer port, no local echo, and modem protocol equivalent to full duplex data leads only.

7.2 TRANSMITTED CHARACTERS

The LK201 Keyboard transmits a code for each key that identifies the physical location of that key on the keyboard. These position codes are converted to character codes by means of ROM-resident language tables. The ROM must be mapped by language to the keyboard (different keycap legends). Two different types of codes are passed to routines requesting keyboard data. These types are designated as Level 1 and Level 2. Level 2 is the standard 7-bit codes transmitted by a VT102 with the addition of the DEC STD 169 multi-national character codes being sent in the context of the current language option. At Level 2 (terminal mode) all keys not defined in a normal VT102 send no code and cause the bell to beep. In console mode, level 2, the function keys not defined in normal VT102 send escape sequences (see section 7.2.7). Level 2 supports all the VT102 key-generated escape sequences (cursor and keypad keys) in the current key mode context (keypad numeric/application, cursor key normal/application). In addition, foreign keyboard support includes a correspondence/data processing mode that allows up to four different character codes per key. This mode is a Set-Up parameter and allows a foreign keyboard user to access key codes he normally loses because of his special character requirements.

Level 1 is only available to a sophisticated user in console mode. This provides a unique 16-bit code for any key in combination with the CAPS LOCK, SHIFT, and CONTROL keys with the following exceptions:

Hold Screen - not available
SET-UP - not available

The keyboard may be broken into several functional key groups. Each has its own general characteristics.

Note

> The following refers to the keyboard layout shown in the figure at the end of this section. This layout differs from a VT102 keyboard.

7.2.1 Un-Seen Fixed Function Keys - HOLD SCREEN, SET-UP

These keys always provide the same function regardless of console or terminal mode and are never provided to any level of output request.

7.2.1.1 Hold Screen - Position G99 - Freezes the screen display or unfreezes it (toggle mode). Any attempt to output any character is blocked until Hold Screen is "off". May cause an XOFF to be sent in terminal mode if receive buffer reaches high water mark and auto XON/XOFF is enabled. This is equal to the NO SCROLL key on a VT102.

Note

> If the user does not want blocking, he should test the state (available in SYSPAR) and put off "console out" until the user unblocks the display process by turning the Hold Screen off.

7.2.1.2 Set-Up - Position G01 - This causes entry to and exit from Set-Up mode. A system reset occurs in Set-Up mode when the CONTROL key is pressed in combination with the Set-Up key.

7.2.2 Fixed Function Keys - Escape, Line Feed, Backspace, Shift, Control, Tab, Return, Delete

These keys always provide the same function regardless of console or terminal mode and are provided to any level of output request.

7.2.2.1 ESCAPE - POSTION G11 - Escape at all times generates the ASCII backspace character code, 1B (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys.

7.2.2.2 LINE FEED - POSITION G13 - Line feed at all times generates the ASCII line feed character code, 0A (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys.

7.2.2.3 BACKSPACE - POSITION G12 - Backspace at all times generates the ASCII backspace character code, 08 (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys.

7.2.2.4 SHIFT (2 Keys) -POSITION B99, B11 - Shift at all levels causes a modification of the codes being generated by the alpha, numeric, and symbol keys. For alpha keys it sends the upper case code. The numeric and symbol keys send the code for the upper character shown on the keycap. If there are multiple upper and/or lower characters shown on the keycap, then the upper character/case is sent according to the correspondence/data processing mode in effect at the time.

7.2.2.5 CONTROL - POSITION C99 - Control at all levels causes a modification of the codes being generated by the alpha keys and some of the symbol keys and the space bar. Some of the symbol keys are only accessible with some foreign keyboards by using the data processing mode. The control codes remain associated with the keycap legend. If, for example, the alpha key for C is moved, a <Ctrl/C> still generates the ETX code.

7.2.2.6 LOCK - POSITION C00 - Lock at all levels causes selection of upper case for all alpha keys when "on." "On" state is indicated when the LED marked "Lock" is lit.

7.2.2.7 TAB - POSITION D00 - Tab at all times generates the ASCII horizontal tab code, 09 (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys (except in SET-UP mode).

7.2.2.8 RETURN - POSITION C13 - Return at all times generates the ASCII carriage return code, 0D (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys.

Note

> If New-Line mode is selected, this key will generate a CR LF combination.

7.2.2.9 DELETE - POSITION E13 - Delete at all times generates the ASCII delete character code, 7F (hex). It is not affected by SHIFT, CONTROL, or CAPS LOCK keys.

7.2.3 Alpha and Symbol Keys - POSITIONS E00-E12, D01-D12, C01-C12, B00-B10

These are the Standard Keys affected by the SHIFT, CONTROL, and CAPS LOCK keys, as well as the correspondence/data processing mode. They are mapped to match the keycap legends according to the language being used.

Note

> This requires use of the shift key in addition to the control key for those 'symbols' that generate control codes. Some foreign language keyboards may also require use of the 'data processing' keyboard mode (see SETUP) in order to select the desired 'symbol'.

7.2.4 Keypad Keys - POSITION E20-E23, D20-D23, C20-C23, B20-B22, A21-A23

These keys act the same at Level 2 as in a VT102 except for the Enter key which is not used for print functions. Either character codes or escape sequences are generated depending on keypad numeric/application mode and ANSI/VT52 mode. At Level 1 these keys are considered as function keys, and control/shift/caps lock flags are included in the 16-bit code.

7.2.5 Cursor Arrow Keys - POSITION C17, B16-B18

These keys act the same at Level 2 as in a VT102. Escape sequences are generated depending on cursor key normal/application mode and ANSI/VT52 mode. At Level 1 these keys are considered as function keys and the control/shift/caps lock flags are included in the 16-bit code.

7.2.6 Special Function Keys - Print Screen, Break

These keys have a defined function in terminal mode and are available in console mode only at Level 1.

7.2.6.1 Print Screen - POSITION G00 - In terminal mode Print Screen causes the contents of the screen to be sent to the attached printer. Pressing <Ctrl/Print Screen> causes the terminal to toggle back and forth between auto print "on" and "off." This key is used in place of the ENTER key on a VT102 for printer functions. In console mode, this key is considered a function key and is only available at Level 1. The control/shift/caps lock flags are included in the 16-bit code.

7.2.6.2 Break Key - POSITION G03 - In terminal mode, the Break key acts just like in a VT102 including Shift-Break for a long break disconnect and Control-Break for a transmitted answerback message. In console mode, this key is considered a function key and is only available at Level 1. The control/shift/caps lock flags are included in the 16-bit code.

7.2.7 Function Keys - POSITION G02, G05-G09, G14-G16, G20-G23, E16-E18, - D16-D18, A99 - These keys are only available in console mode at either Level 1 or Level 2 (as escape sequences). The control/shift/caps lock flags are included in the 16-bit level 1 code.

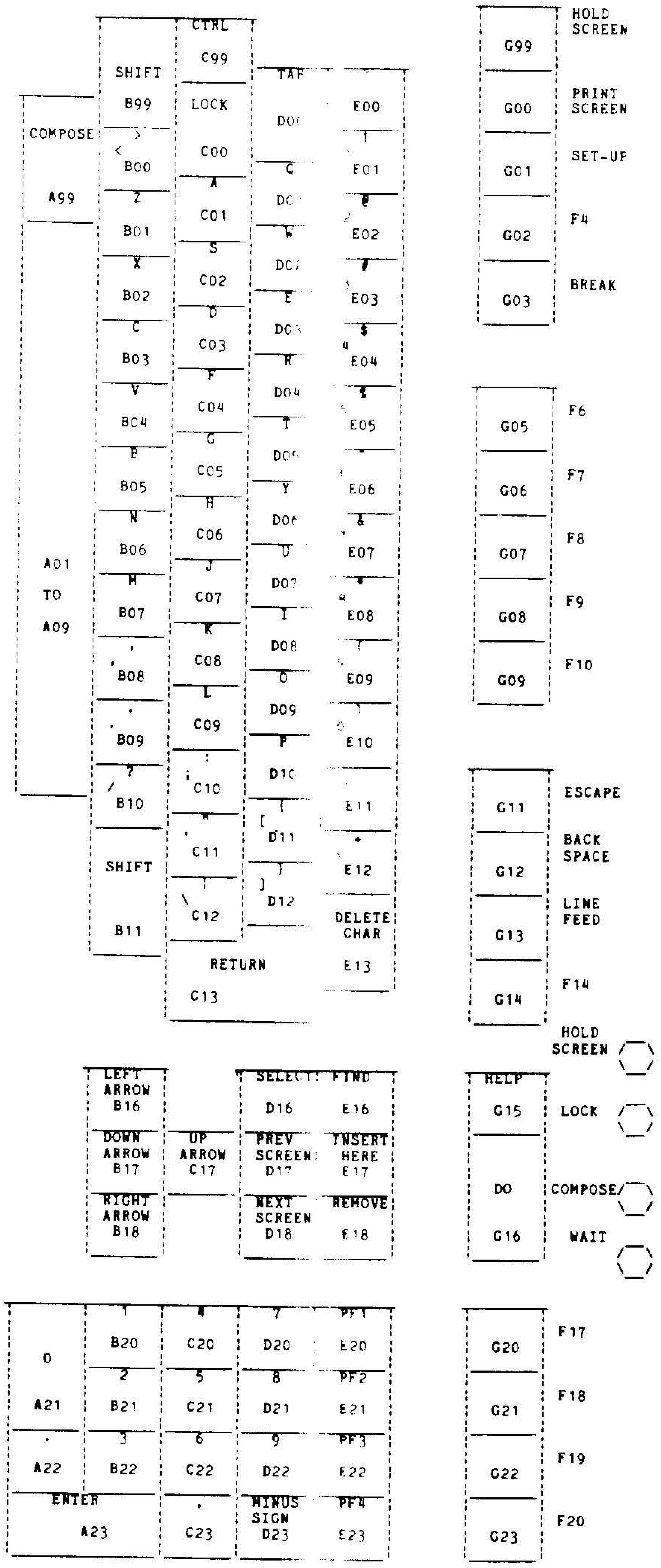
Note

> Some of these keys have functions within Set-Up mode:
> Help - position G15
> Next Screen - position D18
> Previous Screen - position D17

ESCAPE SEQUENCES GENRATED BY FUNCTION KEYS (all final characters are 'tilde').

Name	Position	ESC Sequence
F4	G02	ESC [1 4 ~
F6	G05	ESC [1 7 ~
F7	G06	ESC [1 8 ~
F8	G07	ESC [1 9 ~
F9	G08	ESC [2 0 ~
F10	G09	ESC [2 1 ~
F14	G14	ESC [2 6 ~
HELP	G15	ESC [2 8 ~
DO	G16	ESC [2 9 ~
F17	G20	ESC [3 1 ~
F18	G21	ESC [3 2 ~
F19	G22	ESC [3 3 ~
F20	G23	ESC [3 4 ~
FIND	E16	ESC [1 ~
INSERT	E17	ESC [2 ~
REMOVE	E18	ESC [3 ~
SELECT	D16	ESC [4 ~
PREV SCREEN	D17	ESC [5 ~
NEXT SCREEN	D18	ESC [6 ~
COMPOSE	A99	ESC [10 ~

The keyboard layout of the PC100 is shown below.


COMPOSE
A99
A01
TO
A09
SHIFT
B99
B00
B01
B02
B03
B04
B05
B06
B07
B08
B09
B10
SHIFT
B11
CTRL
C99
LOCK
C00
C01
C02
C03
C04
C05
C06
C07
C08
C09
C10
C11
C12
RETURN
C13
TAB
D04
D08
D09
D11
D12
E00
E01
E02
E03
E04
E05
E06
E07
E08
E09
E10
E11
E12
DELETE CHAR
E13
G99
HOLD SCREEN
G00
PRINT SCREEN
G01
SET-UP
G02
F4
G03
BREAK
G05
F6
G06
F7
G07
F8
G08
F9
G09
F10
G11
ESCAPE
G12
BACK SPACE
G13
LINE FEED
G14
F14
HOLD SCREEN
LEFT ARROW
B16
DOWN ARROW
B17
UP ARROW
C17
RIGHT ARROW
B18
SELECT
D16
FIND
E16
PREV SCREEN
D17
INSERT HERE
E17
NEXT SCREEN
D18
REMOVE
E18
HELP
G15
LOCK
DO
G16
COMPOSE
WAIT
0
A21
A22
ENTER
A23
B20
B21
B22
C20
C21
C22
C23
7
D20
8
D21
9
D22
MINUS SIGN
D23
PF1
E20
PF2
E21
PF3
E22
PF4
E23
G20
F17
G21
F18
G22
F19
G23
F20

7.3 RECEIVED CHARACTER PROCESSING

7.3.1 Received Character Processing

VT102 emulation responds to different characters and control sequences so as to duplicate the response of the VT102. The full description is found in section 8 (Terminal Control Functions) of the VT102 Engineering Specification. A summary follows.

Reception of 8-bit control codes cause the same effect as if the 2 character 7-bit escape-FE equivalent had been received.

Note

Reception of the 'RESET TO INITIAL STATE' escape sequence (ESC c) will also reset the 7201 serial line controller effectively disabling its interrupt structure. This escape sequence should not be used from within an application without restoring the interrupt structure. Normally, the operating system is in control of the interrupts of the 7201 and an application will not know how to restructure the interrupts.

Note

Some operational capabilities are common to both terminal and console modes; others are not. These are noted below in the following format:

1. Those common to both are marked BOTH.

2. Differences are marked as either TERMINAL or CONSOLE.

7.3.2 ANSII Mode Control Functions

BOTH These functions give the terminal its intelligence. Examples in this group include:

1. Cursor functions (Movement, positioning, position reporting, etc.)

2. Mode setting and resetting

3. Line and character modes (Blink character, underline character, etc.)

4. Terminal editing (Insert and delete line and character, etc.)

5. Terminal identify, test, and status

6. Terminal characteristics (Key autorepeat, linefeed/newline mode, etc.)

CONSOLE MODE No local echo, modem, or printer functions in "console" mode.

7.3.3 Operational Variations

Some of the sequences listed in the previous section affect the terminal's operational mode. Examples include VT52 or ANSI mode, smooth or jump scroll and the like.

The escape sequence which normally causes a VT102 to execute self-tests are ignored and the status report always returns a "no problem" status.

7.3.4 Terminal Reports

BOTH	The host computer tells the VT102 emulator to report its current cursor position, status, and device attributes.
TERMINAL MODE	Printer status reports occur only in Terminal Mode.

7.3.5 Terminal Reset

BOTH	The terminal also responds to a command from the computer which causes it to reset to its saved state. This is not the same as a keyboard entered system reset which returns to the opening menu. This recalls the NVM set-ups, clears the screen, and homes the cursor only.

7.4 VT102 CONTROL OF ATTACHED DEVICES

TERMINAL MODE	VT102 emulation firmware has the same control over the printer and EIA modem as the VT102.
CONSOLE MODE	VT102 emulation firmware does not have control over the printer and comm ports or EIA modem lines.

7.4.1 Modem Control

TERMINAL MODE Terminal Mode has full duplex capabilites:

1. Data leads only
2. Full modem
3. Asymmetrical (require special cable)

Terminal Mode does not have half duplex capabilites:

CONSOLE MODE In console mode the "application" must control the comm port hardware directly.

7.4.2 Printer Control

BOTH The baud rates available for the printer port are more limited than VT102 baud rates. The available baud rates are: 75, 150, 300, 600, 1200, 2400, 4800, 9600.

TERMINAL MODE VT102 firmware contains code to control a serially-connected printer in this mode only. The emulation supports the print screen and print cursor line commands, auto print mode, and printer control mode.

CONSOLE MODE In Console Mode the printer is only accessible to an "application" through direct control of the hardware.

7.5 OTHER DIFFERENCES - TERMINAL VS CONSOLE MODES

TERMINAL MODE This mode emulates a VT102, where keyboard characters g o to the communication line, and communication line characters go to the display, plus all the printer support and Set-Up and modem control, etc.

Differences from a real VT102 are due to differences in the keyboard (keys in different places), different numbers of and different labels for LEDs and more extensive Set-Up information required (option ID's, volumes of bell and click, etc.). Also, no support of HDX modem protocols is provided.

CONSOLE MODE This mode acts like a VT102 console (without modem control, local echo, or printer port) to an application, where keyboard characters go to the a p p l i c a t i o n , application characters go to the display, and the printer is under control of the application; the communication port is under control of the application. However, the VT102 can still be put into Set-Up mode and have its characteristics changed like a real console.

Because there is no XON/XOFF between the "console VT102" and an application, both are running on the same CPU and/or in a single threaded environment. As a result the service routine hangs waiting for buffer space to become available (emptied by interrupt process) before returning to the calling routine.

There are two access methods:

1. The "application" accesses the VT102 "console" through the interface as though it were a serial line controller communicating over a high speed communications line.

2. A "sophisticated application" may access the video display RAM through indirect write of the display/attribute memory. This bypasses normal VT102 rcvd char processing. A "sophisticated user" also obtains "raw" key data to bypass escape sequence encoding and decoding needs.

Note

Level 1 and Level 2 character-available status are not interchangeable; a Level 2 character-available does not imply a Level 1 character-available.

Within the VT102 emulation there are routines to pass status and data from/to the interface layer. Within the VT102 emulation, interrupts must not be disabled any longer than 450 microseconds. This requires cautions on re-entrancy of routines that are shared and potential problems of not completing an interrupt handler that re-enables interrupts and then does not complete before it is called again.

DATA FLOW DIAGRAMS FOR THE DIFFERENT MODES OF OPERATION

```
                          -------------------------
                          |                       |  'TERMINAL' mode
                          |        PRINTER        |<---------------
                          |                       |  all print    |
                          -------------------------   functions   |
                                                                   |
                                                                   |
-----------------                   bell                  -----------------
|               |<----------------------------------------|               |
|   KEYBOARD    |                                         |    DISPLAY    |
|               |---------------------------------------->|               |
-----------------                                         -----------------

-----------------         -------------------------       -----------------
|               |         |                       |       |               |
|  APPLICATION  |         |     SET-UP PROCESS    |       |      COMM     |
|               |         |                       |       |               |
-----------------         -------------------------       -----------------
```

Figure 1. "Terminal" Mode "Off-Line"

```
                         -------------------------
                         |                       |
                         |        PRINTER        |
                         |                       |
                         -------------------------

-----------------                 bell                  -----------------
|               |<--------------------------------------|               |
|   KEYBOARD    |                                       |    DISPLAY    |
|               |----------------|        |------------>|               |
-----------------                |        |             -----------------
                                 |        |
                                 V        |
-----------------        -------------------------      -----------------
|               |        |                       |      |               |
|  APPLICATION  |        |    SET-UP PROCESS     |      |     COMM      |
|               |        |                       |      |               |
-----------------        -------------------------      -----------------
```

Figure 2. "Terminal" Or "Console" Mode "Set-Up"

```
                         -------------------------
                         |                       |
                         |        PRINTER        |
                         |                       |
                         -------------------------

-----------------                 bell                  -----------------
|               |<--------------------------------------|               |
|   KEYBOARD    |                             local     |    DISPLAY    |
|               |-----------------            -------->|               |
-----------------                |            | echo    -----------------
                                 |            |                  A
                                 |            |                  |
                                 ------------------------------  |
                                                              |  |
                                                              V  |
-----------------        -------------------------      -----------------
|               |        |                       |      |               |
|  APPLICATION  |        |    SET-UP PROCESS     |      |     COMM      |
|               |        |                       |      |               |
-----------------        -------------------------      -----------------
```

Figure 3. "Terminal" Mode "On Line" No Printer Functions

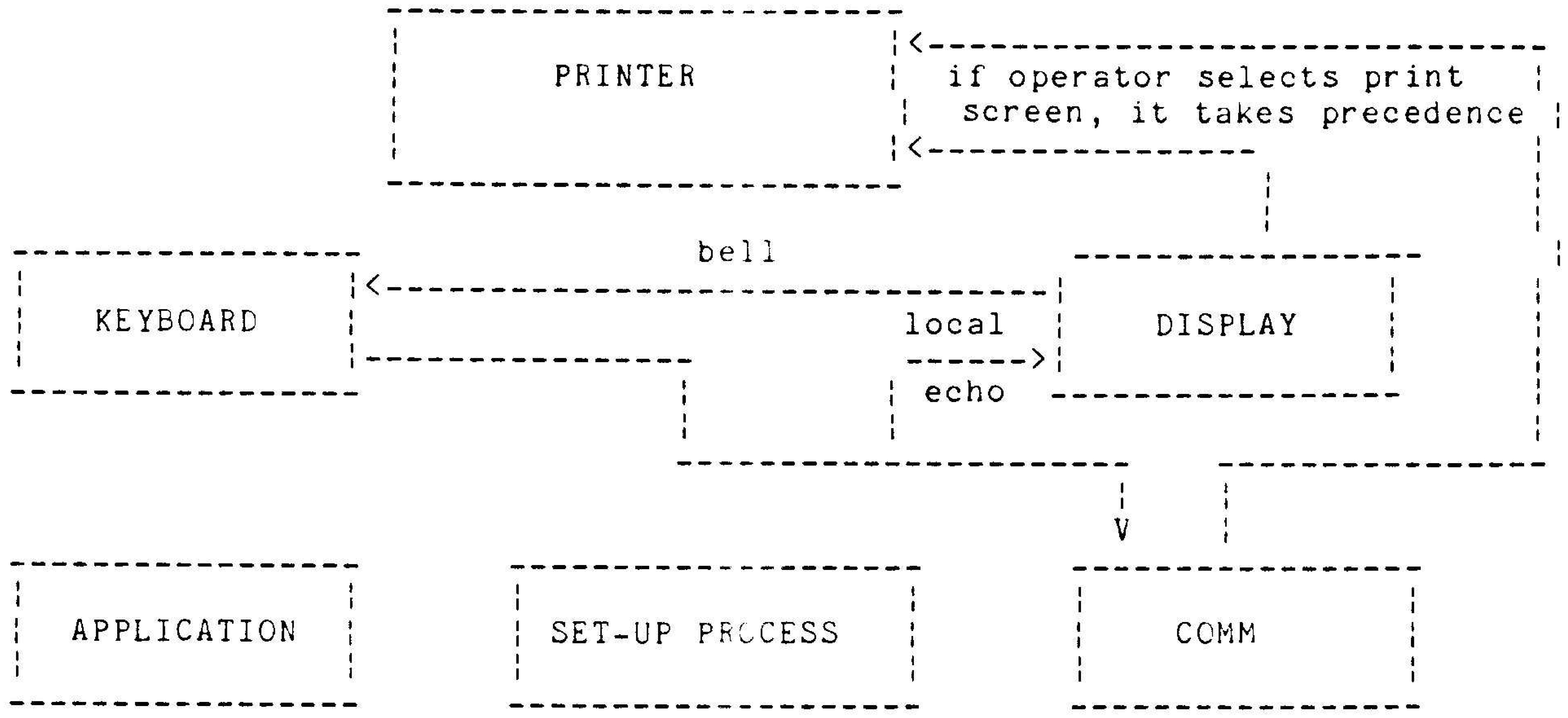


Figure 4. "Terminal" Mode "On Line In "Printer Controller

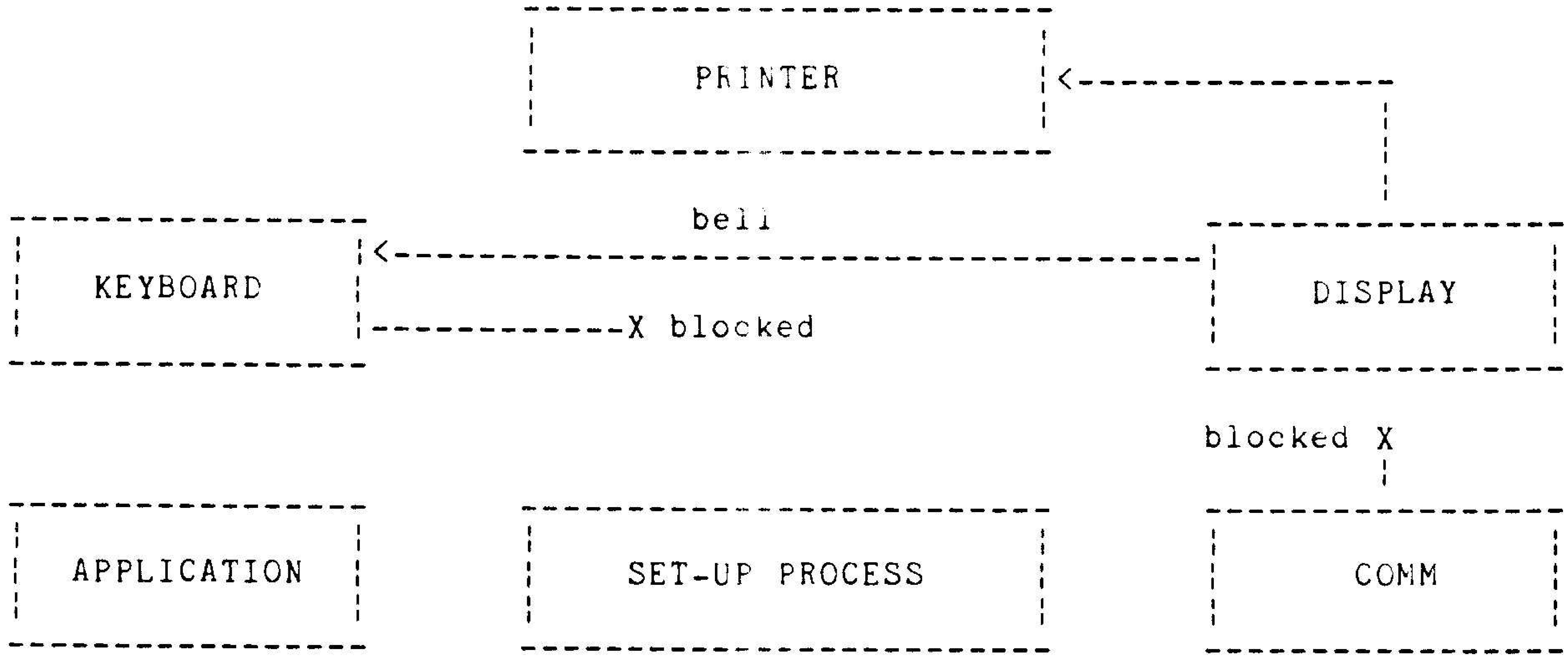


Figure 5. Terminal Mode On Line Printing From Screen

```
                        -------------------------
                        |                       |
                        |        PRINTER        |
                        |                       |
                        -------------------------
                          A
                          |     bell
-----------------         |                           -----------------
|               |<--------|---------------------------|               |
|   KEYBOARD    |         |                           |    DISPLAY    |
|               |         |                   ------->|               |
-----------------         |                   |       -----------------
   |    -------------------                   |
   |    |   -----------------------------------
   |    |   |  -------------------------------------------------
   |    |   |  |                                               |
   V    V   |  V                                               V
-----------------       -------------------------     -----------------
|               |       |                       |     |               |
|  APPLICATION  |       |    SET-UP PROCESS     |     |     COMM      |
|               |       |                       |     |               |
-----------------       -------------------------     -----------------
```

Figure 6. Console Mode

8.0 EXTERNAL INTERACTIONS AND IMPACT

8.1 OPERATING SYSTEM

VT102 emulation allows access to its subroutines by the operating system. It does not require operating system services and runs without the use of disks.

8.2 STACK OVERHEAD

Hardware interrupts and the attendant interrupt handlers impose a stack overhead on any program running at the time of the interrupt. The interrupt handlers swap to their own stack as soon as possible to minimize this overhead. However, it still requires three words due to the interrupt process itself (CS, IP, FLAGS) and the firmware pushes three more words before it swaps to its own stack.

Software interrupts do not swap stacks, and the user must provide sufficient stack space (plus hardware interrupt overhead). The amount of stack required is 25 words (plus hardware, total = 31).

8.3 STACK USE BY APPLICATIONS

The firmware hardware interrupt handlers swap stacks, if required, so they always run on their own stack. Some of the handlers re-enable interrupts after this swap, but while still within the interrupt handler, so other high priority interrupts are not held up. At the conclusion of the original firmware interrupt handler, the stacks are swapped back to the original. There is a caution for "application" interrupt handlers that expect to use the stack or registers to pass data between their interrupt handler and the main-line program. If the application interrupt occurs while still within the firmware interrupt handler, then current stack and registers will not be preserved for main-line use. Application interrupt handlers must never use registers to pass data and must guarantee their own private stack if they are going to pass data on a stack.

9.0 VT102

9.1 SET-UP

The non-volatile Set-Up parameters are different from those in the VT102 due to hardware differences and system requirements.

The non-volatile Set-Up parameters that are the same as the VT102 are:

Minor Field	Major Field	Default
on line/local mode	header	on line
80/132 column mode	parameter	80
tab stop bit map	TABs	every 8 positions
scroll - SMOOTH/JUMP	parameter	smooth
auto repeat - ON/OFF	parameter	on
screen background - LIGHT/DARK	parameter	dark
cursor - UNDERLINE/BLOCK	parameter	block
margin bell - ON/OFF	parameter	off
keyclick - ON/OFF	parameter	on
ANSI/VT52	parameter	ANSI
* auto xon/xoff - ON/OFF	parameter	on
US/UK char set	parameter	US
auto wrap - ON/OFF	parameter	off
line feed/new line	parameter	LF
* local echo - ON/OFF	parameter	off
* print termination char - none/FF	parameter	FF
* print extent - ALL SCREEN/SCROLLING REGION	parameter	all
comm stop bits - 1/2	parameter	1
* rcv parity check - ON/OFF	parameter	on
* break enabled - ON/OFF	parameter	on
* disconnect char enable-ON/OFF	parameter	off
* disconnect delay- 60 MS/2 SEC	parameter	2 sec
* auto answerback enabled - ON/OFF	parameter	off
50/60 hz	parameter	60
comm data/parity bits	modem	7S
comm xmit rate	modem	9600
comm rcv rate	modem	9600
* comm modem line discipline	modem	FDXA
* disconnect char	modem	none
answerback message - UP TO 20 CHAR (PLUS 2 DELIMITERS)	answerback	none
printer data/parity bits	printer	8N
printer xmit/rcv rate	printer	4800

Insertion/replacement mode is always saved as replacement mode.

VT102 non-volatile parameters not included in the emulator are:

screen brightness -	NO SOFTWARE CONTROL
WPS keyboard -	NO KEYBOARD VARIATION FOR THIS

HDX protocol related parameters

New non-volatile parameters to be added in emulator are:

bell volume	misc	7(max)
keyclick volume	misc	7(max)
options memory installed	option RAM	none
- AUTOMATIC SCREEN BLANKING AFTER ELAPSED TIME - on/off	parameter	on
scroll rate for smooth scroll - 3,6,12 LINES/SEC AT 60HZ (slower at 50HZ)	misc	6
- KEYBOARD KEY ASSIGNMENTS (for foreign language keyboard support)	parameter	correspondence
correspondence/data processing		

LEGEND: * only apply in terminal mode

9.1.1 Set-Up DIsplay and Operation

The Set-Up displays consist of two major screen areas. One is fixed and the other variable is a function of what part of Set-Up is used. The fixed part of the display, called the header, consists of the words shown in Figure 7.

Beneath the header is the variable area which is one of eight different displays called "major fields." On entering the Set-Up mode, the tab settings major field is automatically displayed. There are two types of major fields. One type is accessed by stepping through them sequentially by means of the Next Screen and Previous Screen keys. The other type is entered directly at any time (almost) by means of the Help key (help field) and shifted A (answerback field). Within some of the major fields are variable numbers of minor fields, one for each parameter selectable within that major field. Minor fields are stepped through by means of the left and right arrow keys.

```
-----------------------------------------------------------------
|                                                                |
|       SSS    EEE    TTTTT          U    U   PPP               |
|       S      E        T            U    U   P  P              |
|        S     EE       T     XXX    U    U   PPP               |
|         S    E        T            U    U   P                 |
|       SSS    EEE      T             U U     P                 |
|                                                                |
|                                                                |
|                                                                |
|     TO EXIT PRESS "SET-UP"                                     |
|     ----------------------                                     |
|     PRESS "HELP"                                               |
|     TO RESET TYPE <CTRL/SET-UP>                                |
|     VERSION 01.01.01 A                                         |
|     ----------------------                                     |
|     | ON LINE (or LOCAL) |                                     |
|     ----------------------                                     |
|               A                                                |
|               |                                                |
|               |                                                |
|               ---------------- reverse video                   |
-----------------------------------------------------------------
```

Figure 7. Set-Up Mode Header Display

Except for 'HELP' and 'ANSWERBACK' fields, the following keys always have the same effect:

SET-UP	exit set-up mode
CTRL-SET-UP	reset system
HELP	enter/exit help field
NEXT SCREEN	select next major field
PREV SCREEN	select preceeding major field
UPPER/LOWER CASE L	toggle line/local state
UP-ARROW	select next higher value
DOWN-ARROW	select next lower value
SHIFT-S	save current set-ups in NVM
SHIFT-D	set current set-ups to defaults (does not save)
SHIFT-R	recall saved set-ups from NVM
SHIFT-A	enter answerback field

9.1.1.1 Help Field - The Help field is displayed by pressing the Help key. It is entered at any time except when already in the answerback field. It presents a short list of how to access the major sequential fields, minor fields, and how to change values. The only key honored while in "Help" is the Help key which causes an exit to the field displayed before entry to "Help."

9.1.1.2 Answerback Field - The answerback field is displayed at any time by pressing the SHIFT and A keys simultaneously. The major field heading ANSWERBACK is displayed and beneath it "A =". The first character typed (and displayed) is a delimiter. Up to 20 characters can be entered following the delimiter. The string automatically terminates after the 20 characters or before that when a second delimiter entry is made. Any character can be entered in the answerback string, including NULL, DELETE, or CTRL characters. Normally non-printing control characters show as their related ASCII characters in reverse video. For example, ETX (control C) shows up as a reverse video C. Answerback is exited by typing the delimiter character a second time or by reaching the 20 character entry limit. String entry errors can only be fixed by exiting answerback and re-entering to make a new string. The string is eliminated by making the first two characters the same (two delimiters with nothing between).

9.1.1.3 Tab Settings Field - The tab setting field is displayed on entry to Set-Up. It consists of a row of numbers running repetitively from 1 through 0 with alternate groups of 10 shown in reverse video. The line above this row of numbers contains a variable number of the letter "T." The location of the T symbol signifies that a tab stop is set at that point. There are 80 or 132 possible tab stops depending on the screen width setting in effect. A cursor shows the current active position. This cursor moves by means of the left and right arrow keys, Return, Tab (to next "T" location), and the space bar(acts the same as right arrow). The "T" key (or Up or Down arrow keys) reverses the tab setting at the active position. In addition, Ctrl Tab clears all tab stops and SHIFT TAb sets the default tab stops at every 8th position. Beginning with the 9th position, a T is displayed.

9.1.1.4 Parameter Major Field - The parameter major field displays all the Set-Up parameters that have only two possible values (usually on/off). The parameters are shown as a row of 1 and 0's with alternate groups of four shown in reverse video. The current active parameter is shown by a cursor. This cursor moves left and right by means of the left and right arrow keys, Return (to start of line), Tab, and space bar (acts the same as right arrow). As the cursor moves to a new position, a field is displayed below the line that details the name of the parameter and what the 1 and 0 values mean. The 1 and 0 values are changed by means of the up and down arrow keys. Some of these parameters have an immediate affect if changed. Others do not take affect until exiting from Set-Up mode. Changing to either 80 or 132 columns destroys the user's text display (normally it is preserved during Set-Up and restored on exit)

9.1.1.5 Modem Field - The modem field displays the parameters for the modem port (communications port). Some of these are only applicable in "terminal" mode. Each parameter has a range of possible values, and the field is shown as a list on the display (Figure 8). The active parameter is shown by a reverse video field.

```
 ____________________________________________________________________
|                                                                    |
|     MODEM                                                          |
|     -----                                                          |
|      8N         DATA/PARITY                                        |
|     --------                                                       |
| |-->| 9600 |     XMIT BAUD                                         |
| |   --------                                                       |
| |      9600      RCV BAUD                                          |
| |                                                                  |
| |      FDXA      PROTOCOL                                          |
| |                                                                  |
| ---------------- reverse video                                     |
|                                                                    |
|____________________________________________________________________|
```

Figure 8. Modem Major Field Display

The value of the active parameter changes by means of the up and down arrow keys which cause the parameter to step through its allowable values. The active parameter selection changes by means of the left and right arrow keys.

9.1.1.6 Printer Field - The printer field displays the parameters for the printer port. The active parameter selection and value changes are the same as for the modem.

9.1.1.7 Miscellaneous Field - The miscellaneous field is used to select the bell and key click volumes and the smooth scroll rate. The active parameter selection and value changes are the same as for the modem.

9.1.1.8 Memory Size Field - The memory size field identifies the presence and size of the memory extension option so it is included in the self-testing procedure. It only contains a single parameter and the value is stepped through by means of the up and down arrow keys.

9.1.1.9 **Storing the Set-Ups** - The current contents of all the Set-Up fields, including any answerback message, are transferred to non-volatile storage by pressing the SHIFT and "S" keys simultaneously (not while in HELP or ANSWERBACK).

Note

> Insertion/replacement mode is always set to replacement mode before saving is done.

9.1.1.10 **Using Default Set-Ups - All the Set-Up fields are set to** their respective default conditions by pressing the SHIFT and "D" keys simultaneously (not while in HELP or ANSWERBACK). Defaults are listed in section 9.1.

Note

> This does not enter the defaults into non-volatile storage (must use "store"), but it causes the user's text to be erased from the screen and causes a line disconnect in "terminal" mode.

9.1.1.11 **Recalling Stored Parameters** - The parameters stored in non-volatile storage are recalled for use by pressing the SHIFT and "R" keys simultaneously. This also causes the user's text to be erased from the screen and causes a line disconnect in "terminal" mode. Stored parameters are also automatically recalled at power-up, system reset, and reception of the RIS escape sequence (ESC c). RIS will also do a channel reset of the 7201 printer and communications ports, destroying the mode and interrupt structures in use at the time.

9.2 RESET TECHNIQUE

Within Set-Up mode, a "reset" key combination (CONTROL SET-UP) causes a jump to the start of the self-test at a point which allows it to be distinguished from a power-up.

10.0 INTERFACE LAYER

Functions provided by the firmware for use by operating systems and sophisticated applications.

10.1 SOFTWARE INTERRUPT TYPE 40 (DECIMAL)

Function code is passed in DI. It is organized as 16 even number values for ease in using as table offsets to dispatch to service routines. Refer to Table 3.

Table 3. Function Codes

Hex	Function
0	CONSOLE OUT
2	CONSOLE IN
4	CONSOLE IN STATUS
6	LEVEL 1 (16-BIT) CONSOLE IN
8	DISABLE CURSOR
A	ENABLE CURSOR
C	INITIALIZE INTERRUPT VECTORS
E	RETURN CLOCK RATE
10	SET LEDs ON KEYBOARD
12	CLEAR LEDs ON KEYBOARD
14	SEND DATA TO SCREEN
16	INIT 7201 TO NVM PARAMETERS
18	RAW KEYBOARD DATA
1A	RESERVED
1C	RESERVED
1E	RESERVED

Note
Only registers CS: , SS: , and DS: are preserved.

10.1.1 Console Out

ENTRY DI = 0
AL = character in ASCII (includes 8-bit multinational characters)

10.1.2 Level 2 Console In

ENTRY DI = 2

EXIT AL = Level 2 keyboard character if available
CL = returned status
0 = no character available
FF = character is in AL

10.1.3 Level 2 Console In Status

```
ENTRY   DI = 4

EXIT    CL = returned status
             0 = no character available
            FF = character is available
```

Note

Cannot be used to detect status of Level 1 character available.

10.1.4 Level 1 Console In

```
ENTRY   DI = 6

EXIT    AX = Level 1 character
        CL = returned status
             0 = no character available
             1 = no character available due to Level 2 sequence not
                 completed (previous key caused a string of Level 2
                 characters to be generated.  Level 2 buffer has not been
                 emptied of this string yet.)
            FF = character is in AX
```

RULES FOR LEVEL 1 CHARACTERS

```
              AH                AL
              11 10  9  8
    ______________________________________________
   |       |  |  |  |  |  |                      |
   |_______|__|__|__|__|__|______________________|
            ^   ^   ^   ^
            |   |   |   |
            |   |   |   '--- FUNCTION KEY FLAG 1 = This is a function key.
            |   |   |
            |   |   '------- SHIFT FLAG   1 = Shift key in effect.
            |   |
            |   '----------- CONTROL FLAG   1 = Control key in effect.
            |
            '--------------- CAPS LOCK FLAG   1 = Caps Lock key in effect.
```

For non-function keys, the AL = character (including 8-bit multinational characters). The effect of shift/control/caps lock is already taken into account.

For function keys, the AH = flag data and AL = function key code (ASCII) as follows:

KEY CODE HEX	KEY
0	HELP
1	DO
2	COMPOSE
3	PRINT SCREEN
5	F4
7	F6
9	F7
B	F8
D	F9
F	F10
11	F14
13	F17
15	F18
17	F19
19	F20
1B	FIND
1D	INSERT
1F	REMOVE
21	SELECT
23	PREV SCREEN
25	NEXT SCREEN
27	UP-ARROW
29	DOWN-ARROW
2B	RIGHT-ARROW
2D	LEFT-ARROW
2F	KEYPAD 0
32	KEYPAD 1
35	KEYPAD 2
38	KEYPAD 3
3B	KEYPAD 4
3E	KEYPAD 5
41	KEYPAD 6
44	KEYPAD 7
47	KEYPAD 8
4A	KEYPAD 9
4D	KEYPAD DASH
50	KEYPAD COMMA
53	KEYPAD PERIOD
56	KEYPAD ENTER
59	KEYPAD PF1
5C	KEYPAD PF2
5F	KEYPAD PF3
62	KEYPAD PF4
65	BREAK

10.1.5 Disable Cursor

ENTRY DI = 8

EXIT There is no cursor affect on attributes at cursor position. The cursor does not show on the screen.

Note

The disable and enable cursor functions are only to be used immediately preceeding and following a function 14 that may attempt to set the attributes at the current cursor position. They cannot be used to make the cursor "invisble" while it is moved around by other escape sequences or control characters. These functions must be used in pairs; first disable, then enable.

10.1.6 Enable Cursor

ENTRY DI = A

EXIT Cursor does affect attributes at cursor position. The cursor shows on the display.

10.1.7 Initialize Interrupt Vectors

ENTRY DI = C

EXIT The following interrupt types are modified for use by the firmware:

Type 2	NMI for RAM option parity error
32.	vertical frequency refresh
34.	graphics controller option
35.	DMA controller of extended comms option
37.	7201 of extended comms option
38.	keyboard 8251
44.	time tick

In addition, the extended comms option and graphics option are reset to the disabled state.

The extended comms option is reset by writing anything to 8088 port 27 hex.

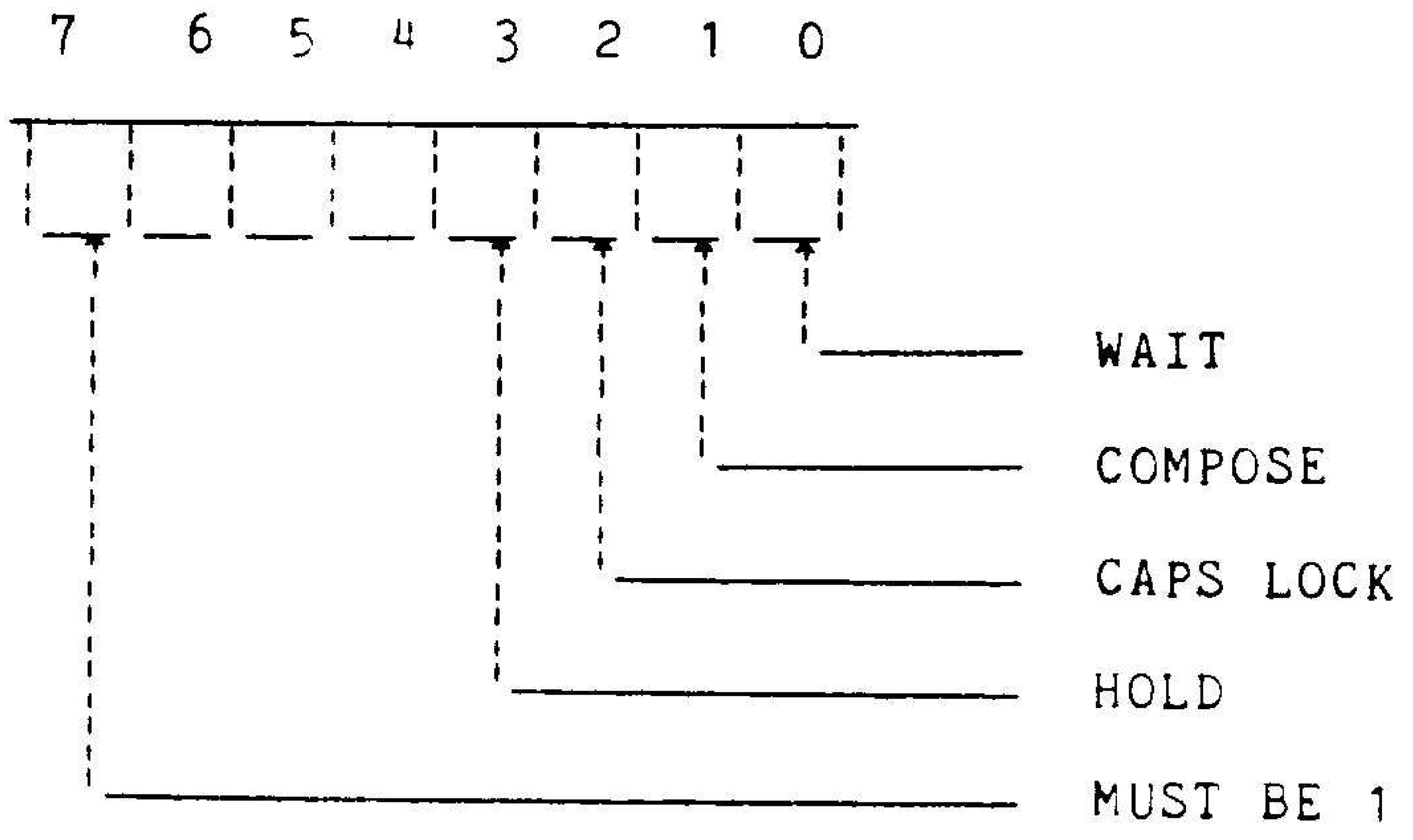
The graphics option is reset by toggling bit 0 of 8088 port 50 hex from high to low to high.

10.1.10 Clear Keyboard LEDs

ENTRY DI = 12

AL = bit pattern of LEDs to turn off

bit set to 1 = LED off



EXIT LEDS as requested.

10.1.11 Send Data To Screen

ENTRY DI = 14

AX = TRANSFER TYPE
0 = CHARACTERS AND ATTRIBUTES
1 = ATTRIBUTES ONLY
2 = CHARACTERS ONLY
3 - FFFF = UNDEFINED

BX = START LOCATION IN DISPLAY
BL = LINE NUMBER (1-24)
BH = COLUMN NUMBER (1-132)

Note

max column number is a function of screen width (80,132) and line width (single,double)

CX = NUMBER OF CHARACTERS/ATTRIB TO TRANSFER, IN BYTES

Note

User is responsible for limiting size of transfer so end-of-line is not exceeded.

DX = OFFEST TO START OF ATTRIBUTES RELATIVE TO USERS DS:

SI = OFFSET TO START OF CHARACTERS RELATIVE TO USERS DS:

BP = CHARACTER/ATTRIB SEGMENT COPY OF USERS DS: USED FOR OFFSETS
PASSED IN DX AND SI.

Note

Characters and attributes must be relative to same value of DS.

10.1.12 INIT 7201 TO NVM PARAMETERS

NVM refers to current contents of the shadow RAM which are displayed in SET-UP. These are not necessarily the same as the currently saved SET-UP parameters.

ENTRY DI = 16
DL = 0

FUNCTION

1. Does a channel reset on both channels A and B
2. Sets baud rates for modem and printer ports according to NVM
3. Loads 10 (hex) into write register 2A, and 0 into write register 2B
4. Loads write registers 4A,B with X16 clock, parity/stop bits according to NVM for the port
5. Loads write registers 3A,B with number of receive data bits according to NVM for the port and enables receive
6. Loads write registers 5A,B with number of transmit data bits according to NVM for the port and enable transmit

Note

When data/parity is 7M or 7S, the 7201 is actually set for eight data bits, no parity.

10.1.8 Return Clock Rate

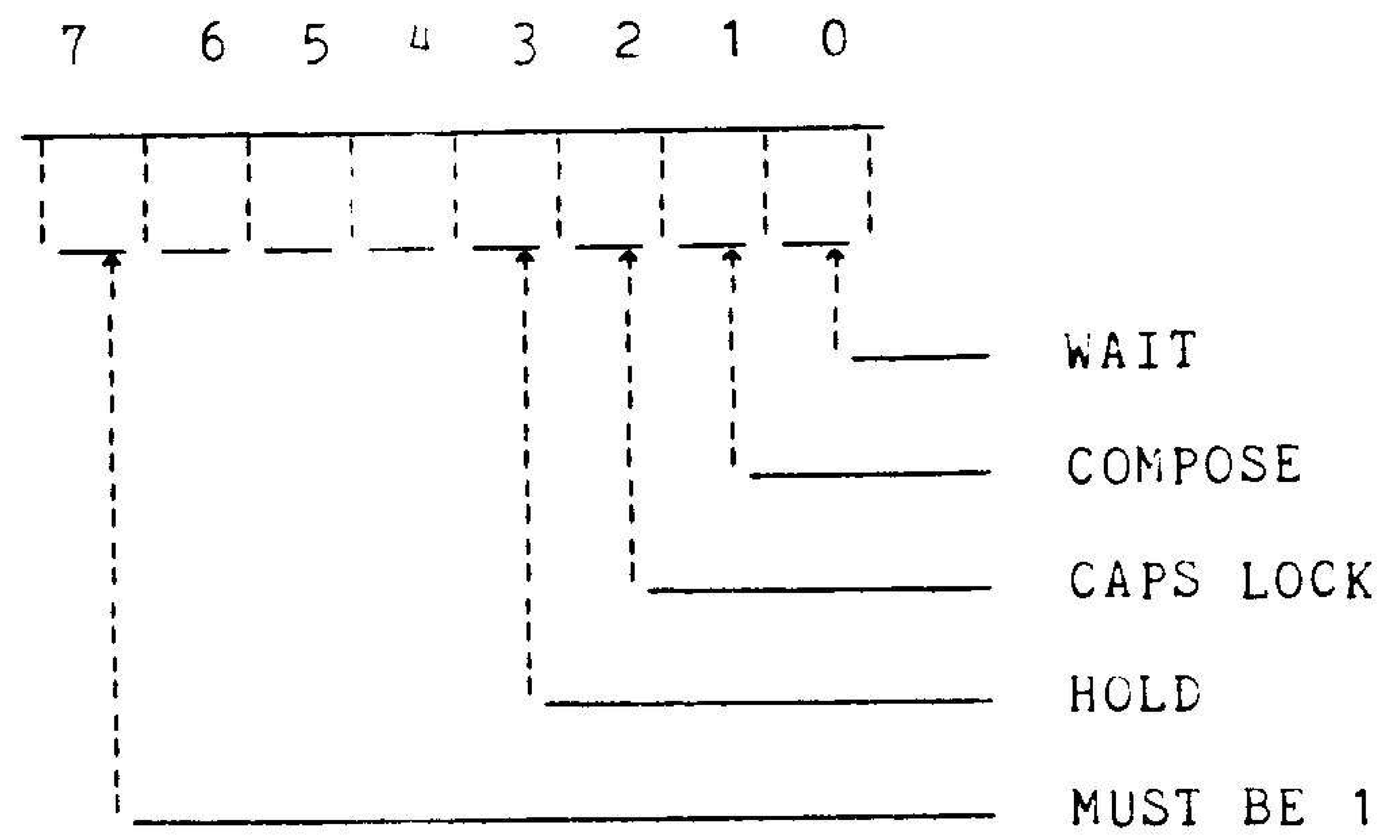
ENTRY DI = E

EXIT AL = clock rate
bit 0 = 0 60 Hz
= 1 50 Hz

10.1.9 Set Keyboard LEDs

Set and clear LEDs are only for the indicators. They do not cause any action that may be implied by the label of the LED being affected. Firmware normally maintains all but the "compose" LED in the proper state.

ENTRY DI = 10
AL = bit pattern of LEDs to turn on
bit set to 1 = LED on



EXIT LEDs as requested

10.1.13 Raw Keyboard Data

ENTRY   DI = 18

This function is provided for diagnostics to test the keyboard and is only intended for that purpose. It is documented here for completeness.

Note

> The SHIFT, CAPS LOCK, and CONTROL keys can only be read in conjunction with another key by looking at the flag bits in AH. The SET-UP will not be detectable by a program, but an operator will see entry into set-up mode on the display. The HOLD SCREEN key will not be detectable by a program, but an operator will see the "HOLD SCREEN" LED on the keyboard light up.

```
EXIT    CL = 0  no key available
           = 1  key available
        AL = key location matrix code as defined in LK201 Keyboard
             specification
        AH = flag bits as for function 6, level 1 console in.
```

11.0 IMAGE OF Z80 RAM SPACE TO BE LOADED

Any routines that must be loaded into the Z80 space for it to run initially must be put there by the 8088. The ROM must contain this code because it cannot be obtained from the floppy disk until after the floppy handler is loaded into the Z80 and the interface to access the loader is also in place. This initial code must know how to take care of the "flipped" Z80 RAM addresses and relocate routines in the proper locations in RAM.

12.0 BOOT LOADER TO READ TRACK 0, SECTOR 1 OF FLOPPY

The purpose of the boot loader is to get into memory a minimal routine which initiates the loading of the overall operating system. The boot loader accesses any available drive as selected by the operator. If an error occurs, an error message is displayed and the opening menu is re-displayed.

The boot loader loads 512 bytes from the specified drive, track 0, sector 1 into the shared RAM beginning at address 1000 (hex) and jumps to it. If the loaded routine returns an error, the opening menu is re-displayed. The selected drive is available by examining the register which did the selection. The loaded data must be Z80 instructions.

12.1 BOOT PROCESS

The boot process consists of the fo wing steps:

1. Operator selects the drive boot from by means of the menu.
2. The 8088 passes control to Z80 routine. The routine attempts to read track 0, sector 1 the selected drive into address 1000 (hex).

3. While the Z80 is attempti to read, the 8088 counts time and monitors a semaphore locat at 0:FFF (initially set to 0).

4. If the semaphore does not ange from 0 within approximately 10 seconds, there is some sor major problem. The Z80 is stopped and the message FAILURE, Z ESPONSE, CONSULT YOUR USER'S GUIDE is displayed along with the op ng menu. The operator may then make a selection from the menu.

5. If the Z80 routine detec a "drive not ready" condition, it returns a value of 6 in t semaphore location. The 8088 displays the message 'Failure, driv t ready, consult your user guide' and redisplays the opening me A 'drive not ready' is caused when either a drive door is op , no disk is in the drive, or when there is no drive in the s m.

6. If the Z80 detects an er reading track 0, sector 1 of the selected drive due to a se or CRC error, it retries up to two more times. If all three a pts fail, the Z80 returns the value 2 in the semaphore location. e 8088 displays the message "Failure, boot loader, consult your r guide" and re-displays the opening menu.

7. If the Z80 successfully r s track 0, sector 1 of the selected drive, it checks the cont of address 1000 (hex). If this is not the Z80 code for disa interrupts (F3), the Z80 returns the value 4 in the semaphore ation. The 8088 displays the message 'Failure, non-system disk, sult your user guide' and redisplays the opening menu.

Note

> This requires the Z code resident in track 0, sector 1 to begin wi a DI instruction.

1. If the Z80 successfull ads track 0, sector 1 of the selected drive into address 100 hex), and the first byte is the DI instruction, control ansfers to this secondary boot by jumping to address 100 hex).

Note

The seconda boot is Z80 code.

2. The secondary boot is responsible for loading the remainder of the system.

3. If the loading process fails, control returns to the 8088 by placing the value 8 in the semaphore location. The 8088 displays the message "Failure, system loader, consult your user guide', halts the Z80, reloads the boot reading routine, and re-displays the opening menu.

4. When the loading process completes successfully, control passes to the 8088 by placing the value A (hex) in the semaphore location. The 8088 passes control to the loaded system by doing an indirect, intersegment, far jump via 0:FFB.

Note

The contents of four bytes, starting at 0:FFB, must be pre-loaded with the code segment and an offset of the 8088 (system) start address:

FFB, FFC contain IP
FFD, FFE contain CS

Note

The selected drive is determined by reading the Z80 port 40 (hex), mask to read bits 0 and 1, and the drive selected is:

Drive	Bit 1	Bit 0
A	0	0
B	0	1
C	1	0
D	1	1

5. When the menu choice is made, the screen is blanked by means of a hardware gate. This leaves the menu image still in display RAM, it just does not show. The loaded program should send escape strings to erase the screen and home the cursor, then unblank the display by writing an 83 (hex)to 8088 port 0A (hex). This port should not be written to at any other time as it contains other bits which could cause major problems if they do not agree with an internally maintained copy of the port. The firmware properly maintains this port at all other times for NVM and Z80 control.

13.0 MENU SELECTION PROCESS

After initialization and self-test (or reset), the operator is presented with a choice of things to do.

1. VT102 terminal mode - system looks like a VT102 to a host connected to the communications port
2. Boot operating system - read in and start the operating system, drive is selectable
3. Run more extensive self-tests

14.0 SYSTEM PARAMETER INFORMATION

This is a word of data which maintains bit flags which define the system state. It is used mainly by the firmware, but is defined here for use by special routines (e.g. 3277 emulator) that need to know about these parameters in order to avoid problems.

Location Mnemonic - Syspar
Address - EF00:FFE
Bit Assignments

Bit 0 - emulator mode flag
0 = console mode
1 = terminal mode

Bit 1 - On/Off Line flag
0 = On Line
1 = Off Line, Local

Bit 2 - Set-Up mode flag
0 = normal
1 = in Set-Up

Bit 3 - Hold Screen mode flag
0 = normal
1 = Hold Screen in effect

Bit 4 - Scroll in process flag
0 = normal
1 = smooth scroll in process

Bits 5-7 reserved

Bit 8 - bundle card option present flag
0 = option present
1 = option not present

Bit 9 - floppy controller board present flag
0 = floppy present
1 = floppy not present

Bit 10 - graphics option present flag
0 = graphics option present
1 = graphics option not present

Bit 11 - memory option present flag
0 = memory option present
1 = memory option not present

Bits 12 - 15 reserved

15.0 POWER SUPPLY

15.1 POWER CONNECTOR

The power connector on the mother board is a 13-pin in-line connector with the following pinout:

1 **ACOK** This signal indicates the presence or absence of valid ac power entering the power supply. When valid ac power is present, this signal will be high (open circuit) and when the ac power is lower than the required minimum input voltage, this signal will be low (short circuit to logic ground).

Low State (ac power invalid): The voltage level of this signal is 0.45 volts maximum when sinking 2.0 milliamperes.

High State (ac power valid): The voltage on this signal is pulled-up by external circuitry. When pulled up to 10.0 volts, the leakage current to logic ground shall be 25 microamperes maximum at the maximum external pull-up voltage of 10.0 volts.

Transition Times: The rise time (10% to 90%) and fall time (90% to 10%) shall be 1.0 microsecond maximum.

2 **VBIAS** When the ac input power is within its valid range, this source has an open circuit voltage of 12.0 volts + 10% and a source impedance of 470 ohms + 10%. This signal is used for manufacturing to automate test monitoring via connecting the LED write signal through a jumper to this pin.

Power-Up: During power-up of the power supply, this source has an open circuit voltage of 8.0 volts minimum at the time when the dc output voltages start to increase from zero volts.

Power Down: During power-down of the power supply, the voltage on this source decreases toward zero. Due to output loading variations, there is no definable relationship between the decay of this output and the decay of the dc output voltages.

3 **Key** This pin must be missing from the mother board.

4 **-12V OUT** Maximum Current -12 VDC 0.0 amperes minimum to 0.35 amperes maximum

Output Voltage Variations:

Total Tolerance	+ 7%
Initial Tolerance	+ 3%
Line Regulation	+ 1.5%
Load Regulation	+ 4.0%
5.1 Volt Load Interaction	+ 3.0%
Temperature Stability	+ 0.05%/C degrees
Long Term Stability	+ 1%/1000 hrs
Ripple and Noise	120 millivolts, peak to peak
Overcurrent Trip Point	
Minimum	0.4 ampere
Maximum	1.5 ampere
Short Circuit Current	0.5 ampere, maximum
Overvoltage Protection	
Range,Minimum Trip Point	-13.0 Volts
Absolute Maximum Output	-15.0 Volts

5,6 **+12.1V OUT** Maximum Current

+12 VDC 0.6 ampere minimum to 6.7 amperes maximum

Output Voltage Variations

Total Tolerance	+ 5%
Initial Tolerance	+ 2%
Line Regulation	+ 3%
Load Regulation	+ 3%
5.1 Volt Load Interaction	+ 3%
Temperature Stability	+ 0.05%/C degrees
Long Term Stability	+ 1%/1000 hrs
Ripple and Noise	75 millivolts, peak to peak
Overcurrent Trip Point	Minimum: 6.8 amperes Maximum: 8.0 amperes
Short Circuit Current	5.2 amperes (Maximum)

Overvoltage Protection Range: not applicable

7,8,9 **+5.1 V OUT** Maximum Current: +5 Vdc amperes minimum to 10.5 amperes maximum

Output Voltage Variations:

Total Tolerance	+ 5%
Initial Tolerance	+ 2%
Line Regulation	+ 1%
Load Regulation	+ 3%
12.1 Volt Load Interaction	+ 3%
Temperature Stability	+ 0.05%/C degrees
Long Term Stability	+ 1%/1000 h
Ripple and Noise	50 millivolts, peak to peak

7,8,9 +5.1 V OUT (continued)	Overcurrent Trip Point, minimum: 10.7 amperes maximum: 12.6 amperes Short Circuit Current: 8.2 amperes, maximum Overvoltage Protection Range, Minimum trip point: 5.80 volts Absolute maximum output: Voltage 7.0 volts
10,11, 12,13	DC Power Return Signal Ground

16.0 CONNECTOR OUTPUTS

16.1 VIDEO INTERFACE CONNECTOR

This connector is a 15-pin D-type female connector supplying interface signals and power to the PC100 monitor and keyboard with the following pinout:

Pin	Name	Description
1	Red Shield	Ground connector for red gun shield
2	Green Shield	Ground connector for green gun shield
3	Blue Shield	Ground connector for blue gun shield
4	Mono Shield	Ground connector for B/W video gun shield
5,6	GND	+12V returns
7,8	+12V	+12V DC to monitor and keyboard
9	Blue	RS170 "like" composite red gun output
10	Green	RS170 "like" composite green gun output
11	Red	RS170 "like" composite blue gun output
12	Mono video	RS170 "like" composite B/W video output/green drive signal for applications color monitor
13	Not used	
14	KBD RCV data	RS423 serial data from keyboard
15	KBD TX data	RS423 serial data to keyboard

16.2 COMMUNICATIONS INTERFACE CONNECTOR

Pin Number	Signal Description	Mnemonic Direction
1	Protective Ground	PROT GND
2	Transmit Data	XMIT DATA
3	Receive Data	REC DATA
4	Request To Send	RTS
5	Clear To Send	CTS
6	Data Set Ready	DSR
7	Signal Ground	GND
8	Receive Line Signal Det.	RLSD
9	Not Used	N/U
10	Not Used	N/U

16.2 COMMUNICATIONS INTERFACE CONNECTOR (Continued)

Pin Number	Signal Description	Mnemonic	Direction
11	Not Used	N/U	
12	Speed Indicator/Secondary Receive Line Signal Det.	SI/SRLSD	
13	Not used		
14	Not used		
15	Send Clock	SEND CLK	
16	Not Used	N/U	
17	Receive Clock	REC CLK	
18	Not Used	N/U	
19	Secondary Request To Send	SRTS	
20	Data Terminal Ready	DTR	
21	Not Used	N/U	
22	Ring Indicator	RI	
23	Speed Select	SPDSEL	
24	Not Used	N/U	
25	Not Used	N/U	

16.2.1 Communications Signal Descriptions

Note

The following terminology is used interchangeable to describe the communications signals:
Negative Voltage = 1 = Mark = OFF
Positive Voltage = 0 = Space = ON

1. **Protective Ground** - This connector is connected to the chassis via wire jumper TBD.

2. **Signal Ground** - This circuit establishes the common ground reference potential for all interface circuits except protective ground.

3. **Transmitted Data (output)** - Signals on the line represent the serially encoded characters that are transmitted from the communications port. This circuit is held in the marking state during intervals between characters and at all times when no data is being transmitted.

4. **Receive Data (input)** - Signals on this circuit represent the serially encoded characters to be received.

5. **Request to Send (output)** - Assertion of this signal indicates that the channel is ready for transmission.

6. **Clear to Send (input)** - When this signal is asserted, it indicates that the modem is ready for transmission.

7. **Data Set Ready (input)** - The on condition of DSR indicates that the modem is in data mode, and that the control signals asserted by the modem are valid.

8. **Receive Line Signal Detector (input)** - Also called Carrier Detect. The modem asserts this signal ON when the received signal is of sufficient quality and magnitude.

9. **Data Terminal Ready (output)** - This signal is turned ON whenever the channel is ready for transmission.

10. **Ring Indicator (input)** - The ON condition indicates that a ringing signal is being received from the comm line.

11. **Speed Indicator (input)** - This signal allows some modems to control channel bit rates.

12. **Secondary Receive Line Signal Detect (input)** - This circuit is used in half duplex coded control with reverse channel.

Note

Speed Indicator and Secondary Receive Line Signal Detect are two different uses of the same physical line.

13. **Speed Select (output)** - This signal allows the 8088 to control the modulation method of the modem to coincide with its selected bit rate.

14. **Secondary Request to Send (output)** - This signal is used for HDX restraint mode and Asymetric FDX Secondary Request to Send.

15. **Secondary Clear to Send (input)** - In FDX, this signal is the same as Clear to Send. In Asymetric FDX, it provides the functionality for the secondary channel.

16. **Secondary Transmitted Data (output)** - In FDX, this signal is the same as Transmitted Data, but when operating in Asymetric FDX, it provides functionality for the secondary channel.

17. **Send Clock (input)** - This is the external transmit clock that is supplied by the modem substituted for the communication transmit clock when the synchronous select bit is set.

18. **Receive Clock (input)** - This is the external receive clock that is supplied by the modem substituted for the communication receive clock when the synchronous select bit is set.

16.3 PRINTER PORT INTERFACE CONNECTOR

Pin No.	Signal Description	Mnemonic	Direction
1	Protective Ground	PROT GND	------
2	Receive Data	RXD	Output
3	Transmit Data	TXD	Input
5	Clear to Send	CTS	Output *
6	Data Set Ready	DSR	Output *
7	Signal Ground	GND	------
20	Data Terminal Ready	DTR	Input

Note

*This output is always asserted high.

16.4 FLOPPY INTERFACE CONNECTOR

Pin Number	Signal Description	Mnemonic
1	Ground	GND
2	Track greater than 43	TG43
3	Ground	GND
4	Not Used	N/U
5	Ground	GND
6	Select 3	SEL3 L
7	Ground	GND
8	Index	INDEX L
9	Ground	GND
10	Select 0	SEL0 L
11	Ground	GND
12	Select 1	SEL1 L
13	Ground	GND
14	Select 2	SEL2 L
15	Ground	GND
16	Motor On	MOTOR ON L
17	Ground	GND
18	Direction	DIR L
19	Ground	GND
20	Step	STEP L
21	Ground	GND
22	Write Data	WRT DATA L
23	Ground	GND
24	Write Gate	WG L
25	Ground	GND
26	Track 00	TK00 L
27	Ground	GND
28	Write Protect	WRT PRT L
29	Ground	GND
30	Read Data	RD DATA L
31	Ground	GND
32	Side Select	Side OH

16.4 FLOPPY INTERFACE CONNECTOR (Continued)

Pin Number	Signal Description	Mnemonic
33	Ground	GND
34	Drive Ready	READY L

16.4.1 Floppy Signal Descriptions

1. **Select Unit 3 (output, Pin 6)** - When asserted, this signal indicates that the current disk in position 3 is selected.

2. **Index Pulse (input, Pin 8)** - This input informs the controller when the index hole is encountered on the diskette. Minimum pulse width is 20 microseconds.

3. **Select Unit 2 (output, Pin 14)** - When asserted, this signal indicates that the current disk in position 2 is selected.

4. **Select Unit 1 (output, Pin 12)** - When asserted, this signal indicates that the current disk in position 1 is selected.

5. **Select Unit 0 (output, Pin 10)** - When asserted, this signal indicates that the current disk in position 0 is selected.

6. **Motor On (output, Pin 16)** - When asserted, this signal turns on the drive's spindle motor.

7. **Stepping Direction Control (output, Pin 18)** - This direction signal is an active low when stepping the head toward the spindle and active high when stepping the head away from the spindle.

8. **Step Pulse (output, Pin 20)** - This is a 2-microsecond pulse to move the head one track. The direction of the step is determined by the direction output.

9. **Write Data (output, Pin 22)** - This is a 500 ns pulse generated for each flux transition.

10. **Write Gate (output, Pin 24)** - This output is made valid before writing is to be performed to the diskette.

11. **Track 00 (input, Pin 26)** - When asserted, this signal informs the controller that the R/W head is positioned over track 0.

12. **Write Protect (input, Pin 28)** - This input is sampled whenever a write command is received. When asserted, the command terminates and sets the write protect status bit in the FDC status register.

13. **Read Data (input, Pin 30)** - This is the raw data signal from the drive. This signal should be a negative pulse from a minimum of 750 ns to a maximum of 1250 ns for each flux transition.

14. **Side Select (output, Pin 32)** - When high, the outer surface is selected. At present, only single surface drives are available, so this pin would always be high.

15. **Ready (input, Pin 34)** - This bit indicates drive readiness and is sampled for a logic high before a read or write operation. This signal means that a disk is in place and the door is closed and drive selected. The motor does not have to be on.

17.0 OPTIONS

The following assemblies shall be also be offered as options to the base system:

1. Expansion RX50 consisting of:
   a. RX50 disk drive
   b. Data cable for second disk drive unit. This cable will be longer than the standard drive cable.
2. Color graphics
3. Extended communications, giving Bit/Byte/Async communications, as well as a high speed networking capability.

18.0 CABLES

The following cables are included with the system:

1. Monitor cable - transports monochromatic RS-170 "like" video signals to the monitor and supplies the keyboard interface. This cable carries all power and ground to the monitor and keyboard. The cable runs external to the system.

2. RX50 cable - is be a 34-pin ribbon cable to supply interface and ground from the system board to a single RX50 disk drive.

3. Power harness - carries all DC power to the system board and up to two disk drive units.

The following cables are optionally offered with the system. They are non-standard cables.

1. RX50 add-on cable - allows an upgrade to a second RX50 disk drive.

2. Video color cable - allows connection to a color monitor. This cable supplies a keyboard connection to the system.

PC100 SYSTEM SPECIFICATION

19.0 ENVIRONMENTAL

The PC100 meets the requirements of the DEC STD 102, Class A. The PC100 and all peripherals as a part of the system meet the requirements for FCC Class B emitted radiation and conducted.

20.0 RELIABILITY

The PC100 demonstrates mean time between failures of no less than 2800 hours. This correlates to roughly one year of operation.

21.0 PHYSICAL PACKAGING

The outer measurements of the BA25 are 17.5 inches in width, 13.625 inches in depth, and 6.0 inches height. On the front of the unit is the main power switch, and a bezel with pop-out plugs for the RX50 disk drive(s). The back of the unit supplies access for ac power and primary circuit selection switch and circuit breaker, and access to standard and option connectors. The packaging includes a fan.

The system board is housed in the lower portion of the BA25 and is encased in sheet metal to minimize RFI problems. Enough space is available to support another plane of circuit at in the very least 7/8-inch above the system module.

22.0 VIDEO CHARACTER SET

See Appendix A.

23.0 APPLICABLE STANDARDS AND REGULATIONS

The PC100 complies with the following standards:

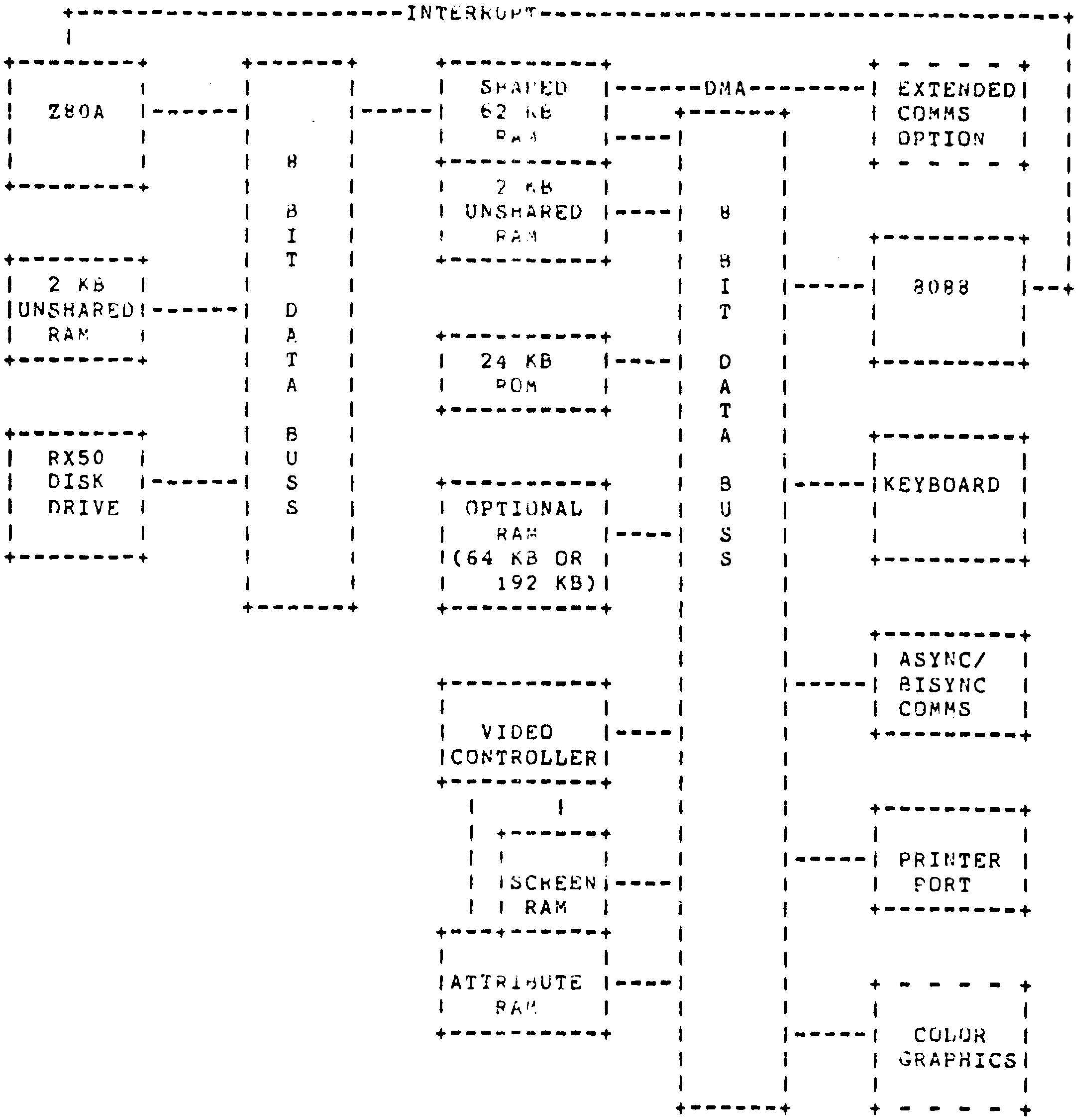
DEC STD 119	Digital Product Safety
DEC STD 102	Environmental Standard for Computers and Peripherals. The PC100 will be a Class A product.
DEC STD 122	AC Power Line Standard
DEC STD 103	Electromagnetic Compatibility (EMC) Hardware Design Requirements (draft). The PC100 will meet FCC class B level.

DEC STD 052, Section 1	Operational Requirements for Asynchronous, Full Duplex, Serial Terminals and System Interfaces Operating as DTE's Connected to EIA RS-232 or CCITT V.28 Point-to-Point Modems.
DEC STD 110	Escape Sequence Standard
DEC STD 111	Terminal Synchronization Standard
DEC STD 107	Digital Standard for Terminal Keyboards
DEC STD 138	Registry of Control Functions (proposed)

In addition, the following non-DEC standards have been used in the design of the PC100:

ANSI X3.16	Character Structure and Character Parity Sense
ANSI X3.4-1977	USA Standard Code for Information Interchange (ASCII)
ANSI X3.41-1974	Code Extension Techniques for Use With ASCII
ANSI X3.64-1977	Additional Controls for Use With ASCII
UL-478	Electronic Data-Processing Units and Systems
CSA C22.2, No. 54	Canadian Electronic Code, Part II, Safety Standards for Electrical Equipment
VDE 0871	Limits of Radio Interference from Radio Frequency Apparatus and Installations
VDE 0875	Regulations for Radio Frequency Suppression
IEC 485	Safety of Data Processing Equipment
FCC Part 15	Rules and Regulations - Radio
EIA RS170	Electrical Performance Standards - Monochrome Television Studio Facilities
CCITT Recommendation V.24	List of Definitions for Interchange Circuit Between Data Terminal Equipment and Data Circuit Terminating Equipment
CCITT Recommendation V.28	Electrical Characteristic for Unbalanced Double-Current Interchange Circuits

RAINBOW TM 100 PERSONAL COMPUTER BLOCK DIAGRAM



RAINBOW TM 100 CP/M-86/80 MEMORY MAP

```
                                            |                     |
                                            |                     |
                                            |                     |
                                            |                     |
                                            |  CPM.SYS : 8088     |
64K  ---------------------------------------|---------------------|
     |                                                            |
     |          Interface Layer : Z80                             |
     |------------------------------------------------------------|
     |          Disk I/O Primitives : Z80                         |
     |------------------------------------------------------------|
     |          Pseudo BIOS, BDOS, CCP : Z80                      |
     |------------------------------------------------------------|
     |          Jump To Pseudo BDOS                               |
61K  |------------------------------------------------------------|
     |                                                            |
     |                                                            |
     |                                                            |
     |                                                            |
     |                    TPA                                     |
     |                                                            |
     |                                                            |
     |                                                            |
     |                                                            |
     |                                       ---------------------|  2K
     |                                      |  Z80 Service        |
     |                                      |  Routine            |
     |                                      |---------------------|  1K
     |                                      |  Interrupt Vectors  |
     |--------------------------------------|---------------------|
                  Z80                               8088
```

CP/M-86/80 Configuration 3: 128K System or greater,
Z80 Program Execution

RAINBOW TM 100 CP/M-86/80 MEMORY MAP

```
64K  ------------------------------------------------
    |                                                |
    |          Interface Layer : Z80                 |
    |------------------------------------------------|
    |        Disk I/O Primitives : Z80               |
    |------------------------------------------------|
    |      Pseudo BIOS, BDOS, CCP : Z80              |
    |------------------------------------------------|
    |                                                |
    |               CPM.SYS : 8088                   |
    |                                                |
    |------------------------------------------------|
    |           Jump To Pseudo BDOS                  |
 48K|------------------------------------------------|
    |                                                |
    |                                                |
    |                                                |
    |                                                |
    |                   TPA                          |
    |                                                |
    |                                                |
    |                                                |
    |                                                |
    |                          ----------------------| 2K
    |                         |   Z80 Service        |
    |                         |     Routine          |
    |                         |----------------------| 1K
    |                         | Interrupt Vectors    |
    |-------------------------|----------------------|
               Z80                     8088
```

CP/M-86/80 Configuration 2: 64K System, Z80 Program Execution

RAINBOW TM 100 CP/M-86/80 MEMORY MAP

```
                         |    (If Available)        |
                         |                          |
                         |                          |
 64K  -------------------|                          |
     |                                              |
     |                                              |
     |                                              |
     |                  TPA                         |
     |                                              |
     |                                              |
     |                                              |
     |                                              |
 15K |----------------------------------------------|
     |                                              |
     |            CPM.SYS : 8088                    |
     |                                              |
  2K |____________________                          |
     |  Disk I/O and      |                         |
     |  Interface Layer   |-------------------------| 1K
     |                    |  Interrupt Vectors      |
     |--------------------|-------------------------|
              Z80                    8088
```

CP/M-86/80 Configuration 1: 8088 Program Execution

RAINBOW ™ 100 PERSONAL COMPUTER PROGRAMMABLE MEMORY