J A G UA R
3 8 6

The material in this manual is for information only and is subject to change without notice.

VERSION: 1.0

RADIO FREQUENCY INTERFERENCE STATEMENT

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

*Reorient the receiving antenna.
*Relocate the computer away from the receiver.
*Move the computer away from the receiver.
*Plug the power cord of computer into a different outlet so that computer and receiver are on different branch circuits.
*Ensure that card slot covers are in place when no card is installed.
*Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
*If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interferences caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interferences.

Note

1. *Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.*

2. *Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.*

3. *After power is on, please wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialize the display adaptor and show messages.*

4. *The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.*

Preface

The manual provides information about the installation and maintenance of OCTEK Jaguar-386 motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide basic information for the general users. There are also some technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK Jaguar-386 motherboard. In the Chapter 2, the functions of Jaguar-386 are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Some technical information are provided in the Chapter 4.

System BIOS and the system setup are described in the appendix A. All the setup procedures are explained. Appendix B contains the information about the memory expansion board.

Additional information are given in appendix C, D, E and F for the maintenance purpose.

CONTENT

Chapter 1
Introduction

OCTEK Jaguar-386 consists of 32-bit 80386 microprocessor, a large cache memory and highly integrated chipsets to provide high performance, reliability and compatibility. OCTEK Jaguar-386 is a perfect choice for CAD/CAM workstation and file server and supports sophisticated 32-bit computing applications and multi-user operating systems.

To speed up the performance of the system, a cache memory with maximum size up to 64KB is incorporated. Frequently used program codes can be fetched by CPU from the high speed cache memory without wait state. Furthermore, access to the main memory is accelerated because the cache controller and the memory controller are integrated together, and operate concurrently. Thus the overhead of accessing the main memory is minimized.

Aimed at supporting advanced CAD/CAM applications, OCTEK Jaguar-386 supports 80387 or WEITEK 3167. The total memory is 16MB. 8MB memory is installed on board and additional 8MB is on memory expansion board which is installed on a fast speed 32-bits memory expansion slot.

Compatibility and reliability are important issues. I/O channel is compatible to standard AT bus. Therefore any AT compatible peripherals may be used on OCTEK Jaguar-386. On board POWERGOOD generator is essential to ensure the reliability of the system and is well-designed to work with all power supplies.

Chapter 2
General Features

SPECIFICATION

Processor :

Intel 80386DX CPU
with optional 80387DX Math
Co-processor
or WEITEK 3167 Coprocessor

Speed :

Turbo/normal speed
Software/hardware selectable

I/O Slot :

Compatible to standard AT bus
Two 8-bit and six 16-bit slots

Cache Memory :

32KB or 64KB Cache Memory
Direct mapped with posted write through operation

Internal Cache :

Built-in 2 way set associative cache controller with integrated 128 Byte cache memory.

Memory :

Shadow RAM for System BIOS and Video BIOS
Page mode/hidden refresh
SIMM sockets for 256K or 1M modules
8M bytes on board
Up to 16M bytes with optional memory expansion board

System Support Functions :

- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery backup

Other Features :

- On board POWERGOOD generation
- External battery connector
- Hardware turbo switch

PROCESSOR

80386DX is a 32-bit microprocessor with 32-bit external data bus and 32-bit external address bus. Therefore it processes more data at the same time than 80286 and can access a large memory size which is necessary for 32-bit applications. To combine the wider bus structure and all the advanced functions on chip, total 275,000 transistors are integrated together.

A advanced pipeline architecture is implemented. Next four bytes of instructions are prefetched into the CPU whenever the bus is idle. The size of the prefetch queue is increased to hold 12 bytes. This architecture reduces the overhead of retrieving and decoding of the instructions.

80386DX is aimed to provide advanced facilities to sophisticated software, but still remains compatible with existing software in the market. It can operate at real mode and protected mode. In Real mode the 386DX operates as a very fast 8086, but with 32-bit extensions if desired. Real mode is required primarily to setup the processor for Protected mode operation. Protected mode provides access to the sophisticated memory managememt, paging and privilege capabilities of the processor. Furthermore, new mechanism allows switching between real mode and protected mode at high speed operation.

Hence applications using EMS memory or extended memory can run efficiently although they need software driver to access the memory beyond 1MB.

The protected mode of 80386 is fully compatible with 80286. All privilege - level and I/O protection system are supported. New system control instructions, memory paging, I/O permission bit map are provided to make 80386 ideal for multi-tasking operation systems.

In addition, a virtual 8086 mode is provided. In this mode, the CPU can be considered by the programs as being divided into several 8086 CPUs and each program has their own CPU and memory space. Several programs for XT/AT as well as operating systems for 80286 and 80386DX can be executed simultaneously. Programs are isolated and protected from each other by 80386DX. Each program can be considered as running at a XT/AT.

Internal memory management unit is complicated, but provides a more flexible addressing scheme for the next generation of operation system. Multitasking, concurrent operation and manipulating huge data base can be accomplished with excellent performance. Paging mechanism is employed by 80386DX to allow powerful operating system to implement virtual memory. Each segment is divided into several pages which are 4K bytes per page. Page mechanism is transparent to software and allows software to address up to 64 terabytes.

Furthermore, the 64KB segment boundary which is an barrier of 8088 and 80286 is removed and the segment length can be increased up to 4GB. It eliminates the need for the software to manage multiple code and data segments and allows software of other operating system to be transferred to PC more easily.

80386DX includes many new instructions for system control, high level language support and processor control. These instructions are used in protected mode. New operation systems and software can make use of these instructions for their advanced features, such as concurrent operation and virtual memory.

MATH COPROCESSOR

The demand for sophisticated, number-crunching scientific and business applications has rapidly increased in recent years. 80386DX features an integer Arithmetic Logic Unit which only handles simple integer operations such as addition and multiplication. Floating-point operations which are actually utilized by applications must be accomplished through software routines.

To overcome this obstacle, external Math coprocessor is necessary. The Math coprocessor contains complex hardware and large data registers for floating-point numeric operations. In OCTEK Jaguar-386, the Math coprocessor is optional and both Intel 80387 and WEITEK 3167 are supported.

80387 is upward object-code compatible from 80287 and 8087, but runs 6 to 11 times faster than 80287 used in AT. It fully implements the IEEE 754 Binary Floating-point Arithmetic standard with a high precision 80-bits internal architecture.

WEITEK 3167 can deliver more power than 80387 and is supported by various operation systems and high level programming language compilers. It has a direct interface with the CPU. So the data are transferred between them at full speed.

CACHE MEMORY

The system performance can not simply be improved by increasing the clock rate of the system. The performance depends on many factors, such as system architecture and memory configuration.

A cache memory system with low cost DRAM as main memory and high speed SRAM as cache memory becomes the only choice for high performance system in terms of price and performance. The frequently used data code instructions are kept in the high speed cache memory. Therefore, most of the memory operations are carried out in the cache memory instead of the slow speed main memory.

The cache controller of Jaguar-386 is integrated into the chipset, which will simplify the system design and reduce the chip count. Furthermore, the cache controller is able to run at three modes: 64K bytes external cache, 32K bytes external cache and internal two-way set associative mode. The 64K bytes and 32K bytes external cache modes are adequate for single user environment as well as multitasking and network operating system. The internal cache mode is suitable for a low cost configuration with optimal performance. In all operation mode, 16MB main memory can be cached. The line size for both cache scheme is 32-byte wide.

The cache controller works jointly with the memory controller. This arrangement can speed up memory access when a cache read miss occurs and hence the overall performance is improved. For a cache read hit, the CPU operation is completed with zero wait state. Posted write mechanism is implemented. The memory write is buffered and runs at zero wait state.

The design of the cache controller is intended to provide optimum performance with simple construction. With 64KB cache memory, hit rate exceeds 95% and the wait state is almost eliminated.

Posted Write through

In a cache system with write through, the CPU has to update both the cache memory and the main memory simultaneously to keep the data consistent. However, the main memory needs many cycles to update the data and thus wait states are needed for all memory write cycles. In a posted write through system, the cache will buffer memory write to the main system memory until the memory bus is available. The CPU can continue processing once it has written to the buffer. In Jaguar-386, zero wait state for memory write operation is achieved. When the memory bus is available, the cache independently completes the write operation to the main memory. The decrease in performance of the write through strategy is thus avoided.

Internal 2-way Set Associative Cache

OCTEK Jaguar-386 provides a built-in 128-bytes two-way set associative cache to boost system performance. No external logic and SRAMs are needed. Although the cache size is 128 bytes, it deliver excellent performance with a two-way set associative architecture.

Additionally, the 128-byte internal cache SRAM or external cache are mutually exclusive, it, thus only one of these schemes can be chosen in the setup procedures.

MEMORY SYSTEM

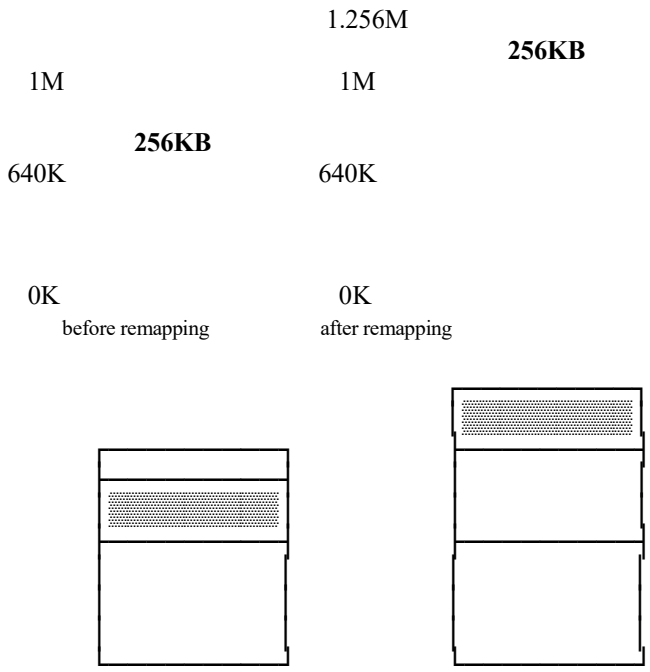
Four banks of DRAMs can be installed. Two banks are available on motherboard and another two banks are on the optional memory expansion board. One bank of DRAM refers to four pieces of SIMM modules. The maximum memory size is 16MB when using 1MB DRAM for all banks.

The memory system supports page mode. Successive memory accesses within the same page need not require wait state and thus CPU can run at full speed.

To enhance the system performance, shadow RAM mode is supported. In shadow RAM mode, system BIOS and video BIOS contained in low speed memory such as EPROM and ROM are copied into DRAM. Improvement is significant because access to DRAM is much faster than ROM.

Another useful feature is memory remapping. 640K bytes is

allocated as base memory. On the other hand, system BIOS and video BIOS occupy some locations between 640K and 1M. When 1M bytes or more are installed, there are some portions of DRAM overlapping with the BIOS which cannot be accessed. Memory remapping allows these portion of memory to be accessed at other locations and thus can be utilized by the software. Memory remapping is supported by hardware and can be enabled in system setup.



Memory Remapping

Because of the shadow RAM and memory remapping feature, the memory size may not be equal to the actual memory size. Suppose that there is 1MB on board. If the shadow RAM feature is enabled, the BIOS will show there is 896KB. 128K bytes are assigned for shadow RAM and can not be used by software. After the shadow RAM is disabled, the memory size is increased to 1MB. When the on-board memory is 4M byte, only 256KB memory can be remapped. For more than 4MB, there is no remapping scheme for Jaguar-386. So only 7808K is available when there is 8M bytes installed. The memory between 640KB to 1M can not be used. The following table is show the remapping scheme for the Jaguar-386 in different memory configuration :

Memory Remapping :

Relocation Memory Size

Memory Install	Shadow RAM Enable	Shadow RAM Disable
1M	256K	384K
2M	256K	384K
4M	256K	256K
>4M	0K	0K

Hidden Refresh

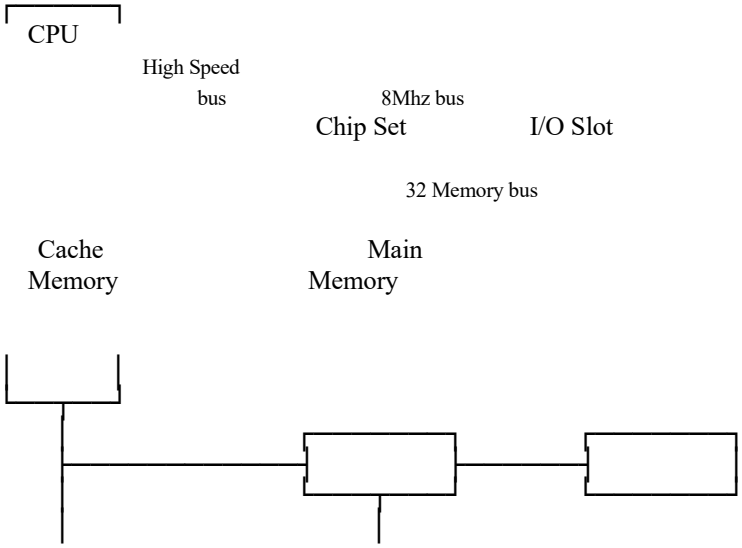
In the original PC/AT design, the CPU suspends its operation during memory refresh. The memory refresh cycle takes about 5% of CPU time which is a short period of time in a slow machine. Nevertheless, in a 33MHz machine, it will significantly downgrade the system performance since the CPU can complete more operations in the same period.

In Jaguar-386, a hidden refresh function is provided. When the hidden refresh function is enabled, the CPU will not stop its operation and the memory refresh operation is transparent to the CPU access. The chipset will monitor the whole system. If the CPU is accessing the main memory, the memory refresh operation is postponed and will be carried out when there is access to AT/expansion bus. Special refresh mechanism is implemented to reduce the period of memory refresh operation.

DUAL BUS DESIGN

It is very important that a high speed system should be compatible with existing peripherals without lowering the performance. To be compatible, the I/O slot should run at 8MHz or slower. On the other hand, the rest of the system are running at full speed.

A dual bus design is employed. A high speed bus links the CPU, coprocessor, cache memory and main memory. This bus is synchronous with the clock of the CPU and the data transfer is 32 bits. Whenever there is a request for transferring to or from I/O slot, the chipset is responsible for handling the conversion between the buses. The clock rate of the high speed bus will not be reduced, which eliminates many compatibility problem.



SYSTEM FUNCTIONS

System functions include :

- Interrupt
- DMA
- Timer
- Real time clock
- Clock and ready generation
- I/O channel control

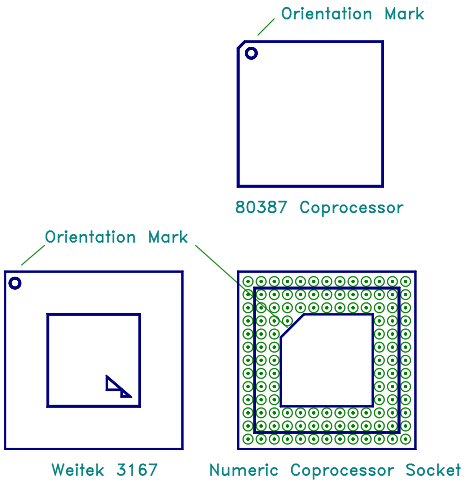
All system functions are 100% compatible to AT standard. I/O channel of OCTEK Jaguar-386 is designed to be compatible with standard AT bus. All the expansion cards conformed to the standard AT bus can be used in OCTEK Jaguar-386 without problem.

Chapter 3
Installing Components

Important Note : Turn off the power before installing or replacing any component.

INSTALLING MATH COPROCESSOR

Math coprocessor 80387 and WEITEK 3167 are PGA devices. Beside the CPU, there is a 121-pin PGA socket. To install Math coprocessor, be sure to line up pin 1 of the Math coprocessor with pin 1 of the socket as shown below. Make sure that the coprocessor is firmly inserted into the socket.



The WEITEK 3167 is a 121-pin chip which matches the pin count of the socket. Align the pins and gently insert the chip into the socket. However, 80387 has 69 pins and its package is smaller and different from WEITEK 3167. So, it only occupies the inner pins of the socket.

Before installing the Math coprocessor, make sure all the pins are straight. The pins are very fragile. Once these pins are bent, the coprocessor may be damaged.

Check whether the system BIOS can find the coprocessor after reset. The system BIOS will display a list of devices on the motherboard after self-test. If the coprocessor is installed, it should show the type of coprocessor.

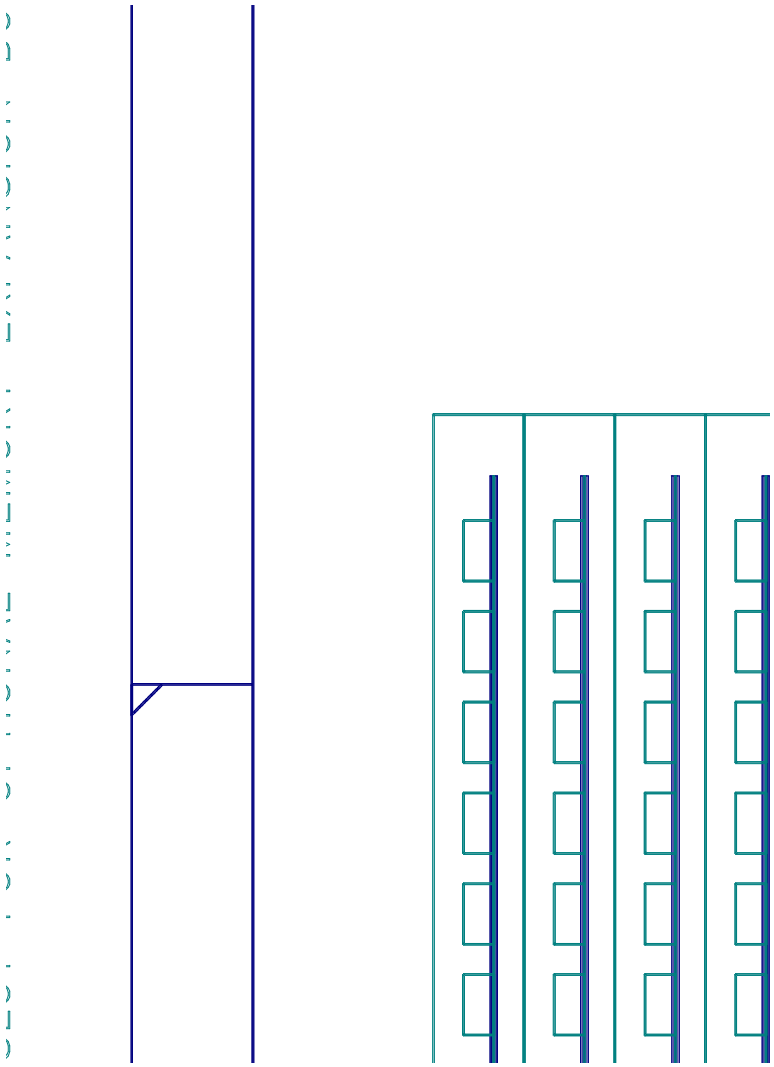
INSTALLING RAM MODULES

OCTEK Jaguar-386 has eight sockets for SIMM modules. Whenever adding memory modules to the motherboard, install four modules at the same time. Also make sure that the chips on the modules face toward the memory expansion slot as shown in the next page.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

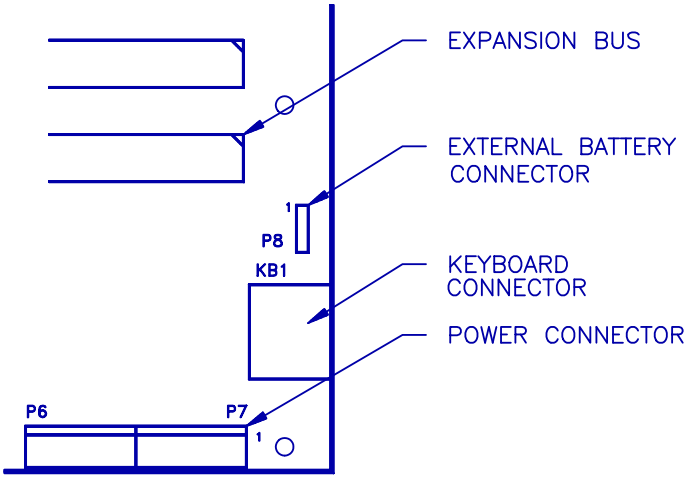
If the BIOS reports an memory error or parity error, drag out the modules and insert them again. If the locking latches are damaged, contact your dealer to replace the socket.



Installing RAM Modules

INSTALLING EXTERNAL BATTERY

To back up the information stored in CMOS RAM, an external battery is needed to provide power after the system is turned off. The connector (P8) for the battery is located beside the keyboard connector on the rear of the board. A 3.6V battery is used. Turn off the power before install the battery. The location of the connector P8 is shown below.



CONFIGURATION OF MEMORY

The configuration of the memory is very flexible. Either 256KB or 1MB SIMM modules are acceptable. There are several combinations of DRAM types you may consider. So, a basic system can be equipped with fewer memory and the system can be upgraded by installing the extended memory. The different configurations of memory is illustrated at the next page.

There are totally four banks of DRAM. Two banks (bank 0 and 1) are on the motherboard and the others (bank 2 and 3) are on the memory expansion board. If bank 0 and 1 are filled, you have to use bank 2 and 3.

Page mode is selected in BIOS. But fast page mode DRAM is recommanded so that page mode operation can be selected to improve the system performance. The memory size is detected automatically by system BIOS. This detection is performed during memory test and the size is indicated after reset. No jumper is needed to be set for the memory size and DRAM type.

To determine what DRAM speed rating to be used is depended on the system speed and wait state. The highest performance is accomplished by using zero wait state, but high speed DRAM has to be used.

The wait state setting is applied to four banks of memory. Therefore make sure to install DRAM modules with the same speed rating, or accommodate the wait state setting to the new DRAM type.

The number of wait state is assigned in the BIOS setup. Improper setting may cause the system malfunction. In this case, reset the CMOS setup using JP7. Then reset the system and go through the system setup again.

DRAM CONFIGURATION

	Bank 0 SIMM (1-4)	Bank 1 SIMM (5-8)	Bank 2 SIMM (9-12)	Bank 3 SIMM (13-16)	Total Memory
1	256K				1M
2	256K	256K			2M
3	1M				4M
4	256K	1M			5M
5	1M	1M			8M
6	1M	1M	1M		12M
7	1M	1M	1M	1M	16M

CONFIGURATION OF CACHE MEMORY

Note : If you have any question about the configuration of cache memory, consult your local dealer. Improper configuration will cause the system malfunction.

The external cache memory is either 32K or 64K bytes. 32K bytes is sufficient for general applications and the performance is improved when the size is increased to 64K bytes.

32K bytes cache memory requires four SRAMs (U3, U5, U7, U9). 64K bytes cache memory requires all eight SRAMs (U2 - U9). The tag RAM (U21-U22) must be installed for both 64K or 32K. The type of SRAM is 8K X 8 and the type of tag RAM is 16K x 4.

For internal cache mode, both tag RAM or SRAM must not be installed. Otherwise all the data will crash and the system will hang.

Make sure that the number of SRAMs is correct and they are installed properly. Otherwise the system will not work.

The speed rating of the SRAM for 25MHz and 33MHz motherboard are listed below:

System Speed	SRAM	Tag RAM
33MHz	25ns	15ns
25MHz	35ns	25ns

The jumper settings for the configuration of cache memory.

Cache Memory Size

	32KB	64KB
JP6	1-2	2-3

Internal Cache

	128 byte
JP1 - JP4	1-2

Note:For external cache, JP1 - JP4 must not be installed.

CONTROL OF SYSTEM SPEED

System Speed can be controlled by hardware switch and keyboard. Connector P3 is connected to the turbo switch of the case. When the system speed is fast, the turbo LED of the case should be turned on.

To change the speed by keyboard, use '-' and '+' of the numeric keypad. Press 'Ctrl', 'Alt' and '-' for slow speed and Press 'Ctrl', 'Alt' and '+' for fast speed.

Whenever the system speed is set to slow by turbo switch, it cannot be changed by keyboard, and vice versa.

RESET CMOS SETUP INFORMATION

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and disconnect the external battery. Then place a jumper on JP7 (1-2) for a while. The internal CMOS status register will be cleared. Then remove the jumper and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information as invalid. So it will prompt you to correct the information. In normal operation, JP7 place in (2-3).

SYSTEM BOARD JUMPER SETTING

There are several options which allow user to select by hardware switches.

Display Selection

JP8	
1-2	CGA, EGA, VGA
2-3	Monochrome display *

Parity Check

JP5	Parity Check
1-2	Enable
2-3	Disable *

Note : * factory setting

SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit.

Connector	Function
P1	Hardware reset connector
P2	Speaker connector
P3	Turbo switch connector
P4	Turbo LED connector
P5	Power LED & Ext-Lock connector
P6, P7	Power supply connector
P8	External battery connector
KB1	Keyboard connector

Pin assignments of the connectors are illustrated as follows:

P 1 - Hardware Reset Connector

Pin	Assignment
1	Selection Pin
2	Ground

P 2 - Speaker Connector

Pin	Assignment
1	Data out
2	+5 Vdc
3	Ground
4	+5 Vdc

P 3 - Turbo Switch Connector

Pin	Assignment
1	Selection Pin
2	Ground

P 4 - Turbo LED Connector

Pin	Assignment
1	+5 Vdc
2	LED signal

P 5 - Power LED & Ext-Lock Connector

Pin	Assignment
1	+5 Vdc
2	Key
3	Ground
4	Keyboard inhibit
5	Ground

P6, P7 - Power Supply Connector

Pin	Assignment
1	POWERGOOD
2	+5 Vdc
3	+12 Vdc
4	-12 Vdc
5	Ground
6	Ground

Pin	Assignment
1	Ground
2	Ground
3	-5 Vdc
4	+5 Vdc
5	+5 Vdc
6	+5 Vdc

P 8 - External Battery Connector

Pin	Assignment
1	+ Vdc
2	not used
3	Ground
4	Ground

KB 1 - Keyboard Connector

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 Vdc

Chapter 4
Technical Information

This section provides technical information about OCTEK Jaguar-386 and is intended for advanced users interested in the basic design and operation of OCTEK Jaguar-386.

MEMORY MAPPING

Address	Range	Function
000000-7FFFFF	000K-512K	System Board Memory (512K)
080000-09FFFF	512K-640K	System Board Memory (128K)
0A0000-0BFFFF	640K-768K	Display Buffer (128K)
0C0000-0DFFFF	768K-896K	Adaptor ROM / Shadow RAM (128K)
0E0000-0EFFFF	896K-960K	System ROM / Shadow RAM (64K)
0F0000-0FFFFF	960K-1024K	System BIOS ROM / Shadow RAM (64K)
100000-7FFFFF	1024K-8192K	System Memory
800000-FFFFFF	8192K-16318K	System Memory

I/O ADDRESS MAP

I/O Address Map on System Board

I/O address hex 000 to 0FF are reserved for the system board I/O.

ADDRESS (HEX)	DEVICE
000-01F	DMA Controller 1, 8237
020-03F	Interrupt Controller 1, 8259, Master
040-05F	Timer, 8254
060-06F	Keyboard Controller
070-07F	Real Time Clock, NMI (non-maskable interrupt) mask
080-09F	DMA Page Register, 74LS612
0A0-0BF	Interrupt Controller 2, 8259
0C0-0DF	DMA Controller 2, 8237
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor Port

I/O address hex 100 to 3FF are available on the I/O channel.

ADDRESS (HEX)	DEVICE
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

SYSTEM TIMERS

OCTEK Jaguar-386 has three programmable timer/counters controlled by 82C206 and they are defined as channels 0 through 2 :

Channel 0	System Timer
Gate 0	Tied on
Clk in 0	1.190 Mhz OSC
Clk out 0	8259 IRQ 0

Channel 1	Refresh Request Generator
Gate 1	Tied on
Clk in 1	1.190 Mhz OSC
Clk out 1	Request Refresh Cycle

Channel 2	Tone Generation of Speaker
Gate 2	Controlled by bit 0 of port hex 61 PPI bit
Clk in 2	1.190 Mhz OSC
Clk out 2	Used to drive the speaker

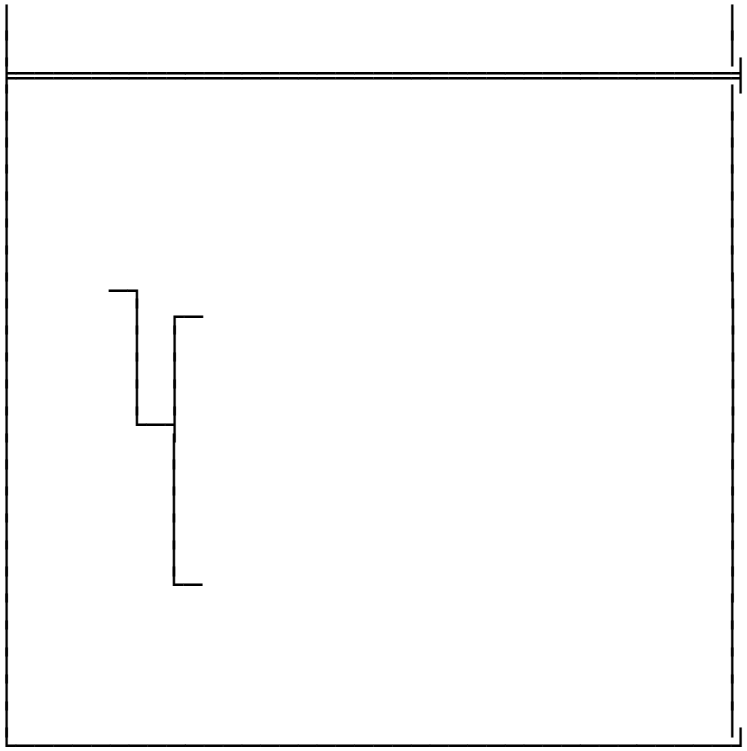
Note :Channel 1 is programmed to generate a 15-micro-second period signal.

The 8254 Timer/Counters are treated by system programs as an arrangement of four programmable external I/O ports. Three are treated as counters and the fourth is a control register for mode programming.

SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK Jaguar-386. The following shows the interrupt-level assignments in decreasing priority.

Level		Function
Microprocessor NMI		Parity or I/O Channel Check
Interrupt Controllers		
CTLR 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1



DIRECT MEMORY ACCESS (DMA)

OCTEK Jaguar-386 supports seven DMA channels.

Channel	Function
0	Spare (8 bit transfer)
1	SDLC (8 bit transfer)
2	Floppy Disk (8 bit transfer)
3	Spare (8 bit transfer)
4	Cascade for DMA Controller 1
5	Spare (16 bit transfer)
6	Spare (16 bit transfer)
7	Spare (16 bit transfer)

The following shows the addresses for the page register.

Page Register	I/O Address (HEX)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

REAL TIME CLOCK AND CMOS RAM

Real time clock and CMOS RAM are contained on board. Real time clock provides the system date and time. CMOS RAM stores system information. Both are backed up by battery and will not lose information after power off. The following page shows the CMOS RAM Address Map.

CMOS RAM ADDRESS MAP

Addresses	Description
00-0D	* Real-time clock information
0E	* Diagnostic status byte
0F	* Shutdown status byte
10	Diskette drive type byte - drives A and B
11	Reserved
12	Fixed disk type byte - drives C and D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	* Low expansion memory byte
31	* High expansion memory byte
32	* Date century byte
33	* Information flags (set during power on)
34-3F	Reserved

REAL TIME CLOCK INFORMATION

The following table describes real-time clock bytes and specifies their addresses.

Byte	Function	Address
0	Seconds	00
1	Second alarm	01
2	Minutes	02
3	Minute alarm	03
4	Hours	04
5	Hour alarm	05
6	Day of week	06
7	Date of month	07
8	Month	08
9	Year	09
10	Status Register A	0A
11	Status Register B	0B
12	Status Register C	0C
13	Status Register D	0D

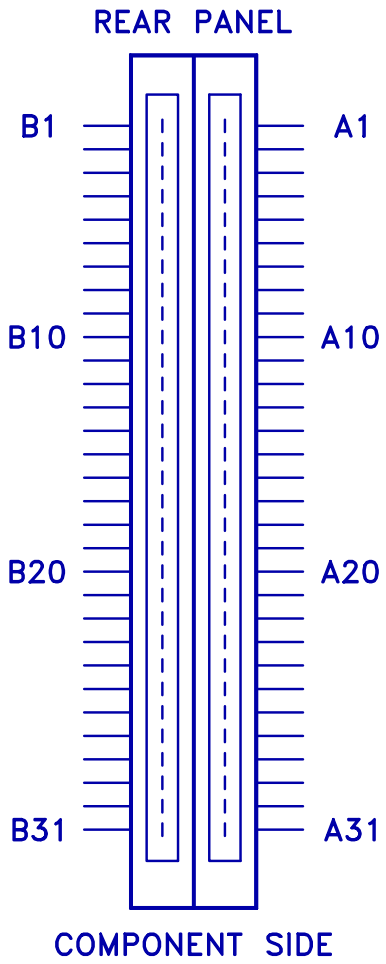
SYSTEM EXPANSION BUS

OCTEK Jaguar-386 provides eight 16-bit slots.

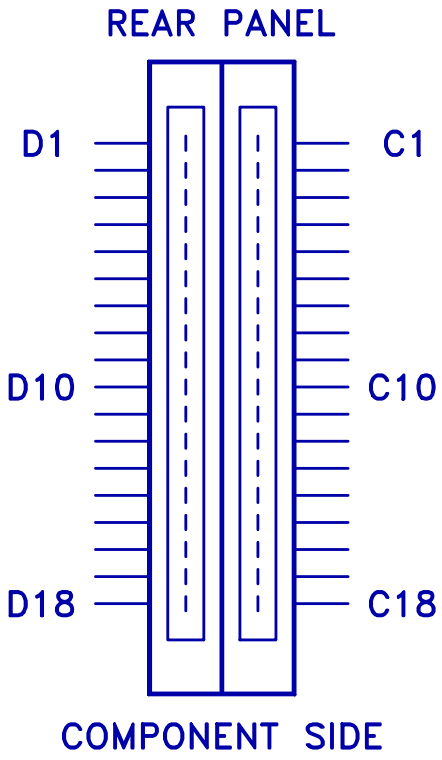
The I/O channel supports:

* I/O address space from hex 100 to hex 3FF
* Selection of data access (either 8 or 16 bit)
* 24 bit memory addresses (16MB)
* Interrupts
* DMA channels
* Memory refresh signal

The following figure shows the pin numbering for I/O channel connectors JA1 to JA7.



The following figure shows the pin numbering for I/O channel connectors JB1-JB6.



The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

I/O Pin	Signal Name	I/O
A1	-I/O CH CK	I
A2	SD7	I/O
A3	SD6	I/O
A4	SD5	I/O
A5	SD4	I/O
A6	SD3	I/O
A7	SD2	I/O
A8	SD1	I/O
A9	SD0	I/O
A10	-I/O CH RDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Channel (B-Side)

I/O Pin	Signal Name	I/O
B1	GND	Ground
B2	RESET DRV	I
B3	+5 Vdc	Power
B4	IRQ9	I
B5	-5 Vdc	Power
B6	DRQ2	I
B7	-12 Vdc	Power
B8	0WS	I
B9	+12 Vdc	Power
B10	GND	Ground
B11	-SMEMW	O
B12	-SMEMR	O
B13	-IOW	I/O
B14	-IOR	I/O
B15	-DACK3	I
B16	DRQ3	O
B17	-DACK1	I
B18	DRQ1	O
B19	-Refresh	I/O
B20	CLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	-DACK2	O
B27	T/C	O
B28	BALE	O
B29	+5 Vdc	Power
B30	OSC	O
B31	GND	Ground

I/O Channel (C-Side)

I/O Pin	Signal Name	I/O
C1	SBHE	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	-MEMR	I/O
C10	-MEMW	I/O
C11	SD8	I/O
C12	SD9	I/O
C13	SD10	I/O
C14	SD11	I/O
C15	SD12	I/O
C16	SD13	I/O
C17	SD14	I/O
C18	SD15	I/O

I/O Channel (D-Side)

I/O Pin	Signal Name	I/O
D1	-MEM CS16	I
D2	-I/O CS16	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	-DACK0	O
D9	DRQ0	I
D10	-DACK5	O
D11	DRQ5	I
D12	-DACK6	O
D13	DRQ6	I
D14	-DACK7	O
D15	DRQ7	I
D16	+5 Vdc	Power
D17	-MASTER	I
D18	GND	Ground

THIS IS INTENTIONALLY LEFT BLANK

Appendix A
System BIOS

The system BIOS provides an interface for operating systems and applications to access hardware. It is fully compatible with standard AT BIOS and works in the network system. It also performs self-test after reset and includes a setup program to setup the system.

SELF-TEST

To ensure the computer hardware is functional, the system BIOS will carry out a self-test upon reset. The test is very intensive and covers all parts of hardware. It takes a while before some messages are shown on the screen. It does not mean that the system is not working when the screen is blank. So wait for a while after turning on the power and listen carefully to the speaker. Some errors are reported by a number of beep sounds. After completing the self-test, the BIOS will display some messages on the screen.

Unlike most of the tests which take a short time, the memory test may be very slow, especially when the memory size is large. Therefore the system BIOS allows you to bypass the memory test by pressing 'ESC'. The following message will be shown during memory test :

Press <ESC> Key to bypass MEMORY test

It is recommended to complete the memory test. The total memory size is displayed after the memory test.

In case of serious errors, the BIOS will suspend the test. If the display is not initialized, the BIOS will report the error through a sequence of beep sounds. Otherwise, error message will be shown on the screen.

There are two types of errors reported by beep sounds. One is conveyed as one long beep followed by a number of short beeps. The meanings of the errors are as below :-

Short Beep Count	Meaning
3	Memory Failure
8	Display Adapter Failure

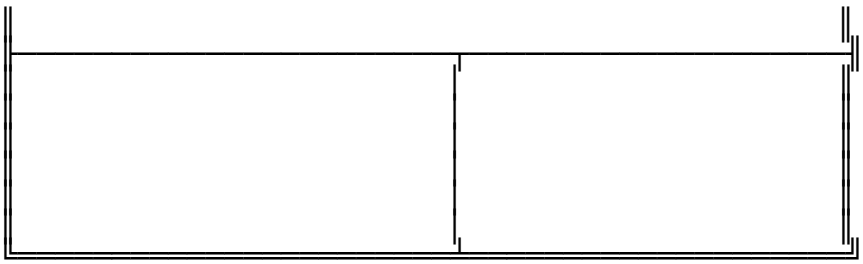
The other type of errors are serious failure and are conveyed as a number of beep and repeated infinitely.

Beep Count	Meaning
1	DRAM Refresh Failure
3	Base 64K Byte Memory Failure
4	System Timer Failure
5	Processor Failure
6	Keyboard Controller - Gate A20 Failure
7	Virtual Mode Exception Error
9	ROM-BIOS Checksum Failure

If no error is found during self-test, the system BIOS will proceed to boot from floppy disk or hard disk. The system BIOS will list the system configuration on the screen as below.

System Configuration (C) Copyright 1985-1990, American Megatrends Inc.,

Main Processor	:	80386	Base Memory Size	:	640 KB
Numeric Processor	:	None	Ext. Memory Size	:	7424 KB
Floppy Drive A:	:	1.2 MB, 5¼"	Hard Disk C: Type	:	2
Floppy Drive B:	:	1.44MB, 3½"	Hard Disk D: Type	:	None
Display Type	:	VGA or EGA	Serial Port(s)	:	None
ROM-BIOS Date	:	04/30/90	Parallel Port(s)	:	3BC



Do check the list to make sure that the configuration is correct. Sometimes, problems arise because of the incorrect information of the configuration. For example, if you forget to modify the setup after changing the floppy disk drive from one type to another, it can not boot from floppy disk or may not work properly. If you check the list, you can find the cause of the problem.

SYSTEM SETUP

The BIOS incorporates two setup sections:

(1) CMOS SETUP
(2) EXTENDED SETUP PROGRAM

It is important that all the setup procedures should be completed before operating the system. Otherwise, the system will not run properly with the incorrect setup information. Run the setup again if the configuration is changed.

To enter the setup section, press 'Del' when the following message is shown :

Press <Del> if you want to run SETUP/EXTD-SET

Whenever the system BIOS finds that the configuration of the system is altered, error message will be shown and you may press 'F1' to run setup. Then the following messages are shown on the screen.

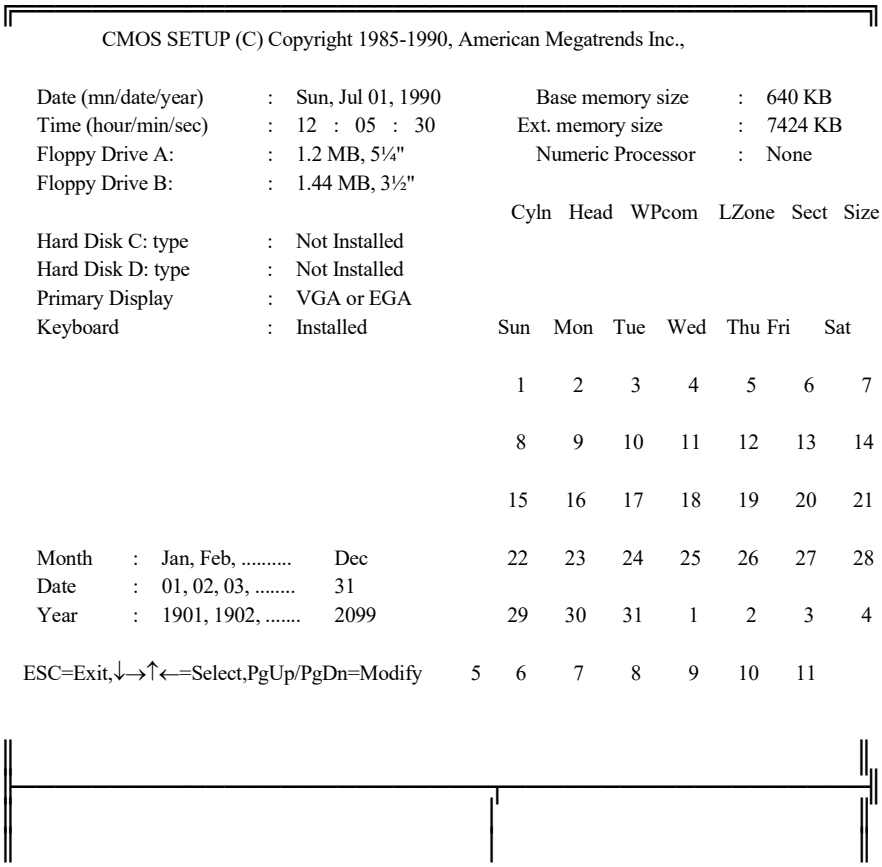
EXIT FOR BOOT
RUN CMOS SETUP
RUN EXTD SETUP

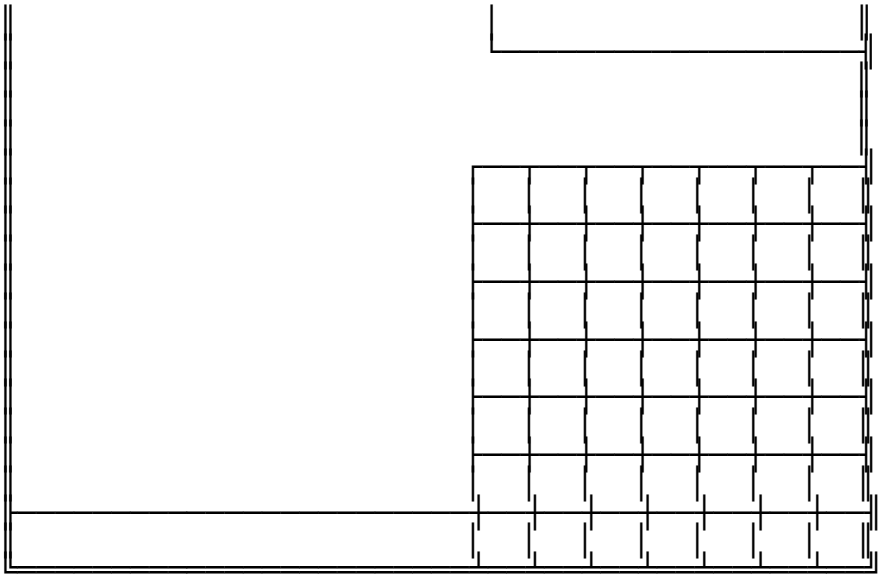
In CMOS SETUP section, you can enter system configuration information which will be stored in CMOS RAM on the motherboard. The information includes the devices of the system as well as memory size.

EXTENDED SETUP allows you to modify the registers of the chipsets. These registers are programmed with default settings by the BIOS. You may change the settings to improve the system performance or to suit the system configuration. Improper settings of the registers may cause the system malfunction. Consult your dealer if you have any doubt.

(1) CMOS SETUP

The memory size and the numeric processor are detected by the BIOS. So you are only required to set those options on the left side of the screen. The system configuration information are shown as follows:





OPTION 1 TIME AND DATE

Use PgUp and PgDn keys to change the value. The date and time cannot be entered directly. An calender is displayed on the lower right corner of the screen for your reference.

OPTION 2 FLOPPY DISK DRIVE

Four types of floppy disk drives are supported:

1. 5-¼ inch standard drive (360K)
2. 5-¼ inch high-density drive (1.2M)
3. 3-½ inch standard drive (720K)
4. 3-½ inch high-density drive (1.44M)

The system BIOS supports two floppy disk drives and they are recognized as drive A and B. Select the correct types. Otherwise the drives cannot work properly. If one of them is not installed, select 'Not Installed' for that drive.

The BIOS is able to detect the type of the drives automatically. But remember to check the settings before exit.

OPTION 3 FIXED DISK DRIVE

There are 47 types of fixed disks supported by the BIOS. Consult your fixed disk manual to determine its correct type. The parameters such as cylinder number, head number, sector number and pre-compensation must match your fixed disk's parameters.

Use PgUp and PgDn keys to change the fixed disk type. If the type of your fixed disk is not included in the hard disk list, define a new type as type 47. Use left and right arrow keys to move between the parameter fields and enter the parameters. The parameters will be stored in the CMOS RAM and your fixed disk can be used afterwards. Each hard disk can be assigned a different type 47 hard disk. So two hard disks which are not included in the list can be used together in your system.

If the type of fixed disk is wrong, it takes a while before the BIOS can identify the error. After setting the fixed disk type, if the system halts after reboot, please wait for a while. It is most likely that the setting of fixed disk type is incorrect.

When you install a new hard disk, make sure whether it is already formatted. If not, the BIOS has to check for a while before reporting the hard disk error. In fact, the error arises only because the hard disk is not formatted. If the hard disk is formatted, you can run DOS FDISK and DOS FORMAT.

Some fixed disks are specially handled and must be set to 'Not Installed'. Consult the fixed disk manual for details.

OPTION 4 DISPLAY

Four types of display are supported:

1. CGA 80 column mode
2. CGA 40 column mode
3. EGA and VGA
4. Monochrome

If the type of display is incorrect, the BIOS will prompt you and ask you to set up again. But the BIOS is still able to display messages on the display attached to the system. Thus you can enter the setup program.

The jumper JP8 must be set according to this setting. Otherwise, the BIOS will report error after self-test.

OPTION 5 KEYBOARD

If a keyboard is attached to the system, select 'Installed'. The BIOS will test the keyboard during self-test.

(2) EXTENDED SETUP PROGRAM

All the registers of the chipsets are set to default values by the system BIOS. Usually, there is no need to modify these registers unless the configuration is changed. Since improper settings of these registers may cause the system malfunction, check your settings carefully before exit.

In EXTENDED SETUP PROGRAM, the main menu is shown as below:

SIS 386 Chipset Setup Program Main Menu
Extended Setup SIS 386 Chipset Write CMOS Register Exit Do Not Write CMOS Register and Exit

Select 'Write CMOS register and exit' to save the new settings in the CMOS RAM. The BIOS will then reboot the system and the new settings are in effect afterwards.

After changing the registers' settings, test your system first to make sure that the settings are correct. It is possible that your system becomes unstable and you need to setup the registers again.

EXTENDED SETUP SIS 386 CHIPSET

In Extended Setup Program, the menu is shown as below :

In this section, you simply use the left and right arrow keys to move between options and press PgUp/PgDn to scroll bit value. After you finish the Setup, press `Esc' to return to main menu. The BIOS will set the registers accordingly.

SIS 386 EXTENDED SETUP PROGRAM Ver - 1.00, 1990, American Megatrends Inc.

	BITS 7 - 0		
85C310	00H ->	0 0 0 0 0 RR0 Go to Prev/Next Register	- ↑↓
	01H ->	1 1 0 0 RRRR Go to Prev/Next Entry	-
			Scroll Bit Value - PgUp/PgDn
85C320	00H ->	R R R 0 0 0 0 0 Return to MAIN MENU	- <ESC>

CLOCK ENABLE/DISABLE

0 -> CACHE DISABLE
1 -> CACHE ENABLE

(1) Cache Enable/Disable

0 ->Cache disable *
1 ->Cache enable

The cache controller is incorporated in the chipset and can be enabled or idsabled. If disabled, the performance will be very low.

(2) Cache Size

00 -> No cache selected *
01 -> 32K cache
10 -> 64K cache and above
11 -> 128 byte internal cache

For 32K, 64K and 128 byte, it must set the jumper in suitable position, otherwise, it may cause the system malfunction. If you select the wrong cache size, it will hang up during boot up. You may clear the CMOS content by JP7 and re-enter the Extended Setup Program.

(3) Cache Write Wait State

0 ->1 wait state *
1 ->0 wait state

The following table shows the speed rating of SRAM in 25MHz and 33MHz.

Operation Speed	0 Wait State
25MHz	35ns
33Mhz	25ns

(4) Shadow RAM Option

00 -> 64K AT F0000 *
01 -> 64K AT C0000, 64K AT F0000
10 -> 128K AT E0000, C0000 AT E0000
11 -> Reserved

There are three options of shadow RAM for different system configuration. For the option 00, the content of the system at F000H segment BIOS is copied to the on board memory. For the option 01, both the system ROM and video ROM at C0000H segment are copied to memory. If you install an add-on card which has a ROM at E000H, you may select option 10 to shadow this ROM as well as the system BIOS. If there is any problem after enabling the shadow memory on the add-on

card, it recommends to enable the shadow RAM function for system BIOS only.

(5) Page Mode Enable/Disable

0 ->Disable *
1 ->Enable

The page mode feature is advanced for the system DRAM. It provided higher performance over conventional DRAM access. The page is enabled by using the page-mode RAM as required.

(6) Shadow RAM Enable/Disable

0 ->Disable *
1 ->Enable

If enabled, the content of the system BIOS is copied to the on board memory and thus the operation of the system BIOS is speeded up.

(7) DRAM CMOS Wait State

00 -> 2 Wait State *
01 -> 1 Wait State (25MHz only)
10 -> Reserved
11 -> 3 Wait State

The number of wait state for memory read and write operations depends on the clock speed of CPU and the speed rating of the DRAM. The following table shows the recommended speed ratings. To ensure the stability of the system, select DRAM equivalent to or better than these ratings.

	Number of wait state		
CPU speed	1	2	3
25 Mhz	70ns	80ns	100ns

	Number of wait state	
CPU speed	2	3
33 Mhz	70ns	100ns

Check carefully whether your DRAM is suitable for the number of wait states you want to select. Improper setting can make the system unstable. The DRAM timing is tight at 33Mhz or at zero wait state. Since the specification of DRAM from different manufacturers may vary, you would better consult your local dealer for the detail information.

(8) DMA CLK Selection

0 ->7.195MHz *
1 ->4.773MHz

The standard AT DMA clock is 4.77MHz. The option of 7.195 is used in fast DMA device. In normal operation, it is recommended to use the 4.77MHz clock.

(9) 8-bit/16-bit AT Cycle Wait State

For 8 bit AT Cycle wait state

0 ->4 Wait State *
1 ->5 Wait State

For 16 bit AT Cycle wait state

0 ->1 Wait State *
1 ->2 Wait State

For the standard AT bus, it requires 1ws for 16 bit and 8 bit bus operation to 8 bit drive, take 4 wait state, so cycle time is achieved. The lower I/O device will require more wait to complete cycle.

(10) Bus Clock Speed Selection

00 -> 1/4 System clock *
01 -> 1/3 System Clock
10 -> 1/2 System Clock
11 -> Unused

Bus clock is used by peripherals on the motherboard and slots, such as display and DMA. Bus clock is generated from CPU clock-in and the speed of Bus clock is shown below.

CPU Speed		
ICLK	33 MHz	25 MHz
CLKIN/4	8.25	6.25
CLKIN/3	11.00	8.33
CLKIN/2	16.50	12.50

The system performance can be improved by selecting a higher Bus clock speed. To be compatible with general add-on cards, the Bus clock must be 8.33 MHz or less. There are many old version add-on cards that can only run at the slow speed. so, be careful when you want to set to higher speed.

* Default Setting

Appendix B
Memory Expansion Card

Memory expansion card contains bank 2 and bank 3 of memory. There are 8 SIMM modules on the card and total memory on this card is 8MB. Please refer to Chapter 3 for the configuration of the memory.

After installing the memory card, the system BIOS will determine the type of DRAM and the amount of total memory. There is no need to set any jumper. The system BIOS will prompt you to setup the memory size after re-boot.

However, you should make sure that the memory on the memory expansion board can be used reliably with the current setting of wait state. If there is any problem, increase the number of wait state.

There is a mounting plate on rear of the card. This mounting plate is used to keep the card on the slot firmly. Use a screw to fasten the card to the case.

THIS IS INTENTIONALLY LEFT BLANK

Appendix C
Operation and Maintenance

STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

KEEPING THE SYSTEM COOL

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stably, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

CLEANING THE "GOLDEN FINGER"

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

CLEANING THE MOTHERBOARD

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the mother-board, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

Appendix D
Troubleshooting

POOR PERFORMANCE

If the performance of the system becomes very poor after enabling cache memory, it is likely that the jumper setting for the cache memory is incorrect. Refer to CONFIGURATION OF CACHE MEMORY in the Chapter 3 for the description of the related jumper. Note that if U16 is not installed, there should be no jumper on JP3.

MAIN MEMORY ERROR

After power up, the monitor remains blank, and there are beep sounds indicating a main memory failure. In this case, turn off the power and remove all SIMM modules. Carefully place the modules back to the sockets and make sure that all the modules are locked by the locking latches firmly.

In some other cases, the total memory found by the BIOS is different from the actual amount of memory on board. (Note that 128K bytes memory is reserved for the shadow RAM function and will not be counted by the BIOS). It is also a memory failure and you can follow the instruction above.

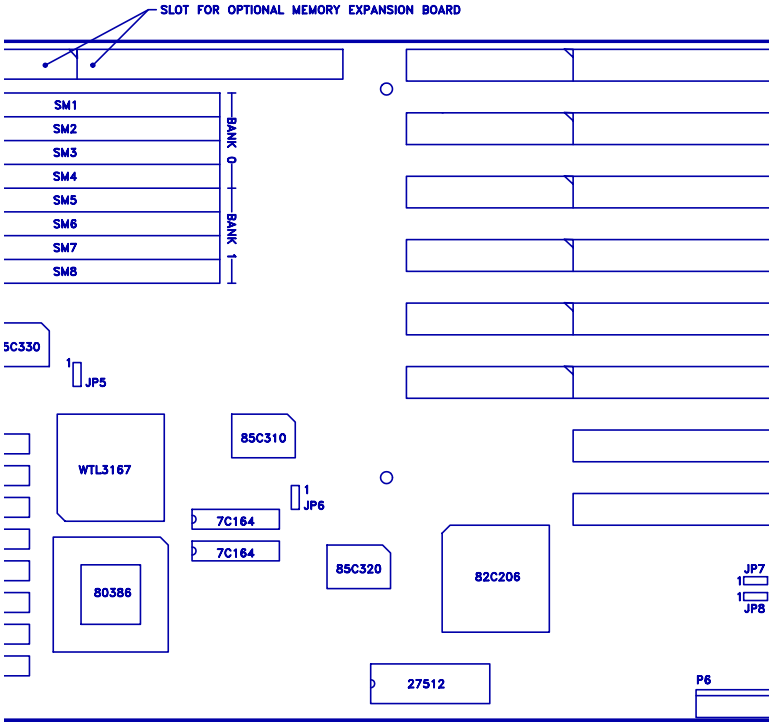
CACHE MEMORY FAILURE

If the system hangs after memory test, it is likely that the cache memory has some problems. May be some of the SRAMs are damaged or the contact of the IC pins is poor. Try to press the SRAM to make sure that the SRAMs are inserted in the sockets, or examine the SRAM to see whether any pins are bent under or out. If the bent pins are found, remove the SRAM, straighten the pin and place the SRAM again. You may also check the BIOS setup of the cache configuration. If the cache controller is enabled, you should select chipset's cache controller. Otherwise, the system will fail.

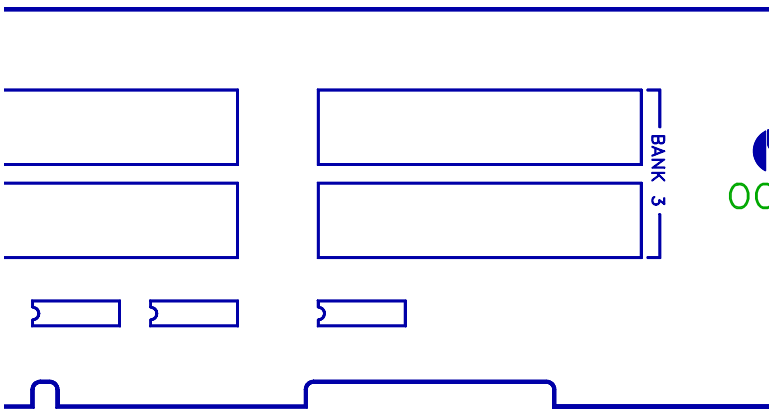
IMPROPER SETTING OF WAIT STATE

If the system hangs after memory test, another possible cause is the improper setting of the wait state for memory operation. The number of wait state must match the speed of the DRAM. Reset the CMOS RAM and set up the wait state. Try to increase the number of wait state.

Appendix E
System Board Layout


SLOT FOR OPTIONAL MEMORY EXPANSION BOARD
SM1
SM2
SM3
SM4
SM5
SM6
SM7
SM8
BANK 0
BANK 1
5C330
1
JP5
WTL3167
85C310
1
JP6
7C164
7C164
80386
85C320
82C206
JP7
1
1
JP8
27512
P6

Appendix F
Memory Expansion Card Layout



33MHz Jaguar 386DX

Supplementary Note

==========

The following table is used to make the 33MHz Jaguar 386DX Mainboard operating in different configuration.

Configuration CMOS Setup	128Byte Internal Cache	32K Cache	64K Cache
Cache Enable/Disable	1 = Enable	1 = Enable	1 = Enable
Cache Size	11 = without Cache RAM	01 = SRAM install in U3, U5, U7 & U9	10 = SRAM install in U2 - U9
Cache Wait State	1 = 0 ws	1 = 0 ws	1 = 0 ws
Page Mode	1 = Enable	1 = Enable	1 = Enable
Shadow RAM Enable/Disable	1 = Enable	1 = Enable	1 = Enable