# HIPPO VL+ 486

The material in this manual is for information only and is subject to change without notice.

**REVISION: 3.0** 

IBM, IBM PC/XT/AT, PC-DOS, MS-DOS, OS/2, INTEL, AMI ARE THE TRADEMARKS OR REGISTERED TRADEMARKS OF THEIR RESPECTIVE OWNERS.

# **RADIO FREQUENCY INTERFERENCE STATEMENT**

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference with radio and television reception.

If this equipment does cause interference to radio or TV reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- \* Reorient the receiving antenna.
- \* Relocate the computer away from the receiver.
- \* Move the computer away from the receiver.
- \* Plug the computer into a different outlet so that computer and receiver are on different branch circuits.
- \* Ensure that card slot covers are in place when no card is installed.
- \* Ensure that card mounting screws, attachment connector screws, and ground wires are tightly secured.
- \* If peripherals are used with this system, it is suggested to use shielded, grounded cables, with in-line filters if necessary.

If necessary, the user should consult the dealer service representative for additional suggestions.

The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

- □ Electronic components are sensitive to dust and dirt. Do inspect and clean the computer system regularly.
- □ Turn off the power whenever you install or remove any connector, memory module and add-on card. Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.
- □ After power is on, wait for a minute. The system BIOS are going through a self-test during this period and nothing is shown on the screen. After the self-test, the system BIOS will initialise the display adaptor and show messages.
- □ The SIMM sockets are fragile device. Do not force the SIMM modules into the sockets. It may break the locking latches.

The manual provides information about the installation and maintenance of OCTEK HIPPO VL+ motherboard. In-depth explanations of the functions of this motherboard are provided. In the appendix, the system BIOS setup is explained.

The content in this manual is only for reference and is intended to provide the basic information for the general users. There are also technical information for hardware and software engineers.

In this manual, there are 4 chapters. Chapter 1 contains a brief introduction and specification of OCTEK HIPPO VL+ motherboard. In the Chapter 2, the functions of OCTEK HIPPO VL+ are explained. It also outlines many advanced features of the CPU and the system architecture. Chapter 3 explains the installation of coprocessor, DRAM modules and jumpers. Technical information is provided in the Chapter 4.

System BIOS is described in the attached BIOS Manual. Additional information is given in the Appendix B and C for maintenance purpose.

## Chapter 1 INTRODUCTION

## Chapter 2 **GENERAL FEATURES**

| Specification             | 2-1  |
|---------------------------|------|
| Processor                 | 2-3  |
| Dynamic Cache Accelerator | 2-8  |
| (DCA)                     |      |
| Memory System             | 2-9  |
| 8042 Emulation            | 2-12 |

# Chapter 3 CONFIGURING THE SYSTEM

| Installing processor         | 3-1 |
|------------------------------|-----|
| Installing RAM Modules       | 3-3 |
| Configuration of Memory      | 3-4 |
| DRAM Configuration           | 3-5 |
| Control of System Speed      | 3-6 |
| Reset CMOS Setup Information | 3-6 |
| System Board Jumper Setting  | 3-7 |
| System Board Connectors      | 3-8 |

## Chapter 4 TECHNICAL INFORMATION

| Memory Mapping               | 4-1  |
|------------------------------|------|
| I/O Address Map              | 4-2  |
| System Timers                | 4-4  |
| System Interrupts            | 4-6  |
| Direct Memory Access (DMA)   | 4-7  |
| Real Time Clock and CMOS RAM | 4-8  |
| CMOS RAM Address Map         | 4-9  |
| Real Time Clock Information  | 4-10 |
| System Expansion Bus         | 4-11 |

# Appendix A OPERATION AND MAINTENANCE

| Static Electricity           | A-1 |
|------------------------------|-----|
| Keeping The System Cool      | A-1 |
| Cleaning The `Golden Finger' | A-2 |
| Cleaning The Motherboard     | A-2 |

### Appendix B TROUBLESHOOTING

| Main Memory Error              | B-1        |
|--------------------------------|------------|
| Improper Setting of Wait State | <b>B-1</b> |

## Appendix C SUMMERY OF JUMPER SETTING

#### Appendix D SYSTEM BOARD LAYOUT

#### **SPECIFICATION**

- Processor : 80486DX, 80486DX2, 80486SX or 80486SX CPU
- Speed : Turbo/normal speed

I/O Slot : Compatible to standard AT bus Six 16-bit slots Three VESA VL-BUS slots

- Cache : 8KB four way set associative internal cache
- Memory : 4 level deep write buffer with byte gathering Shadow RAM for system and video BIOS Page mode and hidden refresh Flexible configuration SIMM sockets for 256KB, 1MB or 4MB modules

System Support Functions :

- 8-Channel DMA (Direct Memory Access)
- 16-level interrupt
- 3 programmable timers
- CMOS RAM for system configuration
- Real time clock with battery back-up
- Fast A20 gate and fast reset

Other Features :

- On board POWERGOOD generation
- External battery connector

### **CPU SUPPORT**

DX/SX and DX2 CPUs are supported at 25/33MHz clock speed. The processoer can be upgraded to Overdrive CPU, P24T and other upgradeable processors operating at 25/33MHz. Jumper settings need to be adjusted and BIOS will automatically set up appropriate system parameters.

A heatsink with fan is recommended when using 50MHz & 66MHz CPU to improve heat dissipation. A +5V header located beside the CPU socket provides power for a +5V fan.

#### **VESA LOCAL BUS**

VESA local bus standard is defined by the Video Electronics Standards Association (VESA) to establish a high speed data path for PC system. It is a 32-bit wide bus running at CPU clock speed, much faster than the standard 8MHz 16-bit ISA bus. Performance is greatly improved for VGA display and mass storage operations. Bus mastering is supported to allow peripheral to become the master of the system and to transfer data under its own control. Some SCSI controllers and LAN controllers make use of bus mastering. They can be plugged in the MASTER slots. VGA cards and IDE controllers are slave devices and can be installed into all VL-bus slots.

#### ON BOARD I/O

XXXX includes an local bus IDE controller, floppy disk controller, serial ports, parallel port and game port.

## DYNAMIC CACHE ARCHITECTURE (DCA)

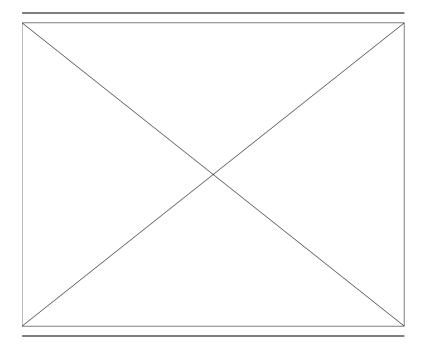
DCA (dynamic Cache Architecture) is a new Cache Memory DCA literally boosts the cache memory efficiency by as much as 300 percent over conventional external cache! It is integrated as part of the high speed logic of the motherboard.

A 486 system, until now, moves information in the same manner because the software written to take full advantage of the 486's 32 bit wide BUS has usually been restricted to CAD/CAM, Expert Systems, Virtual Simulations and other High End applications. DCA, and it's Byte Gathering Write Buffers collect 8 and 16 bit "packets" of information until a single 32 bit "packet" is formed. Using Burst Mode, it then "Writes" this single informational "string" back to RAM in one operation, rather than in several time consuming ones. This is a tremendous improvement on the efficiency of data transfer, as the information is handled solely through the CPU, the High Speed Chipset and the lightning fast Internal Cache of the 80486.

# **Chapter 4 Configuring The System**

## INSTALLING PROCESSOR

There is a 238-pin PGA socket. To install processor, be sure to line up pin 1 of the CPU with pin 1 of the socket as shown below.



Before installing the processor, make sure that all the pins are straight. The pins are very fragile. Once these pins are bent, the processor may be damaged.

#### СРИ Туре

|     | 486DX\DX2 | 486SX | 487SX |
|-----|-----------|-------|-------|
| JP6 | 1 - 2     | 2 - 3 | 1 - 2 |
| JP8 | 2 - 3     | NO    | 1 - 2 |
| JP9 | 2 - 3     | 1 - 2 | 2 - 3 |

System Speed (Only for clock chip version)

|     | 33MHz | 25MHz |
|-----|-------|-------|
| JP4 | 1 - 2 | 2 - 3 |
| JP5 | 1 - 2 | 2 - 3 |

## **INSTALLING RAM MODULES**

OCTEK HIPPO VL+ has eight sockets on board for 30-pins SIMM modules. Whenever you add memory to the motherboard, install four modules at the same time.

To install a module, the module edge is angled into the socket's contact and then the module is pivoted into position, where the locking latches will secure it. If the module edge is not completely inserted into the socket, it cannot be pivoted to be in vertical position and should be dragged out and re-inserted again. Do not force the module into the SIMM socket. It will damage the locking latches.

The modules should be locked by the locking latches of the sockets firmly. Please check carefully before turning on the power. Otherwise, the system will not work properly.

#### **CONFIGURATION OF MEMORY**

The configuration of the memory is very flexible. There are several combinations of DRAM types you may consider. 256KB, 1MB or 4MB SIMM are acceptable. There are two banks of DRAM on the motherboard and another two banks on a memory expansion board. The memory size is detected automatically by system BIOS and indicated during memory test after reset. No jumper is needed to be set for the memory size and DRAM type.

70ns SIMM modules has to be used.

| Bank 0 Simm (1-4) | Bank 1 Simm (5-8) | Total Memory |
|-------------------|-------------------|--------------|
| 256K              |                   | 1M           |
| 256K              | 256K              | 2M           |
| 1M                |                   | 4M           |
| 256K              | 1M                | 5M           |
| 1M                | 1M                | 8M           |
| 4M                |                   | 16M          |
| 1M                | 4M                | 20M          |
| 4M                | 4M                | 32M          |
| 16M               |                   | 64M          |

## **DRAM CONFIGURATION**

SIMM without parity check RAM (x8) is supported. BIOS will detect the presence of the parity check RAM.

#### **CONTROL OF SYSTEM SPEED**

System speed can be controlled by keyboard and turbo switch. To change the speed by keyboard, use `-' and `+' of the numeric keypad. Press `Ctrl' `Alt' and `-' for slow speed and press `Ctrl' `Alt' and `+' for fast speed.

Connect P1 to the turbo switch of the case and P5 to the turbo LED of the case. When the turbo mode is selected, the turbo LED of the case will be turned on.

Whenever the system speed is set to be slow by turbo switch, it cannot be changed by the keyboard, and vice versa.

## **RESET CMOS SETUP INFORMATION**

Sometimes, the improper setting of system setup may make the system malfunction. In this case, turn off the power and set JP10 to 2-3 for a while. The internal CMOS status register is reset. Then set the jumper to 1-2 of JP10 and turn on the power. The BIOS finds the CMOS status register is reset and regards the setup information is invalid. So it will prompt you to correct the information.

#### SYSTEM BOARD JUMPER SETTING

There are several options which allows user to select by hardware switches.

**Display Selection** 

| JP7 |                      |
|-----|----------------------|
| 1-2 | CGA, EGA, VGA        |
| 2-3 | Monochrome display * |

## SYSTEM BOARD CONNECTORS

Under typical conditions, these connectors should be connected to the indicators and switches of the system unit. The functions of connectors on the motherboard are listed below.

|       | Description                    |
|-------|--------------------------------|
| P1    | Turbo switch                   |
| P2    | Speaker connector              |
| P3    | Hardware reset connector       |
| P4    | Power LED & Ext-lock connector |
| P5    | Turbo LED                      |
| P6,P7 | Power supply connector         |
| P8    | External battery connector     |
| P9    | Cooling fan connector          |
| KB1   | Keyboard connector             |

Pin assignment of the connector are illustrated as follows:

P1 - Turbo Switch Connector

| Pin | Assignment              |
|-----|-------------------------|
| 1 2 | Selection Pin<br>Ground |

## P2 - Speaker Connector

| Pin | Assignment |
|-----|------------|
| 1   | Data out   |
| 2   | +5 Vdc     |
| 3   | Ground     |
| 4   | +5 Vdc     |

P3 - Hardware Reset Connector

| Pin | Assignment    |
|-----|---------------|
| 1   | Selection Pin |
| 2   | Ground        |

P4 - Power LED & Ext-Lock Connector

| Pin | Assignment       |
|-----|------------------|
| 1   | +5 Vdc           |
| 2   | Key              |
| 3   | Ground           |
| 4   | Keyboard inhibit |
| 5   | Ground           |

P5 - Turbo LED Connector

| Pin | Assignment |
|-----|------------|
| 1   | +5Vdc      |
| 2   | LED signal |

P6,P7 - Power Supply Connector

| Pin | Assignment |
|-----|------------|
| 1   | POWERGOOD  |
| 2   | +5 Vdc     |
| 3   | +12 Vdc    |
| 4   | -12 Vdc    |
| 5   | Ground     |
| 6   | Ground     |

| Pin | Assignment |
|-----|------------|
| 1   | Ground     |
| 2   | Ground     |
| 3   | -5 Vdc     |
| 4   | +5 Vdc     |
| 5   | +5 Vdc     |
| 6   | +5 Vdc     |

P8 - External Battery Connector

| Pin | Assignment |
|-----|------------|
| 1   | + Vdc      |
| 2   | not used   |
| 3   | Ground     |
| 4   | Ground     |

P9 - Cooling Fan Connector

| Pin | Assignment |
|-----|------------|
| 1   | +5Vdc      |
| 2   | Ground     |

#### KB1 - Keyboard Connector

| Pin | Assignment     |
|-----|----------------|
| 1   | Keyboard clock |
| 2   | Keyboard data  |
| 3   | Spare          |
| 4   | Ground         |
| 5   | +5 Vdc         |

# **Chapter 5 Technical Information**

## SYSTEM INTERRUPTS

Sixteen levels of system interrupts are provided on OCTEK HIPPO VL+. The following shows the interrupt-level assignments in decreasing priority.

| Level                                |  | Function  |
|--------------------------------------|--|---|
| Microprocessor NMI                   |  | Parity or I/O Channel<br>Check  |
| Interrupt Contr                      | ollers   |   |
| CTLR 1                               | CTLR 2   |   |
| IRQ0<br>IRQ1<br>IRQ2                 |  | Timer Output 0<br>Keyboard<br>(Output Buffer Full)<br>Interrupt from CTLR 2   |
|                                      | IRQ8<br>IRQ9<br>IRQ10<br>IRQ11<br>IRQ12<br>IRQ13<br>IRQ14<br>IRQ15 | Real-time Clock Interrupt<br>Software Redirected to<br>INT 0AH (IRQ2)<br>Reserved<br>Reserved<br>Reserved<br>Coprocessor<br>Fixed Disk Controller<br>Reserved |
| IRQ3<br>IRQ4<br>IRQ5<br>IRQ6<br>IRQ7 |  | Serial Port 2<br>Serial Port 1<br>Parallel Port 2<br>Diskette Controller<br>Parallel Port 1   |

## DIRECT MEMORY ACCESS (DMA)

OCTEK HIPPO VL+ supports seven DMA channels.

| Channel | Function                     |
|---------|------------------------------|
| 0       | Spare (8 bit transfer)       |
| 1       | SDLC (8 bit transfer)        |
| 2       | Floppy Disk (8 bit transfer) |
| 3       | Spare (8 bit transfer)       |
| 4       | Cascade for DMA Controller 1 |
| 5       | Spare (16 bit transfer)      |
| 6       | Spare (16 bit transfer)      |
| 7       | Spare (16 bit transfer)      |

The following tables summarize pin assignments for the I/O channel connectors.

I/O Channel (A-Side)

| I/O Pin | Signal Name | I/O |
|---------|-------------|-----|
| Al      | -I/O CH CK  | Ι   |
| A2      | SD7         | I/O |
| A3      | SD6         | I/O |
| A4      | SD5         | I/O |
| A5      | SD4         | I/O |
| A6      | SD3         | I/O |
| A7      | SD2         | I/O |
| A8      | SD1         | I/O |
| A9      | SD0         | I/O |
| A10     | -I/O CH RDY | Ι   |
| A11     | AEN         | О   |
| A12     | SA19        | I/O |
| A13     | SA18        | I/O |
| A14     | SA17        | I/O |
| A15     | SA16        | I/O |
| A16     | SA15        | I/O |
| A17     | SA14        | I/O |
| A18     | SA13        | I/O |
| A19     | SA12        | I/O |
| A20     | SA11        | I/O |
| A21     | SA10        | I/O |
| A22     | SA9         | I/O |
| A23     | SA8         | I/O |
| A24     | SA7         | I/O |
| A25     | SA6         | I/O |
| A26     | SA5         | I/O |
| A27     | SA4         | I/O |
| A28     | SA3         | I/O |
| A29     | SA2         | I/O |
| A30     | SA1         | I/O |
| A31     | SA0         | I/O |

I/O Channel (B-Side)

| I/O Pin | Signal Name | I/O    |
|---------|-------------|--------|
| B1      | GND         | Ground |
| B2      | RESET DRV   | Ι      |
| B3      | +5 Vdc      | Power  |
| B4      | IRQ9        | Ι      |
| B5      | -5 Vdc      | Power  |
| B6      | DRQ2        | Ι      |
| B7      | -12 Vdc     | Power  |
| B8      | 0WS         | Ι      |
| B9      | +12 Vdc     | Power  |
| B10     | GND         | Ground |
| B11     | -SMEMW      | О      |
| B12     | -SMEMR      | 0      |
| B13     | -IOW        | I/O    |
| B14     | -IOR        | I/O    |
| B15     | -DACK3      | Ι      |
| B16     | DRQ3        | 0      |
| B17     | -DACK1      | Ι      |
| B18     | DRQ1        | 0      |
| B19     | -Refresh    | I/O    |
| B20     | CLK         | 0      |
| B21     | IRQ7        | Ι      |
| B22     | IRQ6        | Ι      |
| B23     | IRQ5        | Ι      |
| B24     | IRQ4        | Ι      |
| B25     | IRQ3        | Ι      |
| B26     | -DACK2      | 0      |
| B27     | T/C         | О      |
| B28     | BALE        | О      |
| B29     | +5 Vdc      | Power  |
| B30     | OSC         | О      |
| B31     | GND         | Ground |

# I/O Channel (C-Side)

| I/O Pin | Signal Name | I/O |
|---------|-------------|-----|
| C1      | SBHE        | I/O |
| C2      | LA23        | I/O |
| C3      | LA22        | I/O |
| C4      | LA21        | I/O |
| C5      | LA20        | I/O |
| C6      | LA19        | I/O |
| C7      | LA18        | I/O |
| C8      | LA17        | I/O |
| C9      | -MEMR       | I/O |
| C10     | -MEMW       | I/O |
| C11     | SD8         | I/O |
| C12     | SD9         | I/O |
| C13     | SD10        | I/O |
| C14     | SD11        | I/O |
| C15     | SD12        | I/O |
| C16     | SD13        | I/O |
| C17     | SD14        | I/O |
| C18     | SD15        | I/O |

I/O Channel (D-Side)

| I/O Pin | Signal Name | I/O    |
|---------|-------------|--------|
| D1      | -MEM CS16   | Ι      |
| D2      | -I/O CS16   | Ι      |
| D3      | IRQ10       | Ι      |
| D4      | IRQ11       | Ι      |
| D5      | IRQ12       | Ι      |
| D6      | IRQ15       | Ι      |
| D7      | IRQ14       | Ι      |
| D8      | -DACK0      | 0      |
| D9      | DRQ0        | Ι      |
| D10     | -DACK5      | 0      |
| D11     | DRQ5        | Ι      |
| D12     | -DACK6      | О      |
| D13     | DRQ6        | Ι      |
| D14     | -DACK7      | 0      |
| D15     | DRQ7        | Ι      |
| D16     | +5 Vdc      | Power  |
| D17     | -MASTER     | Ι      |
| D18     | GND         | Ground |

The following table summery pin assignments for VESA VL-bus connector.

VL-bus (side A)

| I/O Pin | Signal Name |
|---------|-------------|
| Al      | CD1         |
| A2      | CD3         |
| A3      | GROUND      |
| A4      | CD5         |
| A5      | CD7         |
| A6      | CD9         |
| A7      | CD11        |
| A8      | CD13        |
| A9      | CD15        |
| A10     | GROUND      |
| A11     | CD17        |
| A12     | POWER       |
| A13     | CD19        |
| A14     | CD21        |
| A15     | CD23        |
| A16     | CD25        |
| A17     | GROUND      |
| A18     | CD27        |
| A19     | CD29        |
| A20     | CD31        |
| A21     | CA30        |
| A22     | CA28        |
| A23     | CD26        |
| A24     | GROUND      |
| A25     | CA24        |
| A26     | CA22        |
| A27     | POWER       |
| A28     | CA20        |

VL-bus (side A)

| I/O Pin | Signal Name |
|---------|-------------|
| A29     | CA18        |
| A30     | CA16        |
| A31     | CA14        |
| A32     | CA12        |
| A33     | CA10        |
| A34     | CA8         |
| A35     | GROUND      |
| A36     | CA6         |
| A37     | CA4         |
| A38     | WBACK-      |
| A39     | BEO-        |
| A40     | POWER       |
| A41     | BE1-        |
| A42     | BE2-        |
| A43     | GROUND      |
| A44     | BE3-        |
| A45     | ADS-        |
| A46     | LRDY-       |
| A47     | LDEV-       |
| A48     | LREQ-       |
| A49     | GROUND      |
| A50     | LGNT-       |
| A51     | POWER       |
| A52     | ID2         |
| A53     | ID3         |
| A54     | ID4         |
| A55     | LKEN-       |
| A56     | LEADS-      |

# VL-bus (side B)

| I/O Pin | Signal Name |
|---------|-------------|
| B1      | CD0         |
| B2      | CD2         |
| B3      | CD4         |
| B4      | CD6         |
| B5      | CD8         |
| B6      | GROUND      |
| B7      | CD10        |
| B8      | CD12        |
| B9      | POWER       |
| B10     | CD14        |
| B11     | CD16        |
| B12     | CD18        |
| B13     | CD20        |
| B14     | GROUND      |
| B15     | CD22        |
| B16     | CD24        |
| B17     | CD26        |
| B18     | CD28        |
| B19     | CD30        |
| B20     | POWER       |
| B21     | CA31        |
| B22     | GROUND      |
| B23     | CA29        |
| B24     | CA27        |
| B25     | CA25        |
| B26     | CA23        |
| B27     | CA21        |
| B28     | CA19        |

VL-bus (side B)

| I/O Pin | Signal Name |
|---------|-------------|
| B29     | GROUND      |
| B30     | CA17        |
| B31     | CA15        |
| B32     | POWER       |
| B33     | CA13        |
| B34     | CA11        |
| B35     | CA9         |
| B36     | CA7         |
| B37     | CA5         |
| B38     | GROUND      |
| B39     | CA3         |
| B40     | CA2         |
| B41     | n/c         |
| B42     | RESET-      |
| B43     | D/C-        |
| B44     | M/IO-       |
| B45     | W/R-        |
| B46     | RDY-        |
| B47     | GROUND      |
| B48     | IRQ9        |
| B49     | BRDY-       |
| B50     | BLAST-      |
| B51     | ID0         |
| B52     | ID1         |
| B53     | GROUND      |
| B54     | VLCLK       |
| B55     | POWER       |
| B56     | LBS16-      |

### STATIC ELECTRICITY

When installing or removing any add-on card, DRAM module or coprocessor, you should discharge the static electricity on your body. Static electricity is dangerous to electronic device and can build-up on your body. When you touch the add-on card or motherboard, it is likely to damage the device. To discharge the static electricity, touch the metal of your computer. When handling the add-on card, don't contact the components on the cards or their "golden finger". Hold the cards by their edges.

#### **KEEPING THE SYSTEM COOL**

The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and hard disk drive can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stable, the temperature must be kept at a low level. A easy way to do this is to keep the cool air circulating inside the case. The power supply contains a fan to blow air out of the case. If you find that the temperature is still very high, it would be better to install another fan inside the case. Using a larger case is recommended if there are a number of add-on cards and disk drives in the system.

For very high speed CPU, place a heatsink and fan on the top of the CPU.

### **CLEANING THE "GOLDEN FINGER"**

Whenever inserting an add-on card to the motherboard, make sure that there is no dirt on the "golden finger" of the add-on card. If not, the contact between the "golden finger" and the slot may be poor and thus the add-on card may not work properly. Use a pencil eraser to clean the "golden finger" if dirt is found.

#### **CLEANING THE MOTHERBOARD**

The computer system should be kept clean. Dust and dirt is harmful to electronic devices. To prevent dust from accumulating on the motherboard, installing all mounting plates on the rear of the case. Regularly examine your system, and if necessary, vacuum the interior of the system with a miniature vacuum.

# Appendix B SUMMERY OF JUMPER SETTING

|     | 486DX/DX2 | 486SX | 487SX |
|-----|-----------|-------|-------|
| JP6 | 1-2       | 2-3   | 1-2   |
| JP8 | 2-3       | NO    | 1-2   |
| JP9 | 2-3       | 1-2   | 2-3   |

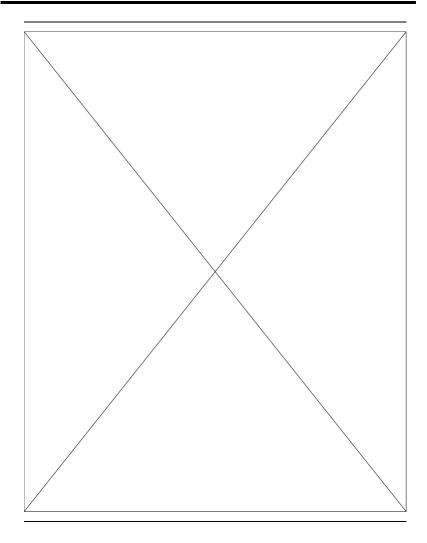
| JP7 |                    |
|-----|--------------------|
| 1-2 | CGA,EGA,VGA *      |
| 2-3 | MONOCHROME DISPLAY |

| JP10 | CMOS CONTAIN  |
|------|---------------|
| 1-2  | NORMAL *      |
| 2-3  | CLEAR / RESET |

|     | 33MHz | 25MHz |
|-----|-------|-------|
| JP4 | 1-2   | 2-3   |
| JP5 | 1-2   | 2-3   |

| RESERVED JUMPER |     |  |
|-----------------|-----|--|
| JP13,14,15      | 2-3 |  |
| JP16            | 1-2 |  |
| JP1             | ON  |  |
| JP3             | OFF |  |

# Appendix C System Board Layout



# HIPPO VL+ BOARD LAYOUT