USER'S MANUAL

HIPPO DCA 2

VESA LOCAL BUS MOTHERBOARD

Hippo DCA2 486

486 VESA Local Bus Motherboard

User's Manual

Version 2.25 December 1994

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Ocean Information Systems, Inc.
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Preface

About the Hippo DCA2

Thank you for purchasing the Hippo DCA2, Ocean Information Systems'new top-of-the-line 486 motherboard. The Hippo DCA2 utilizes DynamiCache, an innovative cache memory technology that takes personal computing to a new level of performance.

DynamiCache was designed to eliminate bottlenecks between the CPU and the memory bank. It does this by replacing traditional DRAM and external L2 cache with a memory bank that runs at CPU speed. With entire memory running at CPU speed the processor can handle multitasking just as easily as it handles single applications.

About the Manual

The content of this manual is for reference only and is intended to provide basic information for the general user. Technical information is also included in the Appendix for hardware and software engineers.

This manual provides information about the installation and maintenance of the Octek Hippo DCA2 motherboard. In-depth explanations concerning the functions and features of this motherboard are provided. Chapter 1 is designed to give the user an overview of DynamiCache, including an in-depth explanation of what it is as well as how it works. Chapter 2 describes the features of the Hippo DCA2 motherboard. It provides important information regarding the main memory system, ISA and VESA slots, the BIOS, and the CPUs supported. Refer to Chapter 3 for instructions on how to setup and install the motherboard. This chapter includes the necessary data for properly setting the pin connectors. Requirements for setting up the BIOS are listed in Chapter 4. An Appendix is also included that provides address maps as well as advanced technical information for hardware and software professionals.

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Chapter 4: BIOS Setup

Appendix: Advanced Technical Information

CHAPTER 1

SYSTEM OVERVIEW

Listed below are answers to some questions you may have about DCA2 and its phenomenal performance.

1.1 What is DCA2 ?

DCA2 (DynamiCache Architecture - 2nd generation) is a high performance cache memory system that alleviates the traditional bottleneck of mainboards. This evolutionary system operates up to four times faster than standard DRAM or external cache based boards. With DCA2 users at last have a means of enhancing their systems without the necessity of processor or external cache upgrades.

1.2 What makes DCA2 so powerful ?

Unlike external cache, which was implemented as a low-cost enhancement to standard DRAM, DCA2 was designed for pure performance. DCA2 transforms the entire memory bank into DynamiCache, a high speed memory that operates at 15ns rather than 70ns.

1.3 What is DynamiCache ?

DynamiCache is a high speed memory module that boosts the entire memory bank so that it operates at the same speed as the CPU clocking rate. The entire memory bank appears as cache to the CPU.

1.4 Why is DCA2 a better choice ?

DCA2 has a far greater impact and offers more benefits dollar for dollar than the best external cache based boards. Programs such as Windows 3.11, OS/2 and Windows NT place extreme stress on external cache based systems, often causing bottlenecks between the CPU and the memory bank. When the cache bank becomes full, the CPU must wait for new instructions to be loaded up from the slower DRAM memory. With DCA2, the

memory operates at the same speed as the CPU, allowing the CPU to retrieve instructions from any location within the main memory at zero wait states.

1.5 Users advantages of DCA2

◊ The entire memory bank acts as if its a cache subsytem.
◊ 15ns memory (standard DRAM only operates at 70ns).
◊ Zero wait states between the CPU and memory.
◊ Up to 200% memory performance increase with applications running in a DOS environment or other 16-bit operating systems.
◊ Up to 400% memory performance increase with applications run in an OS2 and NT environment or other 32-bit operating systems.
◊ DCA2 memory operates at CPU speed, making it four times faster than any other DRAM memory currently on the market.

1.6 Technical advantages of DCA2

◊ 15ns Access Time during Hit Cycle
◊ 15ns Posted Random Writes
◊ 35ns Random Read Access Page Miss
◊ Transparent Refresh during Cache Reads
◊ Hidden DRAM precharge during Page Reads
◊ Consumes 1/3 the power of SRAM plus DRAM solutions
◊ On-board cache Hit/Miss Comparator
◊ Write Posting Register with Direct Path to Memory Array

1.7 DynamiCache Description

The benefits of DynamiCache are easy to understand. New operating systems such as Windows 3.11, Windows NT, OS/2, UNIX and their associated applications generate a new level of high stresses on conventional external caches, preventing the power of these Oss from being fully exploited. Although these operating systems do offer the ability to multitask applications, these features are rarely used in practice as it causes even the best designed L2 cache motherboard to perform at unacceptably low levels. DynamiCache, being able to access any instruction or data string from any physical address in memory at full cache speed, enables the CPU to handle multitasked operations as smoothly as it handles single applications.

1.8 DynamiCache Architecture

The DynamiCache chips are physically similar to a standard 4MB page mode or static column DRAM with the addition of an integrated Row Register Register and an internal controller that allows it to operate much like page mode or static column DRAM. DynamiCache's Row Register register is tightly coupled with the Memory Array. Memory Reads always occur from the Row Register Registers. When the internal comparitor detects a page hit, only the Row Register register is accessed and data is made available in 15ns from the column address. When a page read miss is detected, the new Memory Array row is loaded into the cache and data is available at the output all within a single 35ns access. Subsequent reads within the page (burst read, local instructions or data) can continue at a 15ns cycle time.

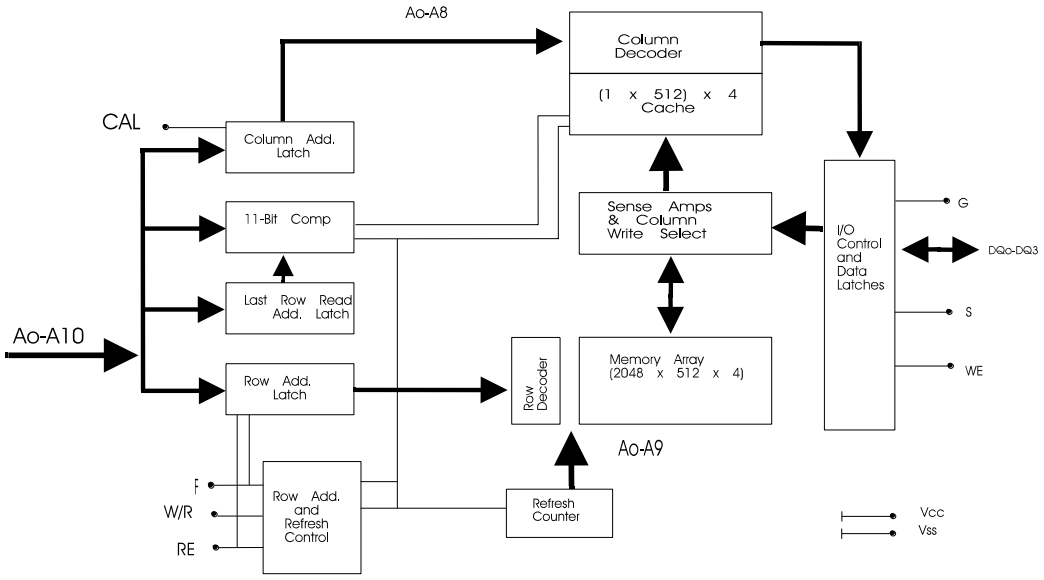

Figure 1

Since reads occur from the Row Register register, the Memory Array Precharge can occur simultaneously without degrading performance. The on chip refresh counter with an independent refresh bus allows the DynamiCache to be refreshed during cache reads. Memory Writes are internally posted in 15 nSecs and are directed to the DRAM array.During a write hit, the on chip comparator activates a parallel write path to the Row Register register to maintain coherency. The DynamiCache delivers 15nSec page mode memory writes. This high level of performance is achieved with a single non-interleaved memory consisting of as few as eight 1M x 4 components or a single 72-pin 4Mbyte DynamiCache module.

1.9 Distributed Cache

DynamiCache uses what is referred to as distributed cache rather than lumped cache. The 15 ns access time is available throughout the entire range of installed DynamiCache, not just in a small external cache. External cache only provides benefit to the system while the instructions are housed in the cache. The penalties that are usually associated with external cache, such as write back latencies, cache thrashings and cache saturation are not present in DynamiCache. This architecture provides all of the cache benefits for the entire range of installed memory with none of the cache penalties.

1.10 DynamiCache Applications

DynamiCache was designed with the new emerging 32-bit protected mode operating systems in mind. External cache, prior to 1994 was an acceptable cost based solution for enhancing DOS applications that typically occupied a memory space that was less than the size of the installed external cache. If the CPU requested an instruction or a string of data, this information was made available to the CPU at cache speed (zero wait state). With the advent of Windows, however, the typical application became larger and much more complex supporting virtual disks, DLLs and GUI interfaces.

1.11 Application Overhead and its effect on External Cache

These new applications subsequently brought with them tremendous overhead for the operating systems. OS/2 and Windows NT were created to handle the demands of the new applications with the hopes that a pre-emptive multitasking, multithreading 32 bit OS would break the bottleneck to productivity. It was quickly found that these operating systems were only effective on high end systems, such as DX2, Pentium or RISC platforms. Even with top end CPUs, a large main DRAM bank was needed, typically 16Mbytes or more and a very expensive L2 cache was often employed, usually 256K to 512K.

1.12 External Cache Saturation Problem

Cache saturation is an easy concept to understand. If the executing program is smaller than the external cache I have installed, then no saturation occurs. There will always be memory address space available for the execution of this program. If the program is slightly larger than my L2 cache, saturation may still not occur, provided that the cache is well designed. There is a point, however, when the L2 cache will remain constantly saturated with instructions. Some of these may be in the process of being read from the main memory and some will be waiting to be written back to memory. The net effect is that if the program

is large enough, the L2 cache is kept filled with data on a continuous basis. It is the maintenance of this traffic flow that dramatically reduces the amount of time the CPU would otherwise have for executing software instructions.

1.13 Dynamicache Excels and External Cache Suffers Under Heavy Processing Loads

Heavy processing loads can easily reduce a 66Mhz CPU and L2 cache combination to effective processing speeds as little as 20% of the CPU's capabilities. A CPU under these circumstances spends as much as 80% of its time squeezing large amounts of data to and from memory through a very small SRAM cache. External cache, under these high stress conditions is kept in a continuous state of flux. This is the point at which a cache mechanism ceases to be effective in providing any benefit to system performance.

This is the state in which the cache has become saturated. If the processing demands from the CPU increase any further, the external cache actually creates a penalty in performance by virtue of it's memory management overhead. DynamiCache does not suffer from these penalties.

1.14 Targeted Operating Environments

DCA2 is designed with the following target operating systems, and application environments:

- ◊ Multitasking Mutlithreding (Windows 3.11, Windows NT, OS/2 2.11, etc.)
- ◊ Large Applications (Desktop publishers, graphic designers, databases/spreadsheets)
- ◊ I/O Intensive computing (Graphics applications, multimedia, disk and data transfers)
- ◊ CPU Bound Computing (CAD/CAM, MATHCad and other scientific number crunchers)
- ◊ Software Compilers
- ◊ Application Servers (Networked applications accessed from a central server)
- ◊ File Servers (Novel, Lantastic, LANManager, Vines)
- ◊ DynamiCache is fully compatible with all the major operating systems and application.

1.15 L2/ DCA2 Cache Efficiency Versus Application Size

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Where do the software applications fit on this curve ?

- Typical Benchmarks usually utilize less than 5% memory load.
- DOS applications typically generate less than 25% memory load.
- Windows 3.11 applications typically generate approximately 50% memory load.
- OS/2 2.11, UNIX and Windows NT easily generate 50% to 100% memory load
- Windows NT Advanced Server and Novell Application Servers routinely use 90% to 100% load.

* Memory Loads do not include virtual disk accesses.

1.16 General Specifications Overview

Processor:

◆ Processor Type	Intel 486SX-25/33, 486DX-25/33, 486DX2-50/66 Intel 486DX4-75/100, Intel P24T AMD 486DX-40, 486DX2-50/66 Cyrix 486DX-33, 486DX2-50/66
◆ Speed	25 / 33 / DX2-50 / DX2-66 / DX4-100
◆ CPU voltage detection	Automatic voltage conversion circuitry

Cache Architecture:

◆ Internal Cache	8KB 4-way set associative cache (SX/DX/DX2) 16KB 4-way set associative cache (DX4)
◆ External Cache	DynamiCache Architecture II (DCA2) running at CPU speed DynamiCache running at 15ns

Memory Subsystem:

◆ DynamiCache Simm sockets	2 x 72 pin 4MB / 8MB / 16MB DynamiCache modules
◆ DRAM Simm sockets	2 x 72 pin 4MB / 8MB / 16MB / 32MB DRAM modules
◆ Max. Memory Size	96MB
◆ Mixed Memory Type	Support mixed DynamiCache / DRAM modules
◆ Memory Width	32-bit DynamiCache & DRAM
◆ Enhancement	Fast Page Mode and Hidden Refresh supported

BIOS Subsystem

◆ BIOS Type	AMI / Microid Research
◆ BIOS Shadowing	Shadow RAM for System and Video BIOS
◆ BIOS Features	Built-in setup, Power-on self test, Drive table optimization, User-definable drive types, Password protection, Shadowing options

Input/Output Subsystem

◆ VESA bus slots	3 x 32-bit VL-Bus slots (2 slave, 1 master/slave)
◆ ISA bus slots	6 x 16-bit ISA slots 2 x 8-bit ISA slots
◆ I/O bus speed	Up to 33MHz (VESA bus)

Power Management

◆ Green functions	Support Green Functions (Hardware controlled) Voltage regulation for DX4 CPUs

System Support Functions

◆ System functions	7 DMA channels, 16 level interrupts, Programmable timers
◆ Support functions	Fast A20 gate and Fast Reset
◆ Clock	Enhanced real time clock/calendar with battery back-up

Other Features

◆ Power good	On board power good signal generation
◆ Switches	Hardware Turbo, Reset, Keylock switches
◆ Size	8.5" (W) x 11" (L)

CHAPTER 2

GENERAL FEATURES

2.1 Layout of Hippo DCA2 Board

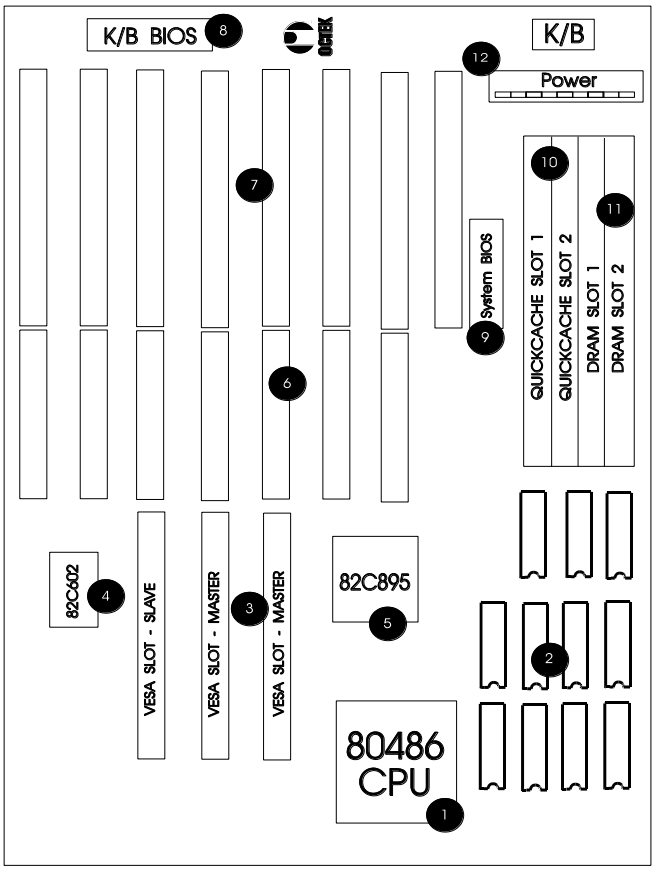


Figure 2

Inspect and clean your computer system regularly. Electronic components are sensitive to dust and dirt.

2.2 System Component Map

Memory / System Components	
1	Keyboard BIOS
2	Keyboard connector
3	Power connector
4	8-Bit ISA slots
5	16-Bit ISA Extension slots
6	32-Bit VESA Extension slots
7	DynamiCache slot-1 and slot-2
8	DRAM slot-1 and slot-2
9	System BIOS
10	Mach 210 programmable logic
11	Mach 110 programmable logic
12	82C802G chipset
13	Transistor Logics
14	CPU socket
15	NPD605A voltage regulator

Jumper Connectors	
P1	Reset
P2	Turbo SW
P3	Turbo Led
P4	Speaker
P5	Keylock
P6	Power Connector
P7	Power Connector
P8	External Battery Connector

2.3 Jumper Description Table

Jumper	Description	Setting Option		
JP1	Fan voltage select (+12/+5V)	1-2		+5V
		2-3	*	+12V
JP2	Fan connector	--		<RFU>
JP3	CPU clock speed select	1-2		25 Mhz
		2-3	*	33 MHz
JP4	CPU clock speed select	1-2		25 Mhz
		2-3	*	33 MHz
JP5	CPU reset signal source	1-2	*	<RFU>
JP6	CPU initialization signal source	open	*	Cyrix, SL
JP7	Cyrix CPU type select	1-2		2 x CLK
		2-3		1 x CLK
		open	*	
JP8	Floating point error pin select	1-2	*	486DX,DX2
		2-3		487
		open		486SX
JP9	VL-Bus operation	2-3		nonsynch.
		open	*	synch.
JP10	Non-maskable interrupt select	1-2, 3-4	*	486DX,DX2,487
		2-3		486SX
JP11	CPU bus speed type selection	1-2		CPU > 33Mz
		2-3	*	CPU <= 33Mz
JP12	VL-Bus wait state selection	1-2	*	1 wait state
		2-3		0 wait state
JP13	SL-CPU select	2-3	*	<RFU>
JP14	SL-CPU select	2-3	*	SL
JP15	Cyrix CPU support	2-3	*	<RFU>
JP16	CPU clock multiplier - 2.5x	open	*	<RFU>
JP17	Clock multiplier - 2x	open	*	<RFU>
JP18	EPMI	open	*	<RFU>
JP19	CMOS discharge	1-2		discharge
		2-3	*	preserve
JP20	Power Good Generation	1-2	*	off-board
		2-3		on-board
JP21	Color / Mono display select	1-2	*	color
		2-3		mono
JP22	Cyrix CPU Voltage Select (+3.3V)	open	*	<RFU> !
JP23	Cyrix CPU Voltage Select (+3.6V)	open	*	<RFU> !
JP24	Cyrix CPU Voltage Select (+3.8V)	open	*	<RFU> !
JP25	Cyrix CPU Voltage Select (+4.0V)	open	*	<RFU> !
JP26	Intel / AMD CLKMUL Select	1-2	*	<RFU>
		2-3		
JP27	CPU Voltage Auto-detect for Intel / AMD	1-2	*	<RFU> !
	CPU (+5.0V or +3.45V)	open		
JP28	Force CPU Voltage to +5.0V	open	*	<RFU> !
JW1	VL-Bus operation	1-2		nonsynch
		2-3	*	synch

* Factory Default Settings
<RFU> reserved for future use

Caution, consult your dealer before making changes to voltage select jumpers. Improper settings could cause permanent damages to the CPU.

2.4 DynamiCache

The DynamiCache memory subsystem consists of two 72-pin DynamiCache SIMM sockets. These sockets support up to 32MB of DynamiCache configured in 4MB, 8MB, and 16MB modules. (16MB to be released Q2 1995). The DynamiCache sockets are located on the top right corner of the motherboard.

The DynamiCache memory has already been preinstalled on the Hippo DCA2 motherboard. Additional DynamiCache can be ordered through Ocean Information Systems, Inc. or from one of over two hundred authorized distributors worldwide. DynamiCache is as easy to handle and install as standard 72-pin DRAM. It requires no special handling or skill other than taking normal anti-static precautions.

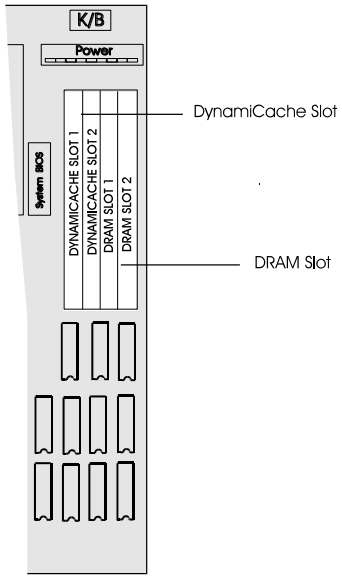


Figure 3

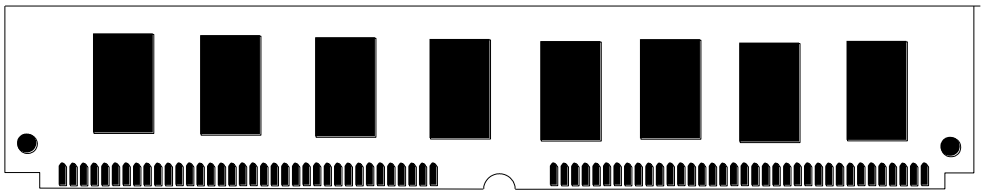


Figure 4 Side View of DynamiCache SIMM Module

2.5 DRAM Memory

For maximum versatility the Hippo DCA2 also has a traditional DRAM memory subsystem located next to the DynamiCache slots.

These two 72-pin DRAM SIMM sockets that support a maximum installation of 64MB DRAM. (It should be noted, however, that DRAM may drag down the overall system performance because of inherent design deficiencies in DRAM.) Each of the DRAM slots can be configured in 4MB, 8MB, 16MB, or 32MB up to a maximum of 64MB of DRAM.

2.6 Memory Configuration Table

Bank 0 DynamiCache Slot 1	Bank 1 DynamiCache Slot 2	Bank 2 DRAM Slot 1	Bank 3 DRAM Slot 2	Total Memory Size
4	X	X	X	4
4	X	2	X	6
4	X	2	2	8
4	X	8	X	12
4	X	8	8	20
4	4	X	X	8
4	4	4	X	12
4	4	4	4	16
4	4	8	X	16
4	4	8	8	24
4	4	16	X	24
4	4	16	4	28
4	4	16	16	40
4	4	32	X	40
4	4	32	32	72
4	8	X	X	12
4	8	8	X	20
8	X	X	X	8
8	X	4	X	12
8	X	4	4	16
8	X	8	X	16
8	X	8	8	24
8	X	16	X	24
8	X	16	4	28
8	X	16	16	40
8	X	32	X	40
8	X	32	32	72
8	8	X	X	16
8	8	8	X	24
8	8	8	8	32
8	8	16	X	32
8	8	16	16	48
8	8	32	X	48
8	8	32	32	80
16 *	X	X	X	16
16	X	8	X	24
16	X	8	8	32
16	X	16	X	32
16	X	16	16	48
16	X	32	X	48
16	X	32	32	80
16	16	X	X	32
16	16	16	X	48
16	16	16	16	64
16	16	32	X	64
16	16	32	32	96

* 16MB DynamiCache Module scheduled to be released Q2, 1995

2.7 Total System Memory

The entire main memory is composed of the total DynamiCache plus DRAM subsystem. Refer to the chart below for possible memory configurations, from 4MB to 32MB. The system auto detects the memory size.

For maximum efficiency in system performance, OISI strongly recommends a minimum of 8MB DynamiCache. Most of the advanced operating system application software (Chicago, Daytona, Windows NT, Windows for Workgroups, OS/2 2.11, et al) require a minimum of 8MB system memory to run efficiently. It would be to the user's benefit to install 8MB DynamiCache to allow the entire program set and data set to run within DCA2.

2.8 ISA Slots

ISA is the abbreviation for Industry Standard Architecture. It refers to the bus architecture originally created for the IBM XT and AT computers. The XT had an 8-bit data path and the AT a 16-bit data path. The AT has become the industry standard because of the large number of peripherals designed to connect to it. The Hippo DCA2 has six 16-bit ISA slots and two 8-bit ISA slot.

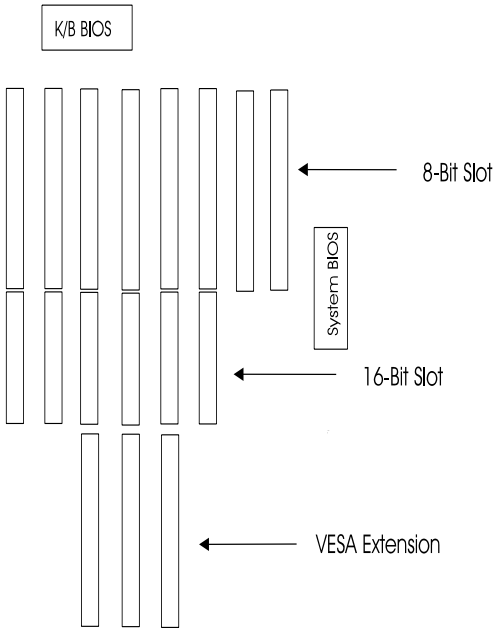


Figure 5

2.9 VESA Local Bus

VESA refers to the Video Electronics Standards Association, an organization of major PC graphics vendors devoted to improving graphics standards. The Hippo DCA2 has three 32-bit VESA Local Bus (VL) extensions and is one hundred percent compatible with the specification set forth by the Video Electronics Standards Association.

The 32-bit data path VESA Local Bus provide a direct link between the CPU and the system memory, allowing data to be processed at the speed of the CPU, up to 33MHz, rather than the slower running 16-bit at 8-12 Mhz data path ISA BUS rate.

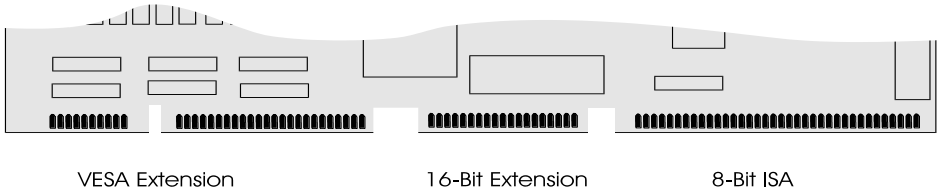


Figure 6

2.10 CPU

The Central Processing Unit (CPU) is the part of the computer that interprets and executes instructions. It is also referred to as the processor.

The Hippo DCA2 supports a wide range of processor types, including write back and low-powered CPUs as well as various processing speeds. With DynamiCache the onboard memory is brought up to the speed of the CPU, making it possible to run a fast processor without the problem of bottlenecks.

2.11 Processor Types Supported:

Intel 486SX-25	Intel 486SX-33	Intel 486DX-33	Intel 486DX2-50
Intel 486DX2-66	Intel 486DX4-100	Intel P24T	
AMD 486DX-33	AMD 486DX2-50	AMD 486DX2-66	
Cyrix 486DX-33	Cyrix 486DX2-50	Cyrix DX2-66	

2.12 BIOS

BIOS is an acronym for Basic Input/Output System. It is a setup program that stores system configurations used by the motherboard. This information is vital in order for the system to boot and work properly. There are various BIOS programs available. The Hippo DCA2 comes with the option of AMI BIOS or Microid Research BIOS.

2.13 Shadow RAM

Shadow RAM improves computer performance by taking data that is stored in ROM (read-only memory) and copying the information into the much faster RAM (random-access memory). The control setup for the Shadow RAM is located in the configuration registers.

2.14 Power Management

The Hippo DCA2 supports Green Functions, which make the system fully compliant with the Environmental Protection Agency's Energy Star program. In order to meet the EPA's Energy Star standards a system must consume fewer than 30 watts when in sleep mode. The Hippo DCA2 accomplishes this with two energy saving modes:

1) Spindown: Shuts down the hard drive when it isn't in use
2) Powerdown : Blanks the monitor and slows down the speed for Intel-compatible CPU.

2.15 Software Compatibility

◊ 100% IBM PC/AT compatible
◊ File servers, application servers, communication servers
◊ DOS, OS/2, UNIX, XENIX, Novell, Windows, and Windows NT.
◊ Computer-aided Design (CAD), Computer-aided Manufacturing (CAM)
◊ Graphic applications, Desktop Publishing

CHAPTER 3

SETUP AND INSTALLATION

3.1 Setup

Before installing the Hippo DCA2 motherboard in your system, you must attach the peripheral connectors. Follow the instructions outlined in this chapter for proper installation.

3.2 Installation Precautions

- Turn off the power whenever installing or removing any connectors, memory module or add-on cards.
- Before turning on the power, make sure that all the connectors, memory modules and add-on cards are secured.
- Eliminate any static electricity when handling the motherboard or any peripherals to prevent damage to electrical components. To eliminate electricity touch a grounded metal object before removing the board from the anti-static bag and wear a grounded wrist or ankle strap when handling the components.
- Put the board and perhipherals back into the anti-static bags when you are not using them.
- Always handle the board by its edges, taking care not to touch any of its components.

3.3 Operation and Maintenance

- Keep the system cool. The motherboard contains many high-speed components and they will generate heat during operation. Other add-on cards and the hard disk can also produce a lot of heat. The temperature inside the computer system may be very high. In order to keep the system running stable, the temperature must be kept at a low level. An easy way to do this is to keep the cool air circulating inside the case. If the temperature is still very high, install another fan inside the case. Using a larger case is recommended if there a number of add-on cards and disk drives in the system.
- Clean the "Gold Finger." Whenever inserting an add-on card to the motherboard make sure that there is no dirt on the "gold finger" of the add-on card. If dirt is present the contact between the "golden finger" and the slot may be poor, causing the add-on card to work improperly. Use a pencil eraser to clean the "gold finger" if dirt is found.
- Clean the motherboard. The computer system should be kept clean. Dust and dirt are harmful to electronic devices. To prevent dust from accumulating on the motherboard install all mounting plates on the rear of the case. Regularly examine your system and, if necessary, vacuum the interior of the system with a miniature vacuum.

3.4 CPU Jumper Settings

Brand	Type	JP3	JP4	JP5	JP6	JP7	JP8	JP10	JP11	JP13	JP14	JP15
Intel	SX-25	1-2	1-2	1-2	open	open	open	2-3	2-3	2-3	2-3	2-3
Intel	SX-33	2-3	2-3	1-2	open	open	open	2-3	2-3	2-3	2-3	2-3
Intel	DX-25	1-2	1-2	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	DX-33	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	DX2-50	1-2	1-2	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel *	DX2-66	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	DX4-75	1-2	1-2	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	DX4-100	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	P24T	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	487-25	1-2	1-2	1-2	open	open	2-3	1-2, 3-4	2-3	2-3	2-3	2-3
Intel	487-33	2-3	2-3	1-2	open	open	2-3	1-2, 3-4	2-3	2-3	2-3	2-3
Intel SL	SX-33	2-3	2-3	1-2	open	open	open	2-3	2-3	2-3	2-3	2-3
Intel SL	DX-33	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Intel SL	DX2-66	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
AMD	DX2-50	1-2	1-2	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
AMD	DX2-66	2-3	2-3	1-2	open	open	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Cyrix	DX-33	2-3	2-3	1-2	open	2-3	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Cyrix	DX2-50	1-2	1-2	1-2	open	1-2	1-2	1-2, 3-4	2-3	2-3	2-3	2-3
Cyrix	DX2-66	2-3	2-3	1-2	open	1-2	1-2	1-2, 3-4	2-3	2-3	2-3	2-3

* Manufacturer default jumper settings

3.5 CPU Installation

The CPU is composed of several pins that can easily be bent during installation, causing permanent damage to the processor. It is therefore very important that you make sure the pins are straight before installing the CPU onto the PGA socket located on your motherboard (refer to layout for exact location). To properly align the CPU with the socket align pin 1 of the CPU with pin 1 of the CPU PGA socket as demonstrated below.

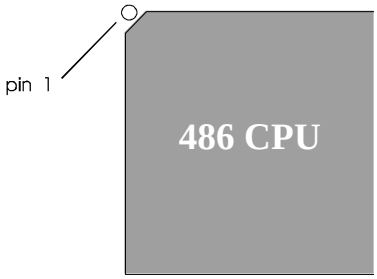


Figure 7 Top view of CPU

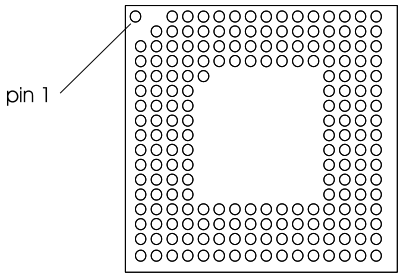


Figure 8 Top view of PGA Socket

Turn off the power whenever installing or removing any CPU, connector, memory module or add-on cards. Before turning on the power, make sure that all of these parts are secured.

3.6 DynamiCache/DRAM Installation

There are four memory banks located on the Hippo motherboard, marked DynamiCache Bank 1, DynamiCache Bank 2, DRAM Bank 1, DRAM Bank 2. The DynamiCache modules must be inserted into theDynamiCache banks and the DRAM modules into the DRAM banks.

Depending on how your memory is configured, you may not need to use all of the memory banks. It is important that you insert the modules in consecutive order, beginning with memory bank one. Before inserting the modules, position the motherboard so that the memory banks are facing the direction demonstrated.

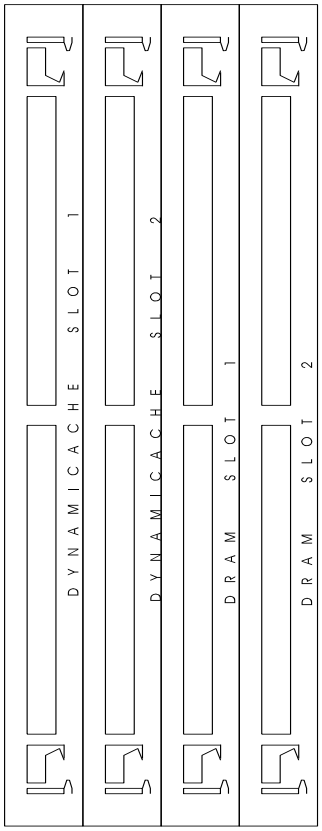


Figure 9 Memory Modules

Sockets

Never force the SIMM modules into the SIMM sockets. The sockets are fragile and the locking latches may break.

To insert the modules into the banks follow these steps:

1. Locate the notch on the corner of the module.
2. Hold the module so that the notch is at the bottom left corner.
3. Insert the bottom edge of the module into the bank at an angle, then push the module forward so that it is locked into place by the latches located on the sides of the bank. The latches should be locked tightly and the holes in the module should be aligned with the tabs on the bank.

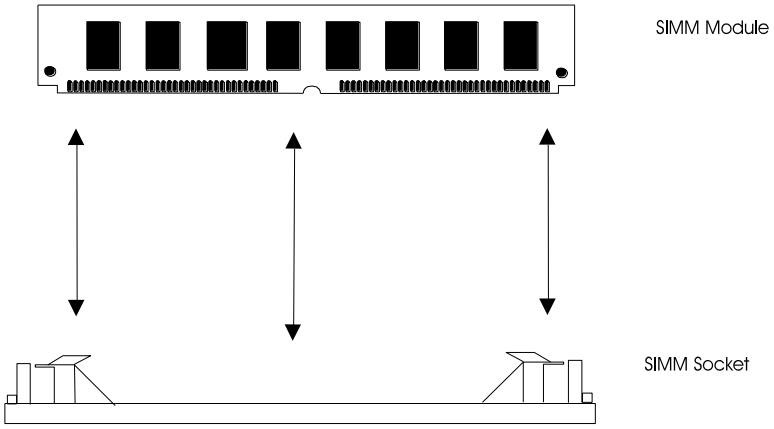


Figure 10 Proper Memory Module Installation

3.7 Compatible 72-pin SIMM TYPES

Slots	Memory Size	Speed
DynamiCache Slot 1	4M, 8M, 16M	15ns
DynamiCache Slot 2	4M, 8M, 16M	15ns
DRAM Slot 1	4M, 8M, 16M, 32M	60ns / 70ns
DRAM Slot 2	4M, 8M, 16M, 32M	60ns / 70ns

3.8 Control of System Speed

System speed can be controlled by keyboard and turbo switch. To change the speed by keyboard, use the minus sign (-) and the plus sign (+). Press <control> + <alt> + <"-"> for slow speed and <control> + <alt> + <"+"> for fast speed.

3.9 Fan voltage

There are two different voltages available for CPU fans; +5 volts and + 12 volts.Select a proper setting for jumper JP1 before you turn on the computer.

3.10 Fan Connector

This connector allows the CPU fan to draw current directly from the motherboard, without having to rely on a separate power connector.

A CPU fan is highly recommended for today's high speed CPUs. Extreme high CPU temperature are generated during system operations , and may cause abnormal hardware behaviour if system is not cool down.

3.11 Reset CMOS

If the setting of the system setup is done improperly it may make the system malfunction. If this happens, turn off the power and set jumper JP19 to 1-2 to reset the internal CMOS status register. Next, set the jumper JP19 back to 2-3 and turn on the power. The BIOS will find the CMOS status register is reset and will regard the setup information invalid, so it will prompt you to correct the information.

3.12 Color / Mono Display Select

Depending on the type of monitor you are using. Set jumper JP21 to 1-2 for a color display monitor (which includes all types of VGA monitors), and set jumper JP21 to 2-3 for a monochrome display monitor.

3.13 Connectors

The motherboard contains jumpers and dip switches that must be properly set before installing the board into the computer. These switches are necessary to configure various functions on the motherboard.

3.14 Reset Switch Connector

The reset switch connector is a two-pin single in-line berg that is attached to an externally mounted reset switch by cable. The reset button is used to warm reboot the system. his switch is open when it's ready for normal operation and is closed or shorted to reset the sytem.

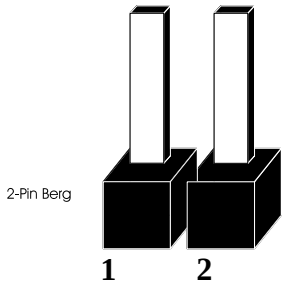


Figure 11

Pin	Assignment
1	Reset strobe
2	Ground

3.15 Turbo Switch Connector

The turbo switch connector is a two-pin single in-line berg that is attached by cable to an externally mounted turbo switch on the chasis. The turbo button is used to toggle between standard AT-Bus speed and maximum speed of the processor. This switch is open when it's ready for normal operation and is closed or shorted to obtain high speed of the sytem.

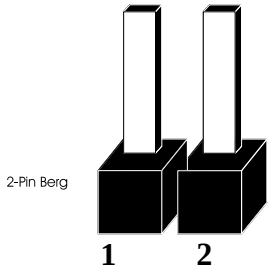


Figure 12

Pin	Assignment
1	Ground
2	Turbo strobe

3.16 Turbo Led Connector

The turbo Led is a two-pin single in-line berg that is connected to a LED display. The display lights up when the CPU is operating at full speed.

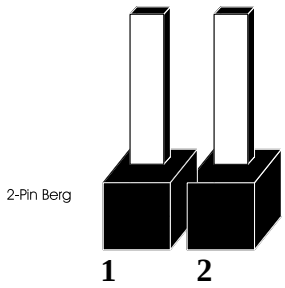


Figure 13

Pin	Description
1	Cathode
2	Anode

3.17 Speaker Connector

The speaker connector is a four-pin berg that is attached via a cable to the system speaker.
This is a nonpolarized connector and can be installed in keyed position.

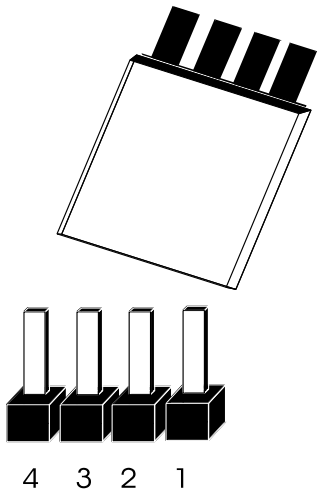


Figure 14

Pin	Description
1	Data Out
2	Key
3	Ground
4	VCC

3.18 Keyboard Lock Connector

The keyboard lock enables the user to lock the keyboard, preventing unauthorized use of the system. J??? is a five-pin single in-line berg that is attached to the keyboard lock connector by a cable.

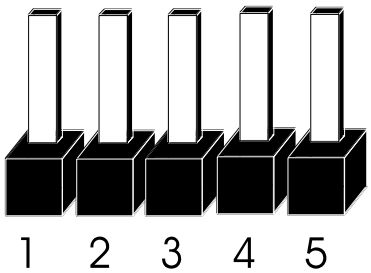


Figure 15

Pin	Assignment
1	LED power
2	Key
3	Ground
4	Keyboard lock
5	Ground

3.19 Keyboard Connector

The keyboard connector is a five-pin DIN socket. Attach a standard AT-compatible keyboard cable. The pin assignments are listed below.

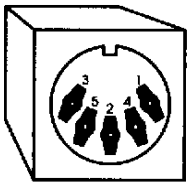


Figure 16

Pin	Assignment
1	Keyboard clock
2	Keyboard data
3	Not used
4	Ground
5	VCC

Turn off the power whenever installing or removing any connector, memory module or add-on cards. Before turning on the power, make sure that all of these parts are secured.

3.20 External Battery Connector

The Hippo DCA2 comes with an onboard rechargeable battery so an external battery is not necessary. As an added feature, however, the board does support an external battery of 3.6 volts. Install the battery according to the pin assignments listed in diagram below.

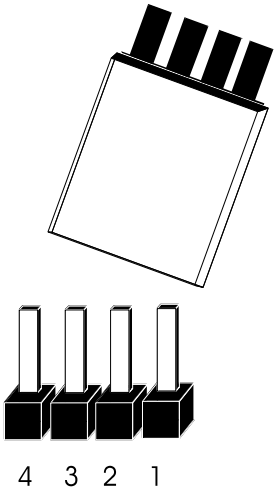


Figure 17

Pin	Assignment
1	3.6 Volt DC
2	Not used
3	Not used
4	Ground

3.21 Power Supply Connector

The power supply is the electrical device that converts the alternating current used by standard A C outlets to the lower-voltage direct current required by computers. A stable power source is essential for proper and reliable operation. It is therefore a good idea to use a high quality power supply. It is essential that the power supply provide +5 VDC with a voltage range between +4.95 VDC and +5.25 VDC.

There are two power supplies connectors on the motherboard. Power supplies can run on a wide range of voltages and must be set to the proper range. Each connector has six wires, all of which must be aligned with the proper pin number.

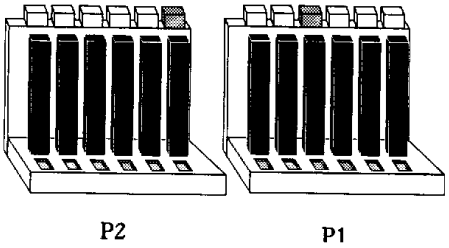
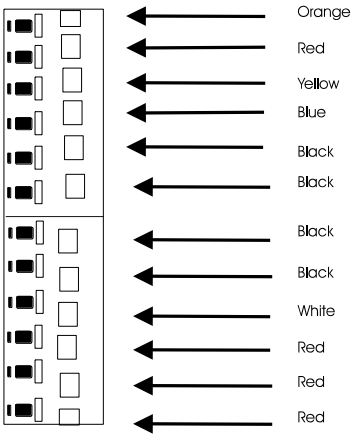


Figure 18 Front View of Power Connectors



Pin	Assignment
1	Power Good (orange wire)
2	VCC (red wire)
3	+12 Volts (yellow wire)
4	-12 Volts (blue wire)
5	Ground (black wire)
6	Ground (black wire)
7	Ground (black wire)
8	Ground (black wire)
9	-5 Volts (white wire)
10	VCC (red wire)
11	VCC (red wire)
12	VCC (red wire)

Figure 19 Top View of Power Connectors

CHAPTER 4

BIOS SET UP

4.1 BIOS Power-On Self-Test (POST)

During the self-test, errors may occur. These errors are communicated through a series of beeps. The method of beeps used depends on the BIOS program. For example, Microid Research BIOS uses a combination of low and high tones. AMI BIOS uses a series of beeps with different error messages that correspond to the number of beeps heard.

4.2 AMI BIOS Error Beep Codes

# of Beeps	Error Message	Explanation
1	DRAM Refresh Failure	The memory refresh circuitry is faulty
2	Parity Error	A parity error occured in the first 64KB block of memory
3	Base 64K RAM Failure	A memory failure occurred in the first 64KB of memory
4	System Timer Failure	Timer 1 is not functioning
5	Processor Failure	An error occurred in the CPU
6	Gate A20 Failure	The BIOS is unable to switch the CPU into protected mode
7	Processor Exception Error	An exception interrupt occured in the CPU
8	Display Memory Read/Write Error	The system video adapter is missing or its memory is faulty
9	ROM Checksum Error	The ROM checksum value does not match the BIOS code
10	Read/Write Error	The CMOS shutdown register memory has failed

4.3 Microid Research BIOS Error Beep Codes

Beep Tones	Error Message
L H L H H	Real time clock is not updating
L H-L L L	ROM BIOS checksum test
L H-H L L	Page register test
L H-L H L	Keyboard controller self-test
L H-H H L	Memory refresh circuit test
L H-L L H	Master DMA controller failure
L H-H L H	Slave DMA controller failure
L H-L L L L	Memory bank 0 pattern test failure
L H-H L L L	Memory bank 0 parity circuitry failure
L H-L H L L	Memory bank 0 parity error
L H-H H L L	Memory bank 0 data bus failure
L H-L L H L	Memory bank 0 address failure
L H-H L H L	Memory bank 0 block access read failure
L H-L H H L	Memory bank 0 block access read/wrfitge failure
L H-H H H L	Master 8259 failure
L H-L L L H	Slave 8259 failure
L H-H L L H	Master 8259 interrupt address error
L H-L H L H	Slave 8259 interrupt address error
L H-H H L L	8259 interrupt address error
L H-L L H H	Master 8259 stock interrupt error
L H-H L H	Slave 8259 stock interrupt error
L H-L H H H	System timer 8254 interrupt failure
L H-H H H H	8254 channel 0 test and initialization
L H-L L L L H	8254 channel 2 speaker failure

After the power is on, wait for a minute before proceeding. The system BIOS are going through a self-test and nothing is displayed on screen. After the self-test, the system BIOS initialize the display adaptor and show messages.

APPENDIX

ADVANCED TECHNICAL INFORMATION

A.1 Memory Address Map

Address	Size	Function
0000000-009FFFF	640 KB	System board memory
00A0000-00BFFFF	128 KB	Video RAM display buffer
00C0000-00DFFFF	128 KB	Reserved for add-on cards ROM BIOS
00E0000-00EFFFF	64 KB	System ROM BIOS expansion
00F0000-00FFFFF	64 KB	System ROM BIOS
0100000-0FDFFFF	15232 KB	Extended memory
0FE0000-0FEFFFF	64 KB	Duplicates of system ROM BIOS at 0F0000-0FFFFFF
1000000-5FFFFFF	80 MB	Extended memory
0000000-5FFFFFF	96 MB	Total memory space addressable by Hippo DCA2 VESA System Board

A.2 I/O Address Map

I/O Address Hex 000 to 0FF are reserved for the system board and Hex 100 to 3FF are for I/O channels.

Address (Hex)	Device
000-01F	DMA Controller 1, 8237A-5
020-021	Interrupt Controller 1, 8237A-5
022-023	Chip set Address
040-04F	Timer 1, 8254
050-05F	Timer 2, 8254
060-06F	8042 Keyboard/Controller
070-07F	Real Time Clock, Non-Maskable Interrupt Mask
080-09F	DMA Page Registers
0A0-0BF	Interrupt Controller 2,8259A
0C0-0DF	DMA Controller 2, 8237A-5
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game Ports
278-27F	Parallel Printer Port 2 (PIO-2)
2F8-2FF	Serial Port 2 (SIO-2)
300-31F	Prototype Card/Streaming Tape Adapter
360-363	PC Network, Low Address
368-36B	PC Network, High Address
378-37F	Parallel Printer Port 1 (PIO-1)
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Primer Adapter
3C0-3CF	EGA Adapter
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1 (SIO-1)

A.3 I/O Extension Pinout

A.3i 8-Bit ISA Pinout

Ground	GND	B1	A1	-I/O CHCK	I
O	RSTDRV	B2	A2	SD7	I/O
Power	+5 VDC	B3	A3	SD6	I/O
I	IRQ9	B4	A4	SD5	I/O
Power	-5 VDC	B5	A5	SD4	I/O
I	DRQ2	B6	A6	SD3	I/O
Power	-12 VDC	B7	A7	SD2	I/O
I	OWS	B8	A8	SD1	I/O
Power	+12 VDC	B9	A9	SD0	I/O
Ground	GND	B10	A10	-I/O CHRDY	I
O	-SMEMW	B11	A11	AEN	O
O	-SMEMR	B12	A12	SA19	I/O
I/O	-IOW	B13	A13	SA18	I/O
I/O	-IOR	B14	A14	SA17	I/O
O	-DACK3	B15	A15	SA16	I/O
I	DRQ3	B16	A16	SA15	I/O
O	-DACK1	B17	A17	SA14	I/O
I	DRQ1	B18	A18	SA13	I/O
I/O	-Ref	B19	A19	SA12	I/O
O	CLK	B20	A20	SA11	I/O
I	IRQ7	B21	A21	SA10	I/O
I	IRQ6	B22	A22	SA9	I/O
I	IRQ5	B23	A23	SA8	I/O
I	IRQ4	B24	A24	SA7	I/O
I	IRQ3	B25	A25	SA6	I/O
O	-DACK2	B26	A26	SA5	I/O
O	T/C	B27	A27	SA4	I/O
O	BALE	B28	A28	SA3	I/O
Power	+5 VDC	B29	A29	SA2	I/O
O	OSC	B30	A30	SA1	I/O
Ground	GND	B31	A31	SA0	I/O

A.3ii 16-Bit ISA Extension Pinout

I	-MEMCS16	D1	C1	-BHE	I/O
I	-I/OCS16	D2	C2	LA23	I/O
I	IRQ10	D3	C3	LA22	I/O
I	IRQ11	D4	C4	LA21	I/O
I	IRQ12	D5	C5	LA20	I/O
I	IRQ15	D6	C6	LA19	I/O
I	IRQ14	D7	C7	LA18	I/O
0	-DACK0	D8	C8	LA17	I/O
I	DRQ0	D9	C9	-MEMR	I/O
0	-DACK5	D10	C10	-MEMW	I/O
I	DRQ5	D11	C11	SD08	I/O
0	-DACK6	D12	C12	SD09	I/O
I	DRQ6	D13	C13	SD10	I/O
0	-DACK7	D14	C14	SD11	I/O
I	DRQ7	D15	C15	SD12	I/O
Power	+5 VDC	D16	C16	SD13	I/O
I	-MASTER	D17	C17	SD14	I/O
Ground	GND	D18	C18	SD15	I/O

A.4 VL-BUS Extension Pinout

CD1	B1	A1	CD0
CD3	B2	A2	CD2
Ground	B3	A3	CD4
CD5	B4	A4	CD6
CD7	B5	A5	CD8
CD9	B6	A6	Ground
CD11	B7	A7	CD10
CD13	B8	A8	CD12
CD15	B9	A9	Power
Ground	B10	A10	CD14
CD17	B11	A11	CD16
Power	B12	A12	CD18
CD19	B13	A13	CD20
CD21	B14	A14	Ground
CD23	B15	A15	CD22
CD25	B16	A16	CD24
Ground	B17	A17	CD26
CD27	B18	A18	CD28
CD29	B19	A19	CD30
CD31	B20	A20	Power
CA30	B21	A21	CA31
CA28	B22	A22	Ground
CD26	B23	A23	CA29
Ground	B24	A24	CA27
CA24	B25	A25	CA25
CA22	B26	A26	CA23
Power	B27	A27	CA21
CA20	B28	A28	CA19
CA18	B29	A29	Ground
CA16	B30	A30	CA17
CA14	B31	A31	CA15
CA12	B32	A32	Power
CA10	B33	A33	CA13
CA8	B34	A34	CA11
Ground	B35	A35	CA9
CA6	B36	A36	CA7
CA4	B37	A37	CA5
WBack	B38	A38	Ground
BEO	B39	A39	CA3
Power	B40	A40	CA2
BE1	B41	A41	n/c
BE2	B42	A42	Reset
Ground	B43	A43	D/C
BE3	B44	A44	M/IO
ADS	B45	A45	W/R
LRDY	B46	A46	RDY
LDEV	B47	A47	Ground
LREQ	B48	A48	IRQ9
Ground	B49	A49	BRDY
LGNT	B50	A50	Blast
Power	B51	A51	ID0
ID2	B52	A52	ID1
ID3	B53	A53	Ground
ID4	B54	A54	VLCLK
LKEN	B55	A55	Power
Leads	B56	A56	LBS16

A.5 Direct Memory Access Channels

Channel	Function	8-Bit	16-Bit	Transfer

				Block Size
0	Spare	8-bit		64
1	SDLC	8-bit		64
2	Floppy Disk	8-bit		64
3	Spare	8-bit		64
4	Cascade for DMA controller 1			
5	Spare		16-bit	128
6	Spare		16-bit	128
7	Spare		16-bit	128

A.6 DMA Controller Registers

Address (Hex)	Command Code
C0	CH-0 base and current address
C2	CH-0 base and current word count
C4	CH-1 base and current address
C6	CH-1 base and current word count
C8	CH-2 base and current address
CA	CH-2 base and current word count
CC	CH-3 base and current address
CE	CH-3 base and current word count
D0	Read Status Register/Write Command Register
D2	Write Request Register
D4	Write Single Mask Register Bit
D6	Write Mode Register
D8	Clear Byte Pointer Flip-Flop
DA	Read Temporary Register/Write Master Clear
DC	Clear Master Register
DE	Write All Mask Register Bits

A.7 Page Register Address

Page Register	I/O Address (Hex)
DMA Channel 0	0087
DMA Channel 1	0083
DMA Channel 2	0081
DMA Channel 3	0082
DMA Channel 5	008B
DMA Channel 6	0089
DMA Channel 7	008A
Refresh	008F

A.8 System Interrupts

Interrupt Controllers (NMI level)		Parity or I/O Channel Check
CTLR 1	CTLR 2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from CTLR 2
	IRQ8	Real-time Clock Interrupt
	IRQ9	Software Redirected to INT 0AH (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Diskette Controller
IRQ7		Parallel Port 1