Developer Note

Macintosh LC III

Developer Note

Developer Technical Publications

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About This Developer Note

This developer note describes the hardware and software features of the Macintosh LC III computer, emphasizing those features that are new or different from other Macintosh computers.

This document is written primarily for experienced Macintosh hardware and software developers who want to create products that are compatible with the Macintosh LC III. If you are unfamiliar with Macintosh computers, or would simply like more technical information, you may want to read the related technical manuals listed in the following section.

Supplementary Documents

For more information about Macintosh computers, developers should read *Guide to the Macintosh Family Hardware*, second edition, *Designing Cards and Drivers for the Macintosh Family*, third edition, and *Inside Macintosh*. The Macintosh LC and LC II developer notes provide information about these similar models that may also be of interest to you. For detailed information about the Motorola 68030 microprocessor used in the Macintosh LC III, refer to the *MC68030 Enhanced 32-Bit Microprocessor User's Manual*. All of these books are available through APDA.

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Conventions and Abbreviations

This developer note uses abbreviations and typographical conventions that are standard in Apple publications.

Typographical Conventions

This note uses the following typographical conventions.

New terms appear in **boldface** where they are first defined.

Computer-language text—any text that is literally the same as it appears in computer input or output—appears in `Courier` font.

Standard Abbreviations

When unusual abbreviations appear in this book, the corresponding terms are also spelled out. Standard units of measure and other widely-used abbreviations are not spelled out.

Standard units of measure used in Apple reference books include:

A	amperes	MB	megabytes
GB	gigabytes	MHz	megahertz
Hz	hertz	ms	milliseconds
K	1024	ns	nanoseconds
KB	kilobytes	V	volts
mA	milliamperes	W	watts

Standard abbreviations used in Apple reference books include:

$*n*	hexadecimal value *n*
AC	alternating current
ADB	Apple Desktop Bus
CD-ROM	compact disc read-only memory
CLUT	color look-up table
DAC	digital-to-analog converter
IC	integrated circuit
ASIC	application-specific integrated circuit
MMU	memory-management unit
RAM	random-access memory
ROM	read-only memory
RGB	red-green-blue (a video display system used by Apple computers)

SCSI	Small Computer System Interface
SVGA	super VGA (a video display system used with PC-type computers)
VGA	video graphics adapter (a video display system used with PC-type computers)
VRAM	video RAM

CHAPTER 1

Hardware

This chapter describes the major features of the Macintosh LC III computer and emphasizes the similarities and differences between it and the Macintosh LC II computer.

Introduction

The Macintosh LC III computer is an enhanced version of the Macintosh LC II computer featuring a faster CPU, increased video display options, and a 32-bit processor-direct slot interface that is compatible with cards designed for the Macintosh LC and LC II. The Macintosh LC III comes equipped with 4 MB of RAM and supports up to 32 MB of additional RAM (36 MB total). Overall performance is similar to that of the Macintosh IIci.

Like the Macintosh LC and LC II, the Macintosh LC III contains internal video circuits to drive an external color or monochrome monitor. The Macintosh LC III supports all Apple monitors 16-inches or smaller. The Macintosh LC III also adds 16-bit color mode for photographic quality display and improved QuickTime performance on 14-inch or smaller monitors.

The Macintosh LC III introduces a new 114-pin processor-direct slot (PDS) for expansion cards. The PDS connector is notched to allow installation of 96-pin cards designed for the Macintosh LC and LC II. For compatibility with older cards, the Macintosh LC III computer's processor-direct slot offers both 16-bit and 32-bit bus master capability.

The Macintosh LC III is Apple's most powerful slim-line Macintosh and provides solid performance for business, home, and educational users at a cost comparable to the Macintosh LC II.

Features

The Macintosh LC III includes the following features:

- Microprocessor: 68030 running at 25 MHz.
- Coprocessor: PLCC (plastic leaded chip carrier) socket on the main logic board for installing an optional 68882 floating point unit (FPU).
- Read-only memory (ROM): 1 MB on the main logic board.
- Random-access memory (RAM): 4 MB soldered to the main logic board; 1 SIMM socket that accepts a 1 MB, 2 MB, 4 MB, 8 MB, 16 MB, or 32 MB SIMM for expansion up to 36 MB. Developers should note that the Macintosh LC III uses a 72-pin SIMM package that is different from the SIMM package used on other Macintosh models. The specifications and pinout are described later in this chapter.
- Expansion: a 114-pin processor-direct slot (PDS) on the main logic board provides direct access to the 68030 processor by an optional expansion card. The PDS connector is notched to allow installation of 96-pin cards designed for the Macintosh LC and LC II. Maximum power budget is 4 watts.

- Floppy disk: one internal 20-pin floppy disk connector. One internal 1.4 MB Apple SuperDrive is standard. The Macintosh LC III does not support additional internal or external floppy disk drives.
- Hard disk: one internal SCSI hard disk is standard. Additional SCSI hard disks can be attached to the external SCSI port.
- I/O: one Apple Desktop Bus (ADB) port, two mini-DIN 8 serial ports, one DB-25 SCSI port, one audio output jack for headphones or external speakers, one microphone jack for sound input, and one DB-15 video connector.
- Video: on-board video support for Apple 12-, 13-, and 16-inch RGB monitors, the Apple Portrait monitor, and VGA monitors. The interface is RS-343.

  Video data is stored in 512 KB of video RAM (VRAM) soldered to the main logic board. One SIMM socket is included for optional expansion to 768 KB of VRAM.
- Sound: monaural sound input and output functionally identical to that of the Macintosh LC and LC II. Sound from a microphone or line input is sampled at a 22 kHz or 11 kHz rate, digitized, and stored along with other data to be used for a variety of purposes such as presentations or voice annotation.
- Keyboard: an ADB mouse is standard; a detached ADB keyboard is included with some configurations.

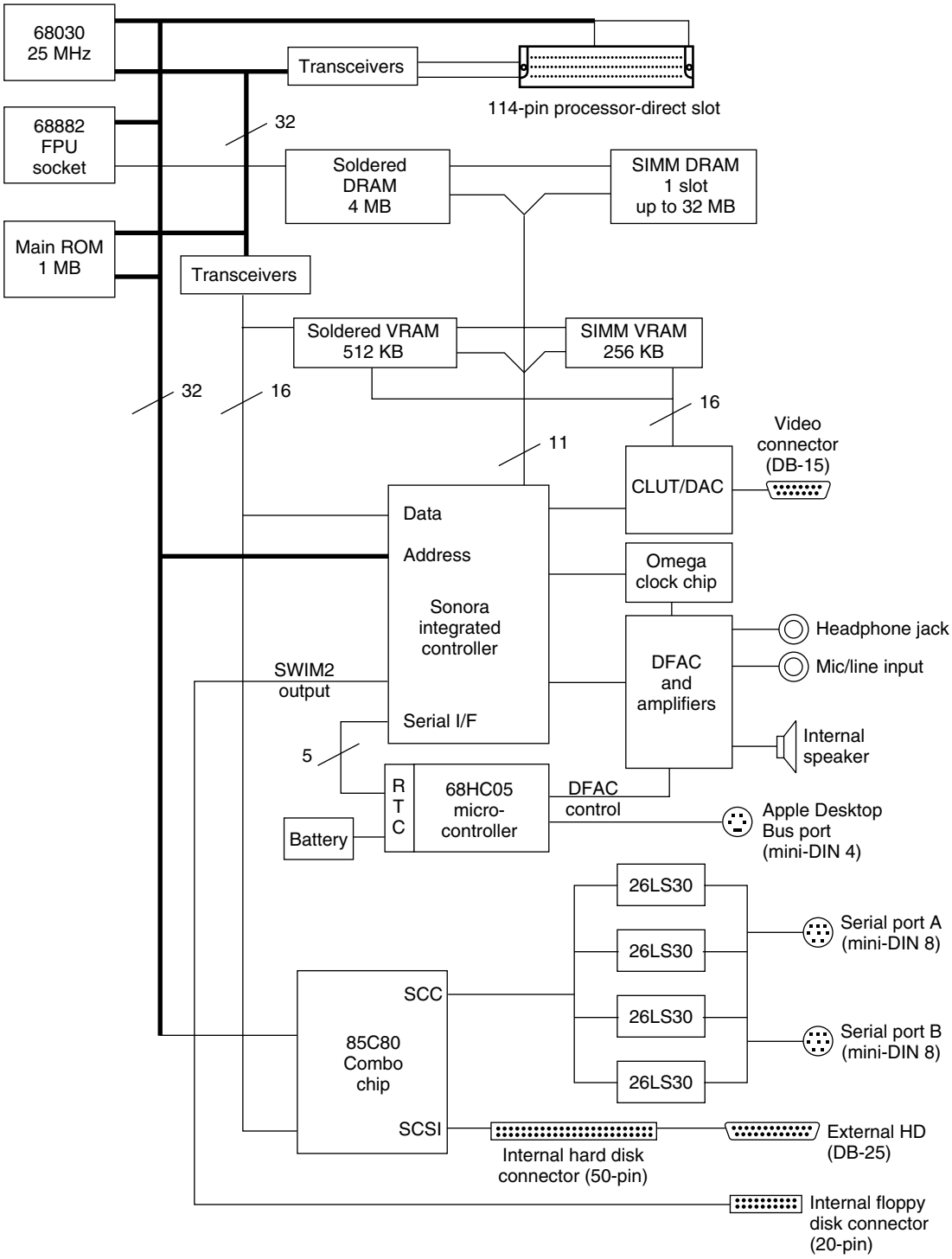
Design Differences

The design of the Macintosh LC III computer is based on a new custom integrated controller chip named Sonora. The Sonora chip provides all the functionality of the V8 gate array used in the Macintosh LC and LC II, while adding new capabilities and features. The major differences between the Macintosh LC III and the Macintosh LC II are listed below.

- The system clock in the Macintosh LC III operates at 25 MHz.
- The Macintosh LC III uses a 32-bit DRAM data path to further improve performance.
- The high-density 72-pin SIMM socket on the Macintosh LC III allows up to 32 MB of memory to be installed in a single socket.
- The new Sonora integrated controller combines the features of the V8 chip (timing, address decoding, video generation, sound control, and general logic circuits) and the SWIM2 chip (floppy disk control) while providing support for more video display modes and higher processor speeds.
- The Macintosh LC III computer includes a 114-pin processor-direct slot with a complete set of data and address lines, and 32-bit bus master capability.
- A socket for an optional FPU is provided on the main logic board. Some configurations of the Macintosh LC III may be shipped with an FPU installed.

The block diagram in Figure 1-1 illustrates how the major components of the Macintosh LC III are interconnected.

Figure 1-1 Block diagram of the Macintosh LC III computer



Compatibility Issues

This section highlights key areas you should investigate to ensure that your hardware and software products are compatible with the Macintosh LC III. These topics are covered in more detail in subsequent sections.

RAM SIMM Socket

The Macintosh LC III uses a 72-pin RAM SIMM package that is very different from the 30-pin packages used on other Macintosh models. Although the connector looks similar to parts used by other computer manufacturers, it is designed to Apple specifications. Likewise, SIMM packages intended for use in the Macintosh LC III must meet Apple design guidelines.

In addition to voiding Apple's warranty, installing a SIMM that does not meet Apple specifications can cause system errors and increase electromagnetic interference (EMI) beyond government-regulated limits.

Processor-Direct Slot

The 114-pin processor-direct slot (PDS) expansion connector introduced in the Macintosh LC III is compatible with cards designed for the 96-pin connector used on the Macintosh LC II. Cards designed for the Macintosh LC will also work, if they are compatible with the 68030 microprocessor.

Video Modes

The video circuitry in the Macintosh LC III is based on the Macintosh LC and LC II, but supports more monitors and 16-bit color. These changes should be transparent to applications that adhere to the compatibility guidelines published in *Inside Macintosh*.

Because the VRAM data path is 16-bits wide, PDS bus master cards that access the frame buffer directly must use 8- or 16-bit transfers.

To ensure that your applications work well with all types of monitors, use the appropriate QuickDraw routines to determine the size and resolution of the monitor attached to a Macintosh LC III computer.

Floppy Disk Controller

The Macintosh LC III uses a new floppy disk controller circuit, SWIM2, that is part of the Sonora chip. Because the SWIM2 controller is different from the original SWIM, software that accesses the controller directly will not work with the Macintosh LC III. The only way for software to access the floppy disk is through driver calls documented in *Inside Macintosh*.

For situations where direct access to the raw track data is required, use the Diagnostic Raw Track Dump call described in the Macintosh Technical Note *M.DV.SonyDriver*.

Floating Point Unit

Application software that takes advantage of an FPU must use the Gestalt Manager to determine if an FPU is installed in a Macintosh LC III. The Gestalt Manager is described in *Inside Macintosh*.

Because an FPU is not standard in all Macintosh models, application software should not expect or require an FPU. The Standard Apple Numerics Environment (SANE) package in the Macintosh Operating System automatically takes advantage of an FPU when available and provides optimized mathematics routines for use when an FPU is not present. SANE is described in the *Apple Numerics Manual, Second Edition*, available from APDA.

Hardware Overview

This section provides a functional description of the Macintosh LC III computer's hardware systems.

IMPORTANT
The memory sizes, addresses, and other information provided in this chapter are specific to the Macintosh LC III computer and are provided for informational purposes only. To ensure that your application software is compatible with both current and future Macintosh systems you must use the Macintosh Toolbox and Operating System routines wherever provided. In particular, never use absolute addresses to access hardware, because these addresses are specific to a particular Macintosh model and are subject to change. ▲

Microprocessor

The Macintosh LC III uses a Motorola 68030 microprocessor running at a clock rate of 25 MHz. The microprocessor accesses RAM and ROM using 32-bit data transfers. VRAM accesses use 16-bit transfers.

Omega Clock Chip

Omega is a custom programmable phase locked loop clock generator that provides the primary clocks required by the Macintosh LC III. Omega produces a hardware-selectable system clock for the microprocessor bus, a programmable dot clock for the video circuits, and a fixed 31.3344 MHz clock used for the serial ports, sound circuits, floppy disk, and various timers.

Sonora Integrated Controller

Sonora is a new custom chip that integrates the functions of the V8 and SWIM chips used in the Macintosh LC II. These functions include timing, memory mapping, video and sound control, miscellaneous GLU (General Logic Unit) functions, and floppy disk control. Sonora's primary functions are described in the following sections.

Timing

Sonora converts the 50 MHz system clock generated by Omega into a 25 MHz CPU clock for the 68030 microprocessor. Sonora also produces a 16 MHz clock for its internal VIAs and the PDS, and sends the necessary commands to Omega to control the dot clock rate.

Address Decode and Memory Mapping

Like other Macintosh computers that use the 68030 processor, the Macintosh LC III supports both 24-bit and 32-bit memory addressing modes. The Macintosh LC III hardware, however, always operates in 32-bit mode. The memory management unit (MMU) inside the 68030 works with Sonora's memory controller to map 24-bit addresses to their 32-bit equivalent. System or application software can select 24-bit addressing mode using the `SwapMMUMode` operating system routine described in *Inside Macintosh*.

In 32-bit mode the 68030 processor supports a 4 GB address space. In 24-bit mode the upper 8 address bits are ignored and address space is limited to 16 MB. Sonora remaps the address space so that RAM, ROM, VRAM, I/O, and expansion all appear in this 16 MB range. Although the address translation is transparent to software, it has the effect of limiting the amount of addressable RAM to 8 MB. Table 1-1 summarizes the 24- and 32-bit memory maps for the Macintosh LC III.

Table 1-1 Memory map summary

Function	24-bit mode	32-bit mode
RAM	$00 0000–$7F FFFF	$0000 0000–$023F FFFF
ROM	$80 0000–$8F FFFF	$4080 0000–$408F FFFF
I/O space	$F0 0000–$FF FFFF	$50F0 0000–$50FF FFFF
VRAM	$B0 0000–$BB FFFF	$60B0 0000–$60BB FFFF
RAM disk	not addressable	$7000 0000–$723F FFFF
PDS	$E0 0000–$EF FFFF	$FE00 0000–$FEFF FFFF

To maintain compatibility with current addressing conventions, software should address the expansion slot as if it were NuBus™ physical slot 6 (logical slot $E) by using either the 16 MB standard slot space from $FE00 0000 through $FEFF FFFF or the 256 MB super slot space from $E000 0000 through $EFFF FFFF.

Note
Sonora issues a bus error if you try to access address $FF FFFF in the 24-bit mode or address $FFFF FFFF in the 32-bit mode. ◆

Video Generation

With the exception of the color look-up table (CLUT) and final output stage, Sonora provides all the video control circuitry for the Macintosh LC III. Sonora determines the amount of VRAM installed in the system at power-up, senses the type of monitor attached to the external video port, refreshes VRAM, controls access to the frame buffer, and controls all video timing signals.

Sound Control

Sonora's sound control circuitry is functionally identical to that provided by the V8 gate array in the Macintosh LC and LC II, except that memory for the sound input and output buffers is located in VRAM rather than in DRAM. This change is transparent to software that uses the Sound Manager.

GLU and VIA Functions

Sonora includes a full-function VIA1, a pseudo-VIA2 similar to that of the V8 gate array, and several registers similar to those of the Apple Sound Chip.

Floppy Disk Control

Sonora contains a new floppy disk controller circuit named SWIM2. This circuit duplicates the functions of the SWIM chip used in previous Macintosh models. Software that uses documented Macintosh routines for floppy disk I/O will work properly with the Macintosh LC III.

ROM

The Macintosh LC III computer's main ROM is contained in two 40-pin, 256K x 16-bit ICs providing 1 MB of read-only memory. A total of 4 MB of address space is reserved for future ROM expansion. ROM accesses by the main processor typically require 5 clock cycles, which is equivalent to 2 wait states.

Like all Macintosh computers, the Macintosh LC III implements an overlay function at power-up or reset that maps ROM address space (in this case, $4080 0000–$408F FFFF) to RAM space starting at location $0000 0000. Following the first access to the normal ROM address range, the ROM image at $0000 0000 is cleared and replaced by RAM. This process is transparent to software developers.

RAM

The Macintosh LC III computer comes standard with 4 MB of RAM soldered to the main logic board. This memory consists of eight 1 M x 4-bit dynamic RAM ICs, and occupies the address space from $0000 0000 through $003F FFFF.

RAM read accesses typically require 5 clock cycles (2 wait states), while write operations are typically accomplished in 4 cycles (1 wait state). Burst reads are supported.

RAM Expansion Interface

A single SIMM socket on the Macintosh LC III main logic board allows users to add up to 32 MB of additional RAM. The Macintosh LC III uses a 72-pin SIMM connector instead of the 30-pin type used in most other Macintosh models. Because all 32 data signals are provided on the connector, one SIMM socket can replace four of the earlier 30-pin SIMM sockets.

The SIMM can contain one or two banks of RAM, using one or both sides of the board. At system startup, the boot code determines the amount of RAM installed in all banks and then sets a RAM configuration register in Sonora. The Macintosh LC III requires 80 ns fast page mode dynamic RAM.

Table 1-2 shows the possible RAM SIMM configurations. Note that expansion RAM begins at address $0040 0000, immediately after the 4 MB of standard RAM.

Table 1-2 RAM SIMM configurations

Expansion RAM	Banks	Address range (24-bit)	Address range (32-bit)
1 MB	1	$40 0000–$4F FFFF	$0040 0000–$004F FFFF
2 MB	2	$40 0000–$5F FFFF	$0040 0000–$005F FFFF
4 MB	1	$40 0000–$7F FFFF	$0040 0000–$007F FFFF
8 MB	2	$40 0000–$7F FFFF*	$0040 0000–$00BF FFFF
16 MB	1	$40 0000–$7F FFFF*	$0040 0000–$013F FFFF
32 MB	2	$40 0000–$7F FFFF*	$0040 0000–$023F FFFF

* A maximum of 8 MB can be addressed in 24-bit mode.

Table 1-3 shows the signal assignments for the SIMM socket. Figure 1-2 shows the physical design guidelines for the SIMM printed circuit board assembly.

To ensure reliable operation, and comply with U.S. and foreign regulations, Apple has developed specific requirements for the Macintosh LC III SIMM. For example, pin contacts must be tin, not gold or copper, and the PCB must dedicate one layer to power and one to ground. Capacitive loading must also be kept within specific limits.

IMPORTANT

The 72-pin SIMM used in the Macintosh LC III is not interchangeable with SIMMs used by other computer manufacturers. ▲

Table 1-3 RAM SIMM connector pinout

Pin	Signal name	Description
1	GND	Ground
2	DQ0	Data input/output bus, bit 0
3	DQ16	Data input/output bus, bit 16
4	DQ1	Data input/output bus, bit 1
5	DQ17	Data input/output bus, bit 17
6	DQ2	Data input/output bus, bit 2
7	DQ18	Data input/output bus, bit 18
8	DQ3	Data input/output bus, bit 3
9	DQ19	Data input/output bus, bit 19
10	+5V	+5 volts
11	n.c.	Not connected
12	A0	Address bus, bit 0
13	A1	Address bus, bit 1
14	A2	Address bus, bit 2
15	A3	Address bus, bit 3
16	A4	Address bus, bit 4
17	A5	Address bus, bit 5
18	A6	Address bus, bit 6
19	n.c.	Not connected
20	DQ4	Data input/output bus, bit 4
21	DQ20	Data input/output bus, bit 20
22	DQ5	Data input/output bus, bit 5
23	DQ21	Data input/output bus, bit 21
24	DQ6	Data input/output bus, bit 6
25	DQ22	Data input/output bus, bit 22
26	DQ7	Data input/output bus, bit 7
27	DQ23	Data input/output bus, bit 23

continued

Table 1-3 RAM SIMM connector pinout (continued)

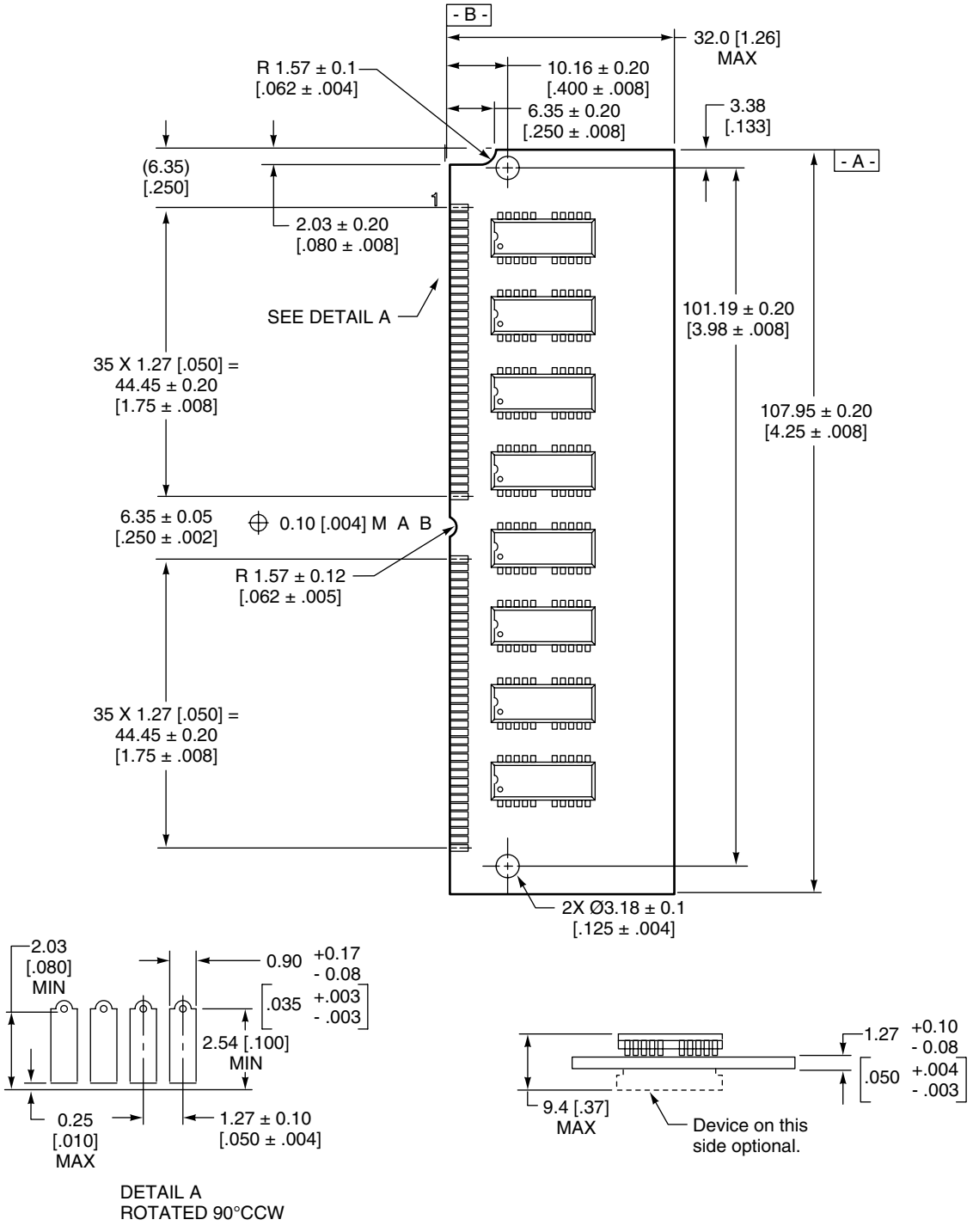
Pin	Signal name	Description
28	A7	Address bus, bit 7
29	n.c.	Not connected
30	+5V	+5 volts
31	A8	Address bus, bit 8
32	A9	Address bus, bit 9
33	/RAS3	Row Address Strobe 3
34	/RAS2	Row Address Strobe 2
35	—	Reserved
36	—	Reserved
37	—	Reserved
38	—	Reserved
39	GND	Ground
40	/CAS0	Column Address Strobe 0
41	/CAS2	Column Address Strobe 2
42	/CAS3	Column Address Strobe 3
43	/CAS1	Column Address Strobe 1
44	/RAS0	Row Address Strobe 0
45	/RAS1	Row Address Strobe 1
46	n.c.	Not connected
47	/W	Write enable
48	n.c.	Not connected
49	DQ8	Data input/output bus, bit 8
50	DQ24	Data input/output bus, bit 24
51	DQ9	Data input/output bus, bit 9
52	DQ25	Data input/output bus, bit 25
53	DQ10	Data input/output bus, bit 10
54	DQ26	Data input/output bus, bit 26
55	DQ11	Data input/output bus, bit 11
56	DQ27	Data input/output bus, bit 27
57	DQ12	Data input/output bus, bit 12
58	DQ28	Data input/output bus, bit 28

continued

Table 1-3 RAM SIMM connector pinout (continued)

Pin	Signal name	Description
59	+5V	+5 volts
60	DQ29	Data input/output bus, bit 29
61	DQ13	Data input/output bus, bit 13
62	DQ30	Data input/output bus, bit 30
63	DQ14	Data input/output bus, bit 14
64	DQ31	Data input/output bus, bit 31
65	DQ15	Data input/output bus, bit 15
66	n.c.	Not connected
67	—	Reserved
68	—	Reserved
69	—	Reserved
70	—	Reserved
71	n.c.	Not connected
72	GND	Ground

Figure 1-2 RAM SIMM design guide



Note: Dimensions are in millimeters with inches in brackets.

Video Interface

The video circuits in the Macintosh LC III computer are similar to those of the Macintosh LC and LC II, but provide support for additional monitors and 16-bit color. All video timing is controlled by Sonora. Video data is stored in a dedicated 512 KB VRAM frame buffer on the main logic board, and a SIMM socket allows VRAM expansion to 768 KB. The Macintosh LC III requires 80 ns VRAM.

Color modes up to 8 bits per pixel use a 256 x 24-bit CLUT which is provided by an enhanced version of the custom chip used in the LC and LC II. Monochrome modes also use the CLUT but drive the red, green, and blue inputs with the same signal.

The Macintosh LC III supports a 640 x 400 video mode that allows users to display 16-bit color on 13-inch RGB and VGA monitors without having to purchase additional VRAM. Users can select this mode from the Options menu in the Monitors control panel.

VRAM

The Macintosh LC III computer comes with 512 KB of VRAM provided by four 256K x 4-bit ICs soldered to the main logic board. A 68-pin SIMM socket allows users to increase their video display options by installing additional VRAM. The Macintosh LC III uses the same type of VRAM SIMM as the Macintosh LC and LC II, except that the Macintosh LC III requires 80 ns components.

The 256 KB VRAM expansion SIMM for the Macintosh LC III contains two 128K x 8-bit parts. Together with the built-in VRAM, this configuration provides a total of 768 KB VRAM. If a SIMM larger than 256 KB is installed, the additional memory is unused.

Monitors Supported

The Macintosh LC III supports the monitors and video modes listed in Table 1-4. The monitor connects to the computer’s DB-15 external video connector and identifies itself by a 3-bit code. Table 1-5 shows the pinout for the external video connector. If no monitor is connected, the synchronization signals are not generated. Monitor sensing is discussed in the following section.

Table 1-4 Video modes

Monitor	Resolution			Dot clock (MHz)	VRAM required
	Width (pixels)	Height (pixels)	Depth (bits)		
12-inch RGB	512	384	1	15.6672	Standard(512 KB)
	512	384	2	15.6672	Standard
	512	384	4	15.6672	Standard
	512	384	8	15.6672	Standard
	512	384	16	15.6672	Standard
	560	384	16	17.2340	Standard
13-inch RGB*	640	400	1	30.2400	Standard
	640	400	2	30.2400	Standard
	640	400	4	30.2400	Standard
	640	400	8	30.2400	Standard
	640	400	16	30.2400	Standard
	640	480	1	30.2400	Standard
	640	480	2	30.2400	Standard
	640	480	4	30.2400	Standard
	640	480	8	30.2400	Standard
	640	480	16	30.2400	768 KB
VGA	640	480	1	25.1750	Standard
	640	480	2	25.1750	Standard
	640	480	4	25.1750	Standard
	640	480	8	25.1750	Standard
	640	480	16	25.1750	768 KB
Portrait	640	870	1	57.2832	Standard
	640	870	2	57.2832	Standard
	640	870	4	57.2832	Standard
	640	870	8	57.2832	768 KB
16-inch RGB	832	624	1	57.2832	Standard
	832	624	2	57.2832	Standard
	832	624	4	57.2832	Standard
	832	624	8	57.2832	Standard

* Includes Macintosh Color Display, AppleColor High Resolution RGB Monitor, and Apple High Resolution Monochrome Monitor.

Table 1-5 External video connector pinout

Pin	Signal name	Description
1	RED.GND	Red video ground
2	RED.VID	Red video signal
3	/CSYNC	Composite synchronization signal
4	SENSE0	Monitor sense signal 0
5	GRN.VID	Green video signal
6	GRN.GND	Green video ground
7	SENSE1	Monitor sense signal 1
8	n.c.	Not connected
9	BLU.VID	Blue video signal
10	SENSE2	Monitor sense signal 2
11	GND	CSYNC and VSYNC ground
12	/VSYNC	Vertical synchronization signal
13	BLU.GND	Blue video ground
14	HSYNC.GND	HSYNC ground
15	/HSYNC	Horizontal synchronization signal
Shell	SGND	Shield ground

Monitor Sense Codes

To identify the type of monitor connected, the Macintosh LC III uses the standard Apple monitor sense codes as well as the newer extended sense codes. Table 1-6 shows the sense codes for each of the monitors that the Macintosh LC III supports. Refer to the Macintosh Technical Note *M.HW.SenseLines* for a description of the sense code system.

Table 1-6 Recognized monitor sense codes

Monitor	Standard sense code	Extended sense code		
	(2 : 0)	(1,2)	(0,2)	(0,1)
12-inch RGB	0 1 0	—	—	—
13-inch RGB	1 1 0	—	—	—
Portrait	0 0 1	—	—	—

Table 1-6 Recognized monitor sense codes

Monitor	Standard sense code	Extended sense code		
	(2 : 0)	(1,2)	(0,2)	(0,1)
VGA	1 1 1	0 1	0 1	1 1
16-inch RGB	1 1 1	1 0	1 1	0 1
No monitor	1 1 1	1 1	1 1	1 1

Internal Video Connection

Like the Macintosh LC and LC II, the Macintosh LC III includes a 12-pin surface-mount video connector on the main logic board. This feature allows you to design a video overlay card for the 512 x 384 monitor. The card plugs into the PDS expansion connector and uses the internal video connector to drive the monitor without requiring an external loopback cable. The video overlay card attaches to the internal video connector using a flexible cable, which the card manufacturer must provide. Table 1-7 shows the pinout for the internal video connector.

Table 1-7 Internal video connector pinout

Pin	Signal name	Description
1	GND	Ground
2	GRN.VID	Green video signal
3	GND	Ground
4	RED.VID	Red video signal
5	GND	Ground
6	BLU.VID	Blue video signal
7	GND	Ground
8	/CBLANK	Composite blanking signal
9	GND	Ground
10	OVERLAY	Overlay signal
11	GND	Ground
12	/CSYNC	Composite synchronization signal

The three color video signals shown in Table 1-7 are the same as the RS-343 signals that appear on the external DB-15 video connector. /CBLANK and /CSYNC are TTL signals that drive the CLUT (color look-up table).

The internal video connector does not provide a pixel clock signal for a video overlay card. Your card must generate the pixel clock and synchronize itself with the internal video controller using the /CSYNC and /CBLANK signals.

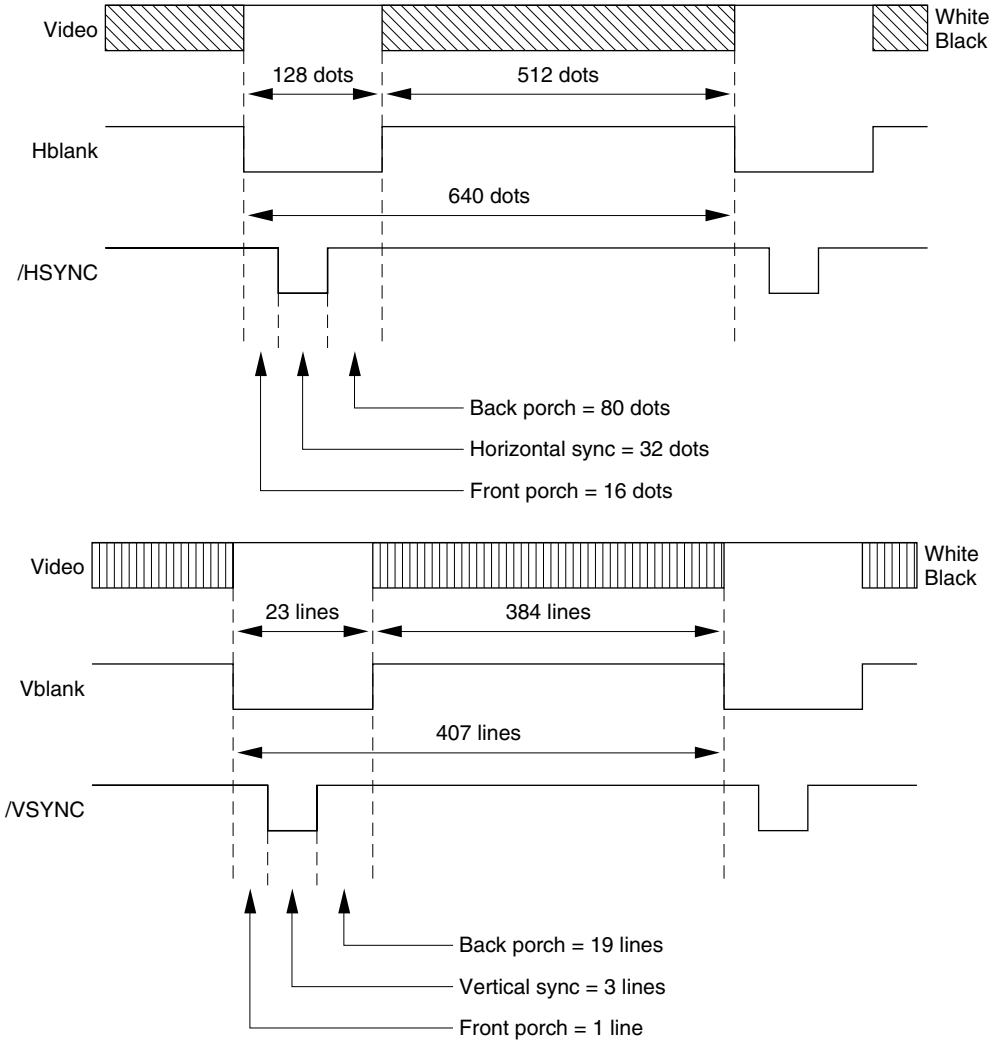
The OVERLAY signal selects which video controller drives the monitor. Normally this is the digital-to-analog converter (DAC) on the Macintosh LC III computer's main logic board. Asserting the OVERLAY signal turns off the internal DAC and allows a video overlay card to drive the monitor.

Transmission line effects are minimized by the fact that the video DAC outputs are current outputs and are terminated with 75-ohm resistors on the main logic board. There is a 2-pixel clock delay period between the time when the OVERLAY signal is asserted and the time when the master DAC outputs go off. Even when the internal DAC is off it outputs blanking and setup current, so if the video card fails to provide a signal the video outputs are driven to the completely dark level.

Video Timing

Figures 1-3 through 1-9 show timing information for the supported video modes. These figures define the blanking, synchronizing, and active video regions of the video scan waveforms in terms of dot or pixel times. A dot is the time required to draw a single pixel.

Figure 1-3 512 x 384 video timing

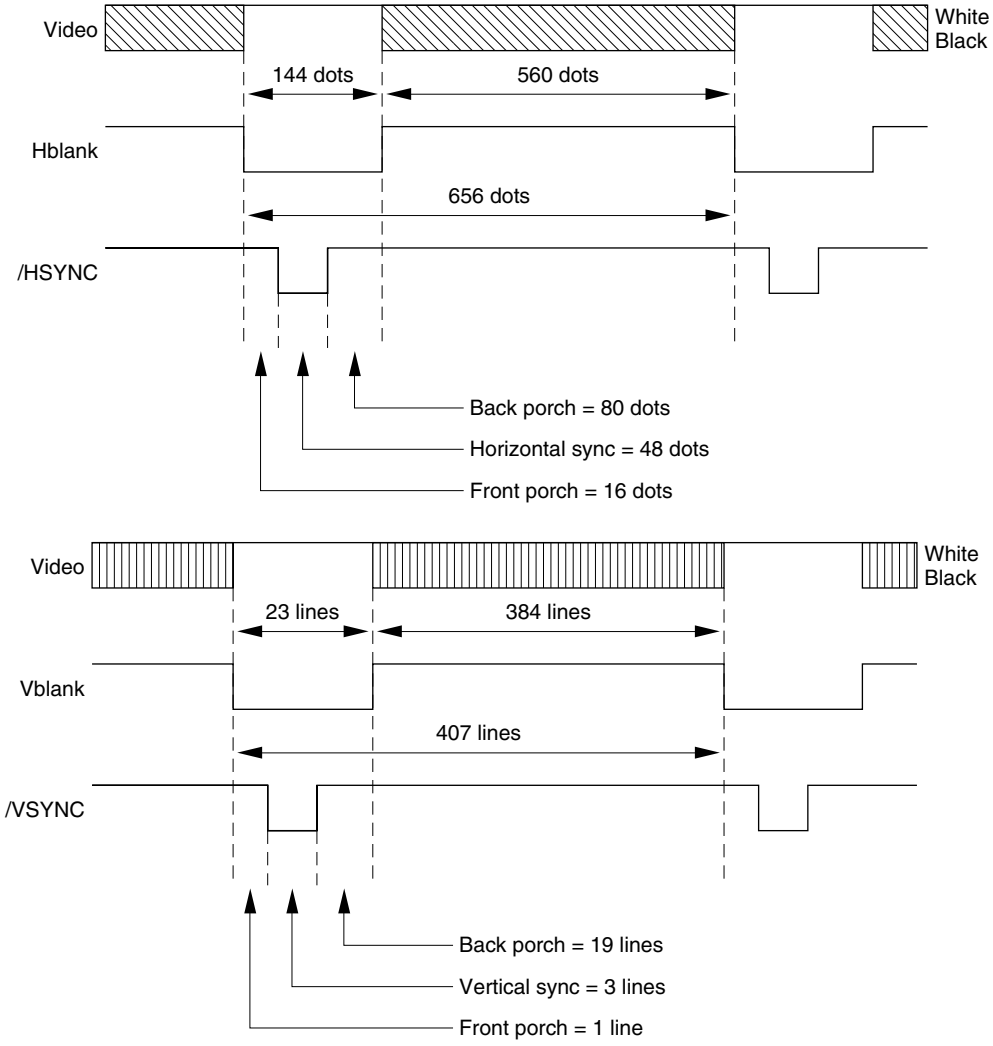


Dot clock = 15.6672 MHz
Dot = 63.83 nS

Full line = 40.85 µs
Line rate = 24.48 kHz

Full frame = 16.626 mS
Frame rate = 60.15 Hz

Figure 1-4 560 x 384 video timing

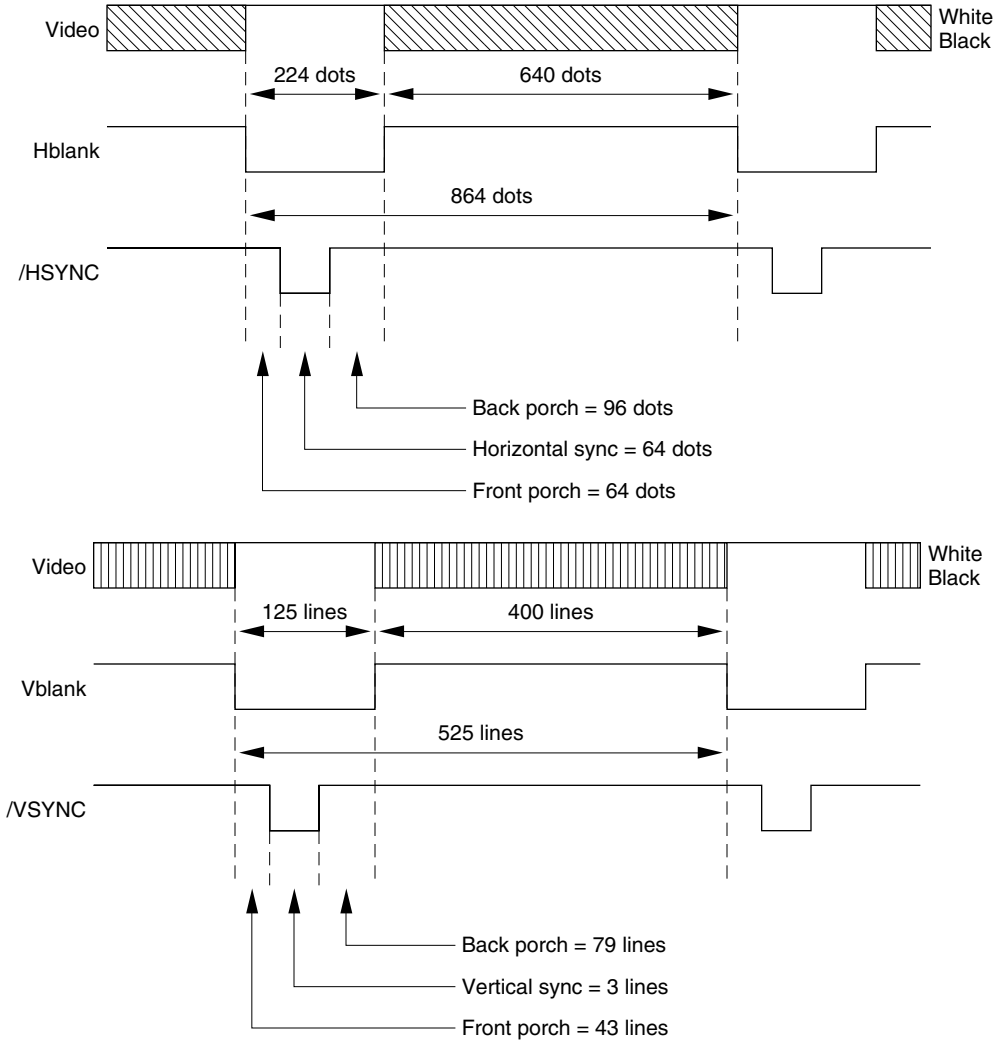


Dot clock = 17.2340 MHz
Dot = 58.02 nS

Full line = 40.85 µs
Line rate = 24.48 kHz

Full frame = 16.63 mS
Frame rate = 60.15 Hz

Figure 1-5 640 x 400 video timing

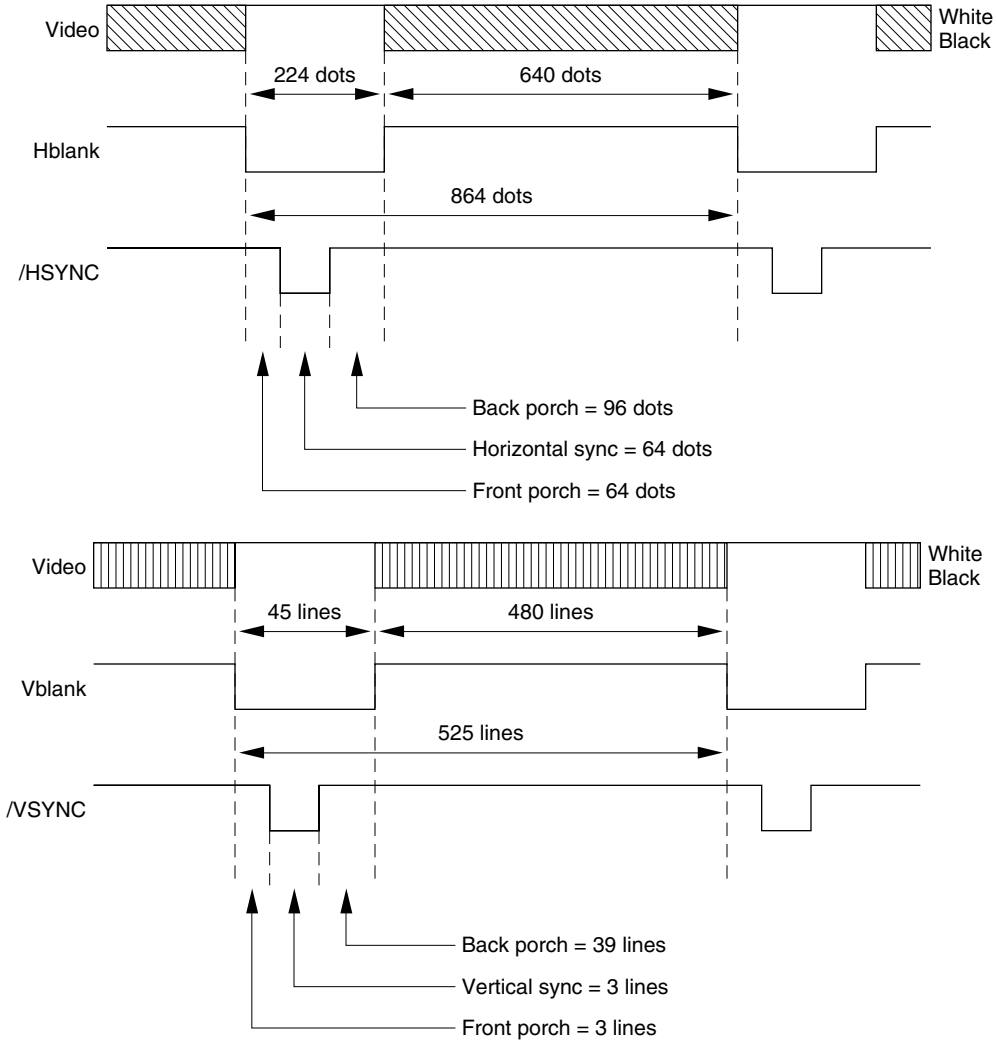


Dot clock = 30.2400 MHz
Dot = 33.07 nS

Full line = 28.57 µs
Line rate = 35.0 kHz

Full frame = 15.0 mS
Frame rate = 66.67 Hz

Figure 1-6 640 x 480 video timing

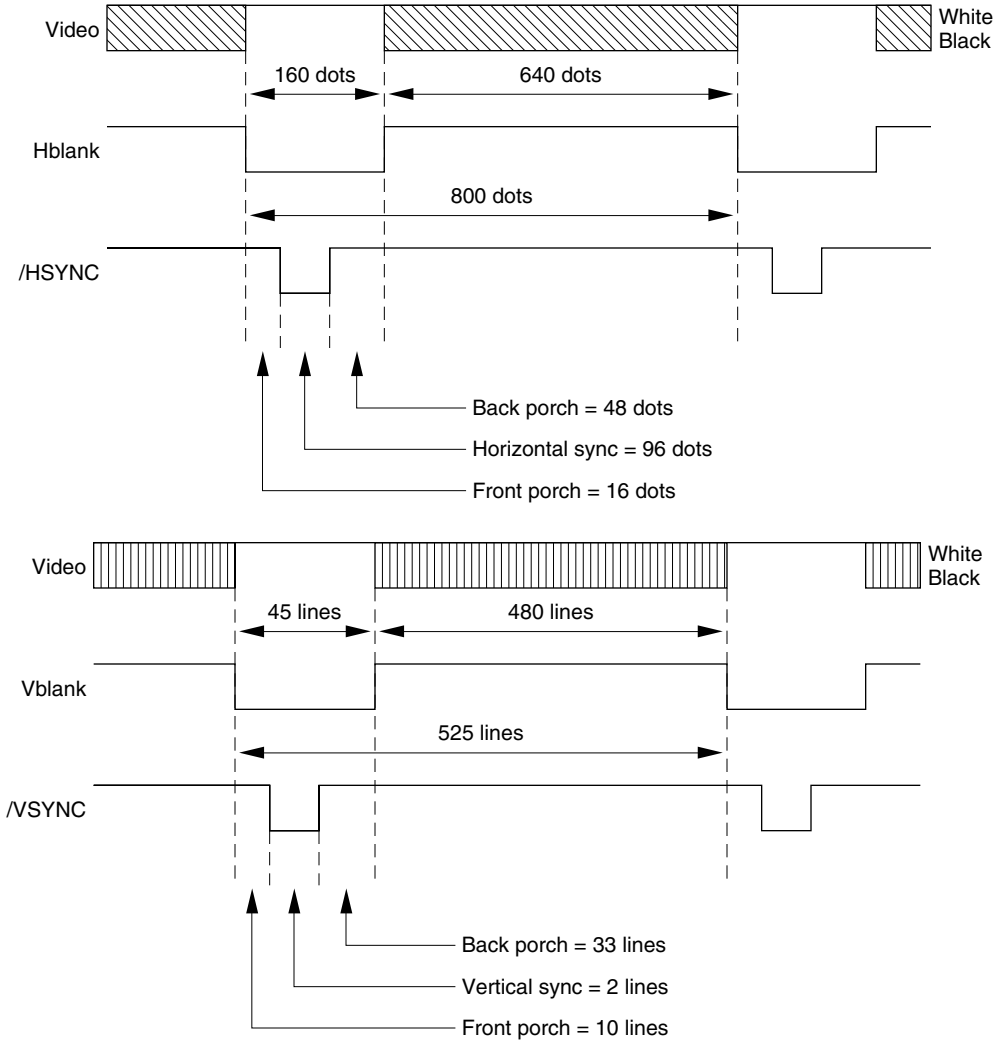


Dot clock = 30.2400 MHz
Dot = 33.07 nS

Full line = 28.57 µs
Line rate = 35.0 kHz

Full frame = 15.0 mS
Frame rate = 66.67 Hz

Figure 1-7 640 x 480 VGA timing

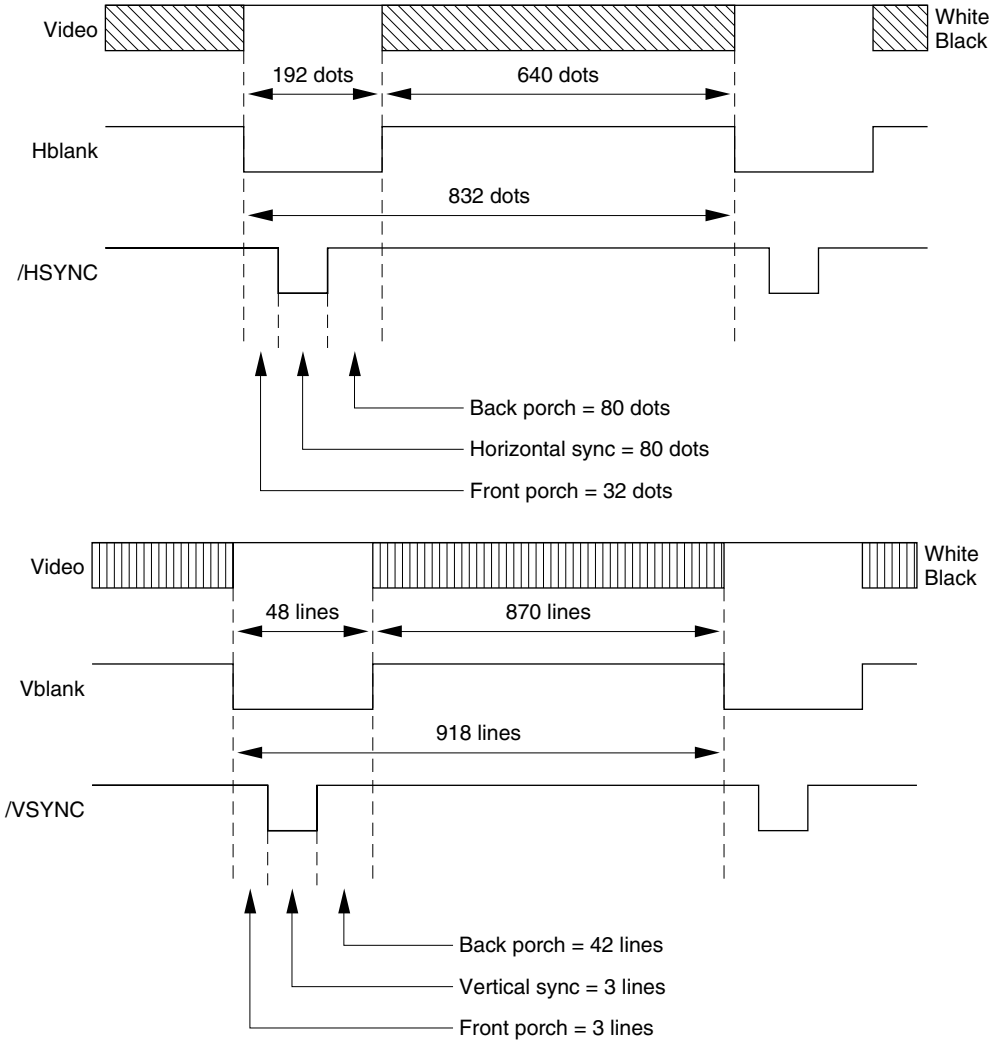


Dot clock = 25.175 MHz
Dot = 39.722 nS

Full line = 31.778 µs
Line rate = 31.469 kHz

Full frame = 16.68 mS
Frame rate = 59.94 Hz

Figure 1-8 640 x 870 video timing

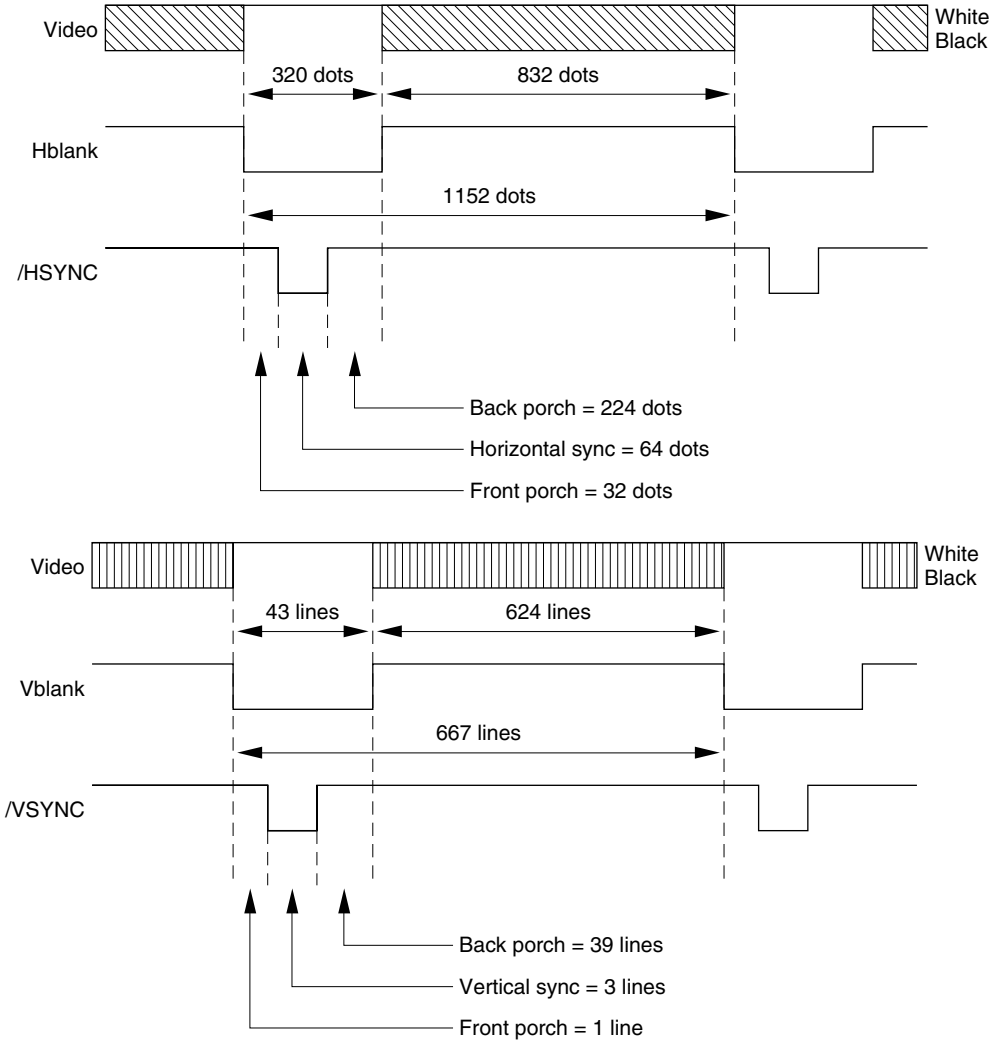


Dot clock = 57.2832 MHz
Dot = 17.457 nS

Full line = 14.52 µs
Line rate = 68.850 kHz

Full frame = 13.33 mS
Frame rate = 75 Hz

Figure 1-9 832 x 624 video timing



Dot clock = 57.2832 MHz
Dot = 17.46 nS

Full line = 20.11 µs
Line rate = 49.725 kHz

Full frame = 13.41 mS
Frame rate = 74.55 Hz

Sound System

The Macintosh LC III sound system includes a built-in speaker, an external stereo headphone jack that plays in monaural but to both ears, and a microphone input jack for the sound input feature.

The Macintosh LC III sound hardware is essentially the same as that of the Macintosh LC and LC II, except that memory for the sound input and output buffers is located in VRAM rather than in DRAM. This change is transparent to application software that uses the Sound Manager.

Serial and SCSI Interfaces

The Combo serial communication and SCSI controller in the Macintosh LC III is the same custom chip used in the Macintosh LC and LC II. The Combo chip combines the functions of the 85C30 serial communication controller (SCC) and 53C80 SCSI controller chips in a single device.

Serial Communication Controller

The SCC portion of the Combo chip provides two independent ports for serial communication. These ports are identical except that the modem port supports synchronous transmission while the printer port does not. The 8-pin miniature DIN connectors are the same as those currently used on other Macintosh computers. Table 1-8 shows the pinout for the serial ports.

Table 1-8 Serial port signals

Pin number	Signal name	Signal description
1	HSKo	Handshake output
2	HSKi	Handshake input
3	TxD–	Transmit data –
4	SG	Signal ground
5	RxD–	Receive data –
6	TxD+	Transmit data +
7	GPi	General-purpose input
8	RxD+	Receive data +

SCSI Controller

The SCSI controller in the Combo chip is completely compatible with the SCSI controller chip used on current members of the Macintosh family. It is designed to support the SCSI interface as defined by the American National Standards Institute (ANSI) X3T9.2 committee. The Macintosh LC III includes the same 50-pin internal and 25-pin external SCSI connectors used on other members of the Macintosh family. Table 1-9 shows the pinouts for these connectors.

Table 1-9 Internal and external SCSI connector pinouts

Internal (50-pin)	External (25-pin)	Signal name	Signal description
2	8	/DB0	Bit 0 of SCSI data bus
4	21	/DB1	Bit 1 of SCSI data bus
6	22	/DB2	Bit 2 of SCSI data bus
8	10	/DB3	Bit 3 of SCSI data bus
10	23	/DB4	Bit 4 of SCSI data bus
12	11	/DB5	Bit 5 of SCSI data bus
14	12	/DB6	Bit 6 of SCSI data bus
16	13	/DB7	Bit 7 of SCSI data bus
18	20	/DBP	Parity bit for SCSI data bus
26	25	TPWR	+5 volts termination power
32	17	/ATN	Attention
36	6	/BSY	Busy
38	5	/ACK	Acknowledge
40	4	/RST	SCSI data bus reset
42	2	/MSG	Message
44	19	/SEL	Select
46	15	/C/D	Control/data
48	1	/REQ	Request
50	3	/I/O	Direction (input/output)
All odd pins (25 total)	7, 9, 14, 16, 18, and 24	GND	Ground

NOTE Pins not listed above are not connected.

Floppy Disk Interface

The Sonora chip contains a new floppy disk control circuit named SWIM2. This circuit is functionally identical to the SWIM chip used in other Macintosh models, and is fully compatible with applications that use the File Manager or Disk Driver routines for floppy disk access.

The Macintosh LC III includes an internal 3.5-inch 1.4 MB Apple SuperDrive. A 20-pin connector carries the signal interface between the main logic board and the drive. Table 1-10 shows the pinout for the floppy disk connector.

Table 1-10 Floppy disk connector pinout

Pin number	Signal name	Signal description
1	GND	Ground
2	PH0	Phase 0: state-control line
3	GND	Ground
4	PH1	Phase 1: state-control line
5	GND	Ground
6	PH2	Phase 2: state-control line
7	GND	Ground
8	PH3	Phase 3: register write strobe
9	n.c.	Not connected
10	/WRREQ	Write data request
11	+5V	+5 volts
12	SEL	Head select
13	+12V	+12 volts
14	/ENBL	Drive enable
15	+12V	+12 volts
16	RD	Read data
17	+12V	+12 volts
18	WR	Write data
19	+12V	+12 volts
20	+5V	+5 volts

ADB Microcontroller

The Macintosh LC III computer uses the same 68HC05 microcontroller as the Macintosh LC and LC II. This chip integrates the functions of the Apple Desktop Bus (ADB) controller, real-time clock (RTC), parameter RAM (PRAM), power-on reset, keyboard reset, and nonmaskable interrupt (NMI).

ADB Interface

The ADB is a single-master, multiple-slave, serial communications bus that uses an asynchronous protocol and connects keyboards, graphics tablets, mouse devices, and other devices to the Macintosh LC III computer. The 68HC05 microcontroller drives the ADB bus and reads status from the selected external device. ADB devices are attached to the 4-pin mini-DIN connector on the rear panel of the Macintosh LC III. The maximum current draw for the ADB interface is 200 mA. Table 1-11 shows the ADB connector pinout.

Table 1-11 ADB connector pinout

Pin number	Signal name	Signal description
1	ADB	Bidirectional data bus used for input and output. An open-collector signal pulled up to +5 volts through a 470 ohm resistor on the main logic board.
2	PSW	Power-on signal.
3	+5V	+5 volts from the computer. Maximum current draw is 200 mA. A 1-amp fuse at the output satisfies safety requirements.
4	GND	Ground from the computer.

Real-Time Clock and Parameter RAM

The 68HC05 microcontroller provides RTC and PRAM functions for the Macintosh LC III. The microcontroller includes a 32-bit counter that operates similarly to the RTC chip used in certain other Macintosh models. A backup battery allows the 68HC05 to continue counting and preserves the PRAM data even when the computer is turned off.

Low-level access to the RTC and PRAM is accomplished through modified ADB-style commands. Applications that use documented routines to read and write to the RTC and PRAM will work without modification on the Macintosh LC III.

Power-On Reset

When the 68HC05 microcontroller senses that the power supply is turned on, it asserts the Reset signal. The Reset signal, which goes to the processor and other I/O devices, provides time for the processor to stabilize before executing any cycles.

Keyboard Reset and NMI

There are no external reset or NMI switches (commonly referred to as programmer's switches) on the Macintosh LC III computer. These functions are accessible from the keyboard as they are for the Macintosh LC and LC II. You can assert the NMI signal by pressing the keyboard power button and Command key at the same time. NMI is a diagnostic signal that enables debugging software to interrupt execution of an application and switch to the debugger for low-level software and hardware testing. You can force a hard reset, identical to a power-on reset, by pressing the Command key, Control key, and power button at the same time.

Note
You must hold down the above sequence of keys for at least 1 second to allow the microcontroller time to respond to the NMI or hard reset signal. ◆

Processor-Direct Slot

The Macintosh LC III introduces a new 114-pin processor-direct slot (PDS) that allows expansion card designers to take full advantage of the computer's capabilities. This slot also accepts LC-style cards with 96-pin connectors. Most existing cards designed for the Macintosh LC and LC II will work without modification in the Macintosh LC III.

Electrical Description of the PDS

The 114-pin PDS connector is physically divided into two sections. The main section (A1–C32) consists of 96 pins which, with one exception, are identical to the pins on the LC-style PDS. The second section (A35–C40) contains an additional 18 pins that provide the signals necessary to make the slot a true 68030 PDS. Table 1-12 shows the pinout for the connector.

Table 1-12 PDS connector pinout

Pin	Row A	Row B	Row C
1	SNDOUT	CH.GND	/FPU.SEL
2	/SLOTIRQ.E	R/W	/DS
3	/PDS.AS	+5V	/BERR
4	/PDS.DSACK1	+5V	/PDS.DSACK0
5	/HALT	SIZ1	SIZ0
6	FC2	GND	FC1
7	FC0	CLK16M	/RESET
8	/RMC	GND	/PDS.BG
9	D31	D30	D29
10	D28	D27	D26
11	D25	D24	D23
12	D22	D21	D20
13	D19	D18	D17
14	D16	D15	D14
15	D13	D12	D11
16	D10	D9	D8
17	/BGACK	/BR	A0
18	A1	A31	A27
19	A26	A25	A24
20	A23	A22	A21
21	A20	/IPL2	/IPL1
22	/IPL0	D3	D4
23	D2	D5	D6
24	D1	D0	D7
25	A4	A2	A3
26	A6	A12	A5
27	A11	A13	A7
28	A9	A8	A10
29	A16	A15	A14
30	A18	A17	A19

continued

Table 1-12 PDS connector pinout (continued)

Pin	Row A	Row B	Row C
31	/FANSPEED	16MASTER	/FC3
32	+12V	GND	–5V
33	not present	not present	not present
34	not present	not present	not present
35	A28	/CPU.BG	CPU.CLK
36	A29	+5V	A30
37	/CIOUT	/CPU.AS	/STERM
38	/CBACK	/CPU.DISABLE	/CBREQ
39	/SLOTIRQ.D	/CPU.DSACK0	/SLOTIRQ.C
40	CACHE.HIT	GND	/CPU.DSACK1

Note
The 16MASTER signal (B31) functioned as the AIICLOCK input on the Macintosh LC and LC II PDS. The AIICLOCK signal is not required by the Macintosh LC III because the Omega chip generates the 17.2340 MHz Apple II dot clock. ◆

Most of the PDS signals are processor-direct, which means that they are tied directly to signals with identical names on the 68030 processor bus. Some of the signals do not tie directly to the processor but are used to satisfy other functional requirements of the Macintosh LC III computer. Table 1-13 lists the functions of the processor-direct expansion connector signals. Refer to the Motorola *MC68030 Enhanced 32-Bit Microprocessor User's Manual* for a complete description of these signals. Table 1-14 describes the functions of the PDS signals that are not tied directly to the processor.

Table 1-13 Processor-direct expansion connector signals

Signal name	Description
A(0–31)	Address lines
/BERR	Bus error
/BGACK	Bus grant acknowledge
/BR	Bus request
/CBACK	Cache burst acknowledge
/CBREQ	Cache burst request
/CIOUT	Cache inhibit out
/CPU.AS	Address strobe
/CPU.BG	Bus grant
/CPU.DSACK(0–1)	Data transfer and size acknowledge
D(0–31)	Data lines
/DS	Data strobe
FC(0–2)	Function code
/HALT	Halt
/IPL(0–2)	Interrupt priority-level
/RESET	Reset
/RMC	Read-modify-write cycle
R/W	Read/write
SIZ(0–1)	Size
/STERM	Synchronous termination

Table 1-14 Non-processor-direct expansion connector signals

Signal name	Description
16MASTER	Indicates to the main logic board the width of the data port of the PDS card when the card is operating as bus master. A 32-bit PDS card must pull this signal low when it has control of the bus, or simply hardwire the pin to ground. A 16-bit PDS card can ignore this signal because it is already pulled high on the main logic board.
CACHE.HIT	Signals Sonora that a second-level cache on the PDS card can satisfy the current bus transaction. When asserted, Sonora suspends the transaction and allows the PDS card to fulfill the request. Must not be asserted while /CIOUT is active.
CH.GND	Analog chassis ground for I/O connectors and the SNDOUT signal. Do not tie to digital ground.
CLK16M	A general-purpose 15.6672 MHz clock provided for compatibility with Macintosh LC and LC II PDS cards.
CPU.CLK	25 MHz system clock.
/CPU.DISABLE	Disables the 68030 CPU and 68882 FPU (if installed) on the main logic board. This signal would be used by a PDS card that replaces the main processor.
/FANSPEED	Controls the speed of the cooling fan. Digitally grounding this pin increases fan speed and improves thermal performance. Apple recommends that all expansion cards ground this pin.
/FC3	Sonora output signal that indicates the current memory addressing mode. This signal is low when the system is operating in 24-bit mode and slot $E address space is being accessed. The signal is high when slot $E address space is not being accessed in 24-bit mode. This signal is always high when the system is in 32-bit mode, which is the default at startup or reset.
/FPU.SEL	Select signal for an optional floating point coprocessor. This signal is asserted when a coprocessor memory cycle is being performed to CpID 1. Note that only one FPU can be used in the Macintosh LC III. Card developers providing an FPU must either disable the on-board FPU (if installed) using the /CPU.DISABLE signal, or instruct the user to remove the FPU from the main logic board.

continued

Table 1-14 Non-processor-direct expansion connector signals (continued)

Signal name	Description
/PDS.AS	This Sonora output signal is logically an /AS line connected to a processor whose CPU clock is CLK16M. The signal is used to indicate the occurrence of an active bus transaction. /PDS.AS is only asserted when a valid slot address is being generated by the bus master or by an access to the FPU. Accesses in the following range will cause /PDS.AS to be asserted: /FC3 = 0 (24 bit mode) & $xxExxxxx /FC3 = 1 (32 bit mode) & $FExxxxxx | $Exxxxxxx FPU: (FC2-0 = $7) & (A19-16 = $2) & (A15-13 = $1) The release of this line when the PDS card is a slave may not be related to CLK16M. /PDS.AS is only asserted for addresses in the slot $E range. When a PDS card is the active bus master, the card may drive either /PDS.AS or /CPU.AS, but not both.
/PDS.BG	When this Sonora output signal is asserted, a PDS bus master card may take control of the system bus after all pending bus traffic has been completed (/PDS.AS, /BGACK, and all DSACK signals are inactive).
/PDS.DSACK(0–1)	These signals indicate the completion of the data transfer portion of a bus transaction by the addressed slave, and inform the bus master of the size of the data port being accessed during the current transaction. These signals are conditioned to allow a PDS card running at CLK16M to operate in a system where the processor is running at a different speed. These signals are only enabled when /PDS_AS is asserted.
/SLOTIRQ.C	Slot $C interrupt request. Not supported by the Macintosh LC III.
/SLOTIRQ.D	Slot $D interrupt request. Not supported by the Macintosh LC III.
/SLOTIRQ.E	Slot $E interrupt request. Generates an interrupt corresponding to a device in NuBus slot $E.
SNDOUT	Input to the audio amplifier on the main logic board. Allows a PDS card to drive the speaker without involving the CPU.

Load/Drive Limits of the PDS Signals

Table 1-15 provides the load presented or drive available to each pin of an expansion card and indicates whether the signals are inputs or outputs.

In the column labeled *Input/output* in Table 1-15, input refers to a signal from the expansion card to the processor and corresponds directly to the load shown in the column labeled *Load or drive limits*. Output refers to a signal from the processor to the expansion card and corresponds directly to the drive shown in that column. An example may be helpful in interpreting the *Load or drive limits* column. The /RESET line is shown as presenting a load of 100 µA/8 mA, 200 pF. This is the maximum expected load that an expansion card must drive when sending a /RESET signal to the main logic board. The

DC load is given in the format *signal high/signal low*. This means that the expansion card must drive a load of up to 100 uA when it drives /RESET high (logic 1) and a load of up to 8 mA when it drives /RESET low (logic 0). The AC load is given as 200 pF, the maximum capacitance to ground presented by the main logic board to AC signals from an expansion card.

Additionally, /RESET presents a drive of 50 µA/50 µA, 30 pF. This is the maximum amount of drive from the main logic board that is available to integrated circuits on the expansion card. The /RESET line can drive an expansion card DC load of up to 50 µA in both the high state and the low state. The AC drive is given as 30 pF, the maximum capacitance to ground that an expansion card may present to AC signals from the /RESET line.

Table 1-15 PDS signal load/drive limits

Signal name	Input/output	Load or drive limits
16MASTER	Input	Load: 100 µA/4 mA, 20 pF 1 kΩ pull-up
A(0–31)	In/Out	Load: 100 µA/8 mA, 130 pF Drive: 50 µA/400 µA, 30 pF
/BERR	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/1 mA, 30 pF 1 kΩ pull-up
/BGACK	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/1 mA, 30 pF 1 kΩ pull-up
/BR	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/2 mA, 30 pF 1 kΩ pull-up
CLK16M	Output	Drive: 100 µA/100 µA, 20 pF
CACHE.HIT	Input	Load: 100 µA/4 mA, 75 pF
/CBACK	Output	Drive: 100 µA/1 mA, 30 pF
/CBREQ	Input	Load: 100 µA/4 mA, 20 pF 1 kΩ pull-up
CH.GND	In/Out	Chassis ground for I/O and sound. Not to be used for digital ground.
/CIOUT	Output	Drive: 100 µA/1 mA, 30 pF
/CPU.AS	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/2 mA, 30 pF 1 kΩ pull-up
/CPU.BG	In/Out	Load: 100 µA/8 mA, 75 pF Drive: 100 µA/1 mA, 30 pF

continued

Table 1-15 PDS signal load/drive limits (continued)

Signal name	Input/output	Load or drive limits
CPU.CLK	Output	Drive: 100 µA / 100 µA, 20 pF
/CPU.DISABLE	Input	Load: 100 µA / 4 mA, 75 pF 4.7 kΩ pull-up
/CPU.DSACK(0–1)	In / Out	Load: 100 µA / 4 mA, 75 pF Drive: 100 µA / 1 mA, 30 pF 1 kΩ pull-up
D(0–31)	In / Out	Load: 500 µA / 2 mA, 130 pF Drive: 40 µA / 200 µA, 30 pF
/DS	In / Out	Load: 100 µA / 8 mA, 75 pF Drive: 100 µA / 2 mA, 30 pF
FC0	In / Out	Load: 100 µA / 8 mA, 75 pF Drive: 100 µA / 1 mA, 30 pF
FC1	In / Out	Load: 3mA / 1 mA, 75 pF Drive: 100 µA / 1 mA, 30 pF
FC2	In / Out	Load: 100 µA / 8 mA, 75 pF Drive: 100 µA / 1 mA, 30 pF
/FC3	Output	Drive: 1 mA / 1 mA, 20 pF
/FPU.SEL	Output	Drive: 100 µA / 100 µA, 30 pF
/HALT	In / Out	Load: 100 µA / 8 mA, 75 pF Drive: 100 µA / 5 mA, 50 pF 1 kΩ pull-up
/IPL(0–2)	In / Out	Load: 100 µA / 4 mA, 75 pF Drive: 40 µA / 400 µA, 30 pF 1 kΩ pull-up
/PDS.AS	In / Out	Load: 400 µA / 4 mA, 100 pF Drive: 100 µA / 2 mA, 30 pF 4.7 kΩ pull-up
/PDS.BG	Output	Drive: 40 µA / 400 µA, 30 pF
/PDS.DSACK(0–1)	In / Out	Load: 400 µA / 4 mA, 100 pF Drive: 100 µA / 2 mA, 30 pF 1 kΩ pull-up
/RESET	In / Out	Load: 100 µA / 8 mA, 200 pF Drive: 50 µA / 50 µA, 30 pF 1 kΩ pull-up
/RMC	Output	Drive: 100 µA / 2 mA, 75 pF
R/W	In / Out	Load: 400 µA / 8 mA, 100 pF Drive: 40 µA / 1 mA, 30 pF 1 kΩ pull-up

continued

Table 1-15 PDS signal load/drive limits (continued)

Signal name	Input/output	Load or drive limits
SIZ(0–1)	In / Out	Load: 100 µA / 100 µA, 75 pF Drive: 100 µA / 1mA, 30 pF
/SLOTIRQ.C	Input	Load: 100 µA / 8 mA, 20 pF
/SLOTIRQ.D	Input	Load: 100 µA / 8 mA, 20 pF
/SLOTIRQ.E	Input	Load: 100 µA / 8 mA, 20 pF 1 kΩ pull-up
SNDOUT	Input	Use transistor with analog grounded emitter and series resistor (47 kΩ nominal). 47 kΩ pull-up
/STERM	In / Out	Load: 100 µA / 4 mA, 75 pF Drive: 100 µA / 1 mA, 30 pF 1 kΩ pull-up

PDS Power Budget

The DC voltages supplied to the PDS connector and the maximum allowable current load for each voltage are listed in Table 1-16.

Table 1-16 PDS power budget

Voltage	Current load
+5V	800 mA
–5V	20 mA
+12V	165 mA

Power restrictions in the Macintosh LC III computer limit the amount of power that can be dissipated by an expansion card to a maximum of 4 watts. The entire 4 watts can be from the +5-volt supply, or from a combination of the three supply voltages, but the total cannot exceed 4 watts.

▲ **WARNING**
Cards dissipating more than 4 watts may overheat and damage the computer's circuitry or cause it to become inoperable. Apple recommends that all cards ground the /FANSPEED signal to provide increased cooling. ▲

Electrical Design Guidelines for Expansion Cards

This section provides the electrical information you need to design an expansion card for the Macintosh LC III computer.

Addressing Guidelines

Although the Macintosh LC III does not use the NuBus expansion interface, you should design your expansion card to occupy an address location corresponding to the 32-bit address space that would be occupied by a NuBus card in slot space $E. This method of emulating NuBus address space is called *pseudoslot* design. The only additional constraints to your design are the need for a declaration ROM and adherence to some address-decoding rules.

The expansion card address is a function of the memory map selected. The card appears in address space $E0 0000 through $EF FFFF in the 24-bit map and in address space $FE00 0000 through $FEFF FFFF in the 32-bit map. However, to allow the Slot Manager to control your card as though it were a NuBus card in slot $E, software must address the card as if it were in either the 16 MB standard slot space ($FE00 0000 through $FEFF FFFF) or the 256 MB super slot space ($E000 0000 through $EFFF FFFF). This means that you will not have to develop a new software driver because the driver for the NuBus expansion interface will also work with your processor-direct expansion card.

To ensure compatibility with future hardware and software, you should decode all the address bits to minimize the chance of address conflicts. To ensure that the Slot Manager recognizes your card, the declaration ROM must reside at the upper address limit of the 16 MB address space.

Timing Considerations

When designing an expansion card for the Macintosh LC III computer, you should make sure that your card's timing matches the timing requirements of the 68030 microprocessor. For information on the processor's timing requirements, see the *MC68030 Enhanced 32-Bit Microprocessor User's Manual.*

To protect the timing signal margins of the Macintosh LC III main logic board, your design should never extend the processor signals beyond their specified current load limits.

Accessing Memory From the Expansion Card

In the Macintosh LC and LC II, RAM accesses are synchronized to an internal clock in the V8 gate array and serviced only at prescribed intervals. For improved performance in the Macintosh LC III, Sonora examines /CPU_AS and /PDS_AS at the beginning of every clock cycle and immediately services RAM accesses except when they must be postponed for memory refresh or other pending operations. This change should not affect existing PDS cards unless designers have taken specific steps to work around the timing delays of the V8 chip.

Because the VRAM data path is 16-bits wide, PDS bus master cards that access the frame buffer directly must use 8- or 16-bit transfers.

Physical Design Guidelines for Expansion Cards

The "Foldouts" section at the end of this book contains mechanical drawings showing the recommended design guidelines for Macintosh LC III expansion cards. Foldout 1 shows the maximum dimensions of the expansion card and the location of the PDS connector. Foldout 2 provides component height restrictions for the expansion card. Foldout 3 shows how the card mounts to the main logic board.

▲ **WARNING**
The component height restrictions shown in Foldout 2 are critical to your expansion card design. Failure to adhere to these specifications could cause damage to the main logic board. ▲

Expansion Card Connectors

The custom 114-pin PDS connector on the Macintosh LC III main logic board accepts either a 96-pin or 120-pin standard Euro-DIN connector. You can order connectors meeting Apple specifications from Amp Incorporated, Harrisburg, PA 17105. Refer to *Designing Cards and Drivers for the Macintosh Family,* third edition, for more information about these connectors.

CHAPTER 2

Software

This chapter summarizes the new software features of the Macintosh LC III computer, describes how to use the Gestalt Manager to determine whether your software is running on the Macintosh LC III, and defines the system software that is included.

The Macintosh LC III ROM

The ROM used in the Macintosh LC III computer includes all of the features incorporated in the Macintosh LC II, with these additional changes:

- video drivers for the new video modes
- a new floppy disk driver to support the SWIM2 controller
- changes to the Sound Manager to support Sonora
- new hardware diagnostics

These ROM changes are effectively transparent to application software developers. Existing applications will work correctly with the Macintosh LC III computer if they follow the guidelines defined in *Inside Macintosh* and do not address the hardware directly.

Identifying the Macintosh LC III

The correct method for software to identify the Macintosh model it is running on is by using the Gestalt Manager routines described in *Inside Macintosh.*

The `gestaltMachineType` value returned by the Macintosh LC III is 27. This value can be used to obtain the machine name string as described in *Inside Macintosh.*

System Software

The Macintosh LC III computer is shipped with System 7.1 software. A system enabler file for the Macintosh LC III is included on the Install Me First disk, which must be installed before the System 7.1 Install disk.

Foldouts