HP 13220

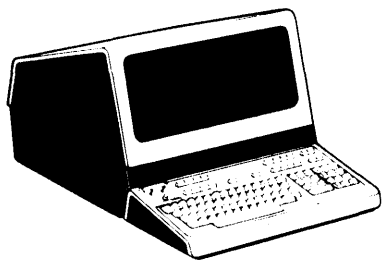
Processor Module

Manual Part No. 13220-91087

REVISED

JAN-04-82

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

Printed in U.S.A.

HP 13220

Processor Module

Manual Part No. 13220-91087

REVISED

JAN-04-82

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

NOTE: This document is part of the 262XX DATA TERMINAL product series Technical Information Package (HP 13220).

1.0 INTRODUCTION

The 02620-60087 Processor PCA performs the terminal logic functions for the 2622A terminal. Its operation is based on the Z80A microprocessor and the National Semiconductor 8367 CRT Controller (CRTC).

The control and I/O section of the Processor PCA provides control signals, input/output and data processing functions. The memory section provides 16K bytes of dynamic RAM for display memory, scratch pad memory and data buffers, and space for up to six 4K or 8K byte ROMs of which 32K are used for complete terminal operation (8K of ROM optional with integral printer). The video control section provides all timing signals for driving the sweep circuitry and video logic as well as performing direct memory access (DMA) of display data. A detailed description of the operation of each of these sections follows in section 3.0.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor Module is contained in tables 1.0 through 4.0

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.1 Inches	Weight (Pounds)
02620-60087	Processor PCA	12.3 x 10.9 x 0.5	1.4

Table 2.0 Reliability and Environmental Information

Environmental:	HP Class B
Restrictions:	Type tested at product level
Failure Rate:	3.71 (percent per 1000 hours)

Table 3.0 Power Supply Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+16 Volt Supply	+12 Volt Supply	+5 Volt Supply	-12 Volt Supply
@ 0 mA	@ 200 mA	@ 2.0 A	@ 50 mA
NOT APPLICABLE			

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J1		** PRINTER **
Pin -1	$\overline{\text{PRINTER}}$	Negative True, Printer Strobe
-2	$\overline{\text{PWR ON/FAIL}}$	Negative True,Power On/Failing
-3	$\overline{\text{WRITE}}$	Negative True, Write signal
-4	$\overline{\text{A1}}$	Negative True, Function select bit 1
-6	$\overline{\text{DATA 0}}$	LSB - Negative True, Data
-7	$\overline{\text{DATA 1}}$	-
-8	$\overline{\text{DATA 2}}$	-
-9	$\overline{\text{DATA 3}}$	-
-10	$\overline{\text{DATA 4}}$	-
-11	$\overline{\text{DATA 5}}$	-
-12	$\overline{\text{DATA 6}}$	-
-13	$\overline{\text{DATA 7}}$	MSB - Negative True, Data
-14	GND	Set printer contrast
-16	$\overline{\text{PINT}}$	Negative True, Printer Interrupt
-17	$\overline{\text{A0}}$	Negative True, Function select bit 0
-18	+5V	Vcc Power
-19	+5V	.
-20	+5V	.
-21	+5V	.
-22	GND	Power Return
-23	GND	.
-24	GND	.
-25	GND	.
-26	GND	.

Table 4.0 Connector Information (Cont'd)

Connector and Pin No.	Signal Name	Signal Description
J2		** POWER SUPPLY **
Pin -1	+5V	+5V Power
-2		N/C
-3	+5V	+5V Power
-4	+12V	+12V Power
-5	GND	Return for Power
-6	GND	Return for Power
-7	PWR ON/FAIL	Negative True, Power On/Failing
-8	-12V	-12V Power
-9	BATTERY	Positive Battery Terminal
-10	BATRET	Negative Battery Terminal
J3		** SWEEP **
Pin -1	HLFBRT	Negative true, Half Bright Video
-2		N/C
-3	RETURN	Return for half bright twisted pair
-4	FULLBRT	Negative true, Full Bright Video
-5	RETURN	Return for Video twisted pair
-6	RETURN	Return for Drive signals
-7	VERDR	Negative True, Vertical Drive
-8	HORDR	Horizontal Drive
J4		** KEYBOARD **
Pin -1	KEY0	Key Data (LSB)
-2	KEY1	Key Data
-3	KEY2	Key Data
-4	KEY3	Key Data
-5	KEY4	Key Data
-6		N/C
-7	KEY5	Key Data
-8	KEY6	Key Data (MSB)
-9	KEYACT	Key Active (Status of key selected)
-10	GND	Power Return
-11	BELL	Bell Line
-12	+5v	+5v Power

Table 4.0 Connector Information (Cont'd)

Connector and pin No.	Signal Name	Signal Description
J5		** DATA COMM **
Pin -1		N/C
-2	+5V	+5V Pod Power
-3	+5V	+5V Pod Power
-4	GND	Power Return
-5	GND	Power Return
-6	GND	Power Return
-7	OCD1	Rate Select (23)
-8		N/C
-9	RD	Received Data (3)
-10		N/C
-11	CS	Clear To Send (5)
-12	DM	Data Set Ready (6)
-13		N/C
-14		N/C
-15	SG	Signal Ground (7)
-16		N/C
-17		N/C
-18	OCR1	Ring Indicator (22)
-19	+12V	+12V Pod Power
-20	-12V	-12V Pod Power
-21	SD	Transmitted Data (2)
-22	RS	Request To Send (4)
-23	TR	Ready (20)
-24		N/C
-25		N/C
-26		N/C
-27		N/C
-28		N/C
-29		N/C
-30		N/C
-31		N/C
-32	GND	Return
-33	SHIELD	Shield Ground (1)
-34		N/C

Notes: (n) denotes the RS-232 pin number

3.0 FUNCTIONAL DESCRIPTION

Refer to block diagram (fig. 1), schematic diagrams (figs. 2,3), timing diagrams (figs. 4-8), component location diagram (fig. 9) and parts list (fig. 10) located in the appendix. The following describes the operation of the three major sections of the Processor PCA; control and I/O, memory, and video control.

3.1 CONTROL AND I/O SECTION

3.1.1 Clock

A 25.7715 MHz crystal is attached to the CRTC which oscillates at the video dot frequency. This is buffered by the CRTC and again by a 74LS244 (U511) to become DRCX, buffered dot rate clock. This clock is then divided by seven by the 74S163 (U611) to produce 3.6816 MHz, which is shaped by Q4 and its associated circuitry to produce a symmetrical clock for the Z80A, which has a zero level < 0.45V and a one level > 4.4V. This clock is also divided by two to produce a 1.8408 MHz clock which the datacomm chip (U613) uses to produce baud rates.

3.1.2 Z80A

The Z80A microprocessor performs the major control and data manipulation functions of the processor PCA. It provides addresses and control signals to read and write data from and to both memory and I/O ports. It also responds to two externally generated interrupts, NNMI and NINT, which, when enabled, interrupt current execution and cause the Z80A to branch to its interrupt service routine. The Z80A also responds to a bus request signal, NBUSREQ, allowing the CRTC control of the system buses.

At power up (or reset) the Z80A begins executing instructions from program memory beginning at address 0000H. A routine is executed which initializes variables and devices according to information contained in non-volatile memory (CMOS) and performs a self test of ROM and RAM. If an error is detected a series of beeps are issued to the keyboard which indicate the failing ROM or RAM. After inintialization the program enters a major loop responding to inputs from the keyboard and datacomm ports.

Three 74LS244's (U47,U57,U511) buffer the address and control lines from the Z80A. The 1 of 8 decoder, U76, is used to separate program memory into six blocks, each 8K bytes long. The addressed ROM is enabled during a memory read by the TNRD and TNMREQ signals or during an instruction fetch by the NM1 signal. Since the time to read the data in an instruction fetch is less than that for a memory read, the NM1 signal was used to provide an early enable of the ROM allowing it to respond within the required time. ROMs with access times of 350 ns from address or 300 ns from enable are required to run the system at full speed. EPROMs or ROMs with 450 ns access times from address may be used by installing jumper W5 and removing jumper W6, which causes the Z80A to wait one cycle longer during instruction fetches. The quad latch U610 and associated gating provides the required wait signal to the Z80A.

3.1.3 I/O Ports

CMOS

The Z80A is capable of addressing 256 different input/output ports. I/O addresses from the Z80A appear on address bits A0-A7 and the accumulator contents appear on bits A8-A15. I/O addresses 0-7FH are used to access locations in the nonvolatile CMOS RAM, U73, where configuration data is stored. Since the CMOS RAM is not fast enough to respond within the I/O cycle time a wait state is generated (by U610) each time the CMOS RAM is accessed. Diodes CR6-CR8 ensure that around 5 volts is always on the CMOS supply pin. Emmitter follower circuit, Q3, makes sure that during a power off the CMOS is always disabled before the Z80A buses become undefined and remains so until buses become defined at power on. During power off the battery maintains CMOS contents. If power on configuration is to be fixed, the COMS RAM may be replaced by an HM7611 PROM (however it must be realized that the standard read/complement/write test for the CMOS self test would show a CMOS error since the prom cannot be written).

DATACOMM

The SY6551 Asynchronous Communications Interface Adapter performs the parallel to serial conversion, error detection and baud rate generation functions required for serial data communication. It appears to the Z80A as four read only and four write only ports with address bit TA2 selecting the read/write function. This is done to compensate for the unique timing of the 6500 series devices. The SY6551 is selected by the rising edge of SELDC which is inverted from U24, the 1 of 8 decoder. The addresses of the SY6551 (U613) are A0-A7H.

The status inputs of the SY6551 produce undesirable results and therefore are forced to their active low states while the necessary status signals are routed through another port. RS-232 line driver, U514, and receiver, U614, are used to convert from TTL levels to RS-232 levels (+-12V) and vice versa. Transmitted signals are: send data (SD), terminal ready (TR), request to send (RS) and optional control driver 1 (OCD1). Received signals are: receive data (RD), data mode (DM), optional control receiver 1 (OCR1), and clear to send (CS).

The datacomm subsystem operates in an asynchronous, full-duplex, point-to-point environment. Characters may be transmitted and received simultaneously (full-duplex) with character flow occurring over random time intervals (asynchronous). To achieve hardware synchronization each character is framed by a start bit and a stop bit (2 stop bits at 110 baud). The addition of the framing bits for transmitted characters and the detection of framing bits for the received characters are done by the SY6551. The parity (for error detection) of the character is selectable (in the datacomm configuration menu) and is also generated and detected by the SY6551 which reports errors (parity, framing, and overrun) to the Z80A by means of a status register in the SY6551 which is read when a character is received. The data transmission and reception rates are set by the Z80A in an internal register within the SY6551.

Rates are selectable (in the datacomm configuration menu) from 110 to 9600 baud.

The datacomm status inputs and outputs provide the necessary control lines to connect the terminal to a host computer via a modem, or to provide direct hardware handshaking between the terminal and host. At power-on the TR and RS lines are activated to indicate that the terminal is ready. Upon receipt of a modem disconnect escape sequence (esc f) the TR line is brought inactive for about two seconds to disconnect the modem. The presence of a modem connection is detected by DM which causes the indicator "LED" (an asterisk '*') to be displayed on the bottom center of the display. The CS signal from the host when active allows the terminal to transmit data and goes inactive to halt transmission (the terminal may ignore CS depending on datacomm configuration). The state of OCD1 is controlled by a configuration strap with its default state being low (inactive). This line selects the modem rate for dual speed modems. OCR1 is monitored in datacomm self test to detect the presence of the loopback test hood. All modem status lines are active high (+12V).

Upon receipt of a character from datacomm the SY6551 generates an interrupt signal (NINT) to the Z80A. This causes the Z80A to branch to the datacomm interrupt service routine which reads the SY6551 status, clearing the interrupt , and if no errors are present, inputs the character and places it into the datacomm buffer in RAM. Characters for which errors (parity, framing or overrun) are present cause a delete character to be placed in the buffer.

TBUS PORTS

The remaining I/O ports are buffered to the Z80A data bus by the biderectional bus driver, U37. This was done because of data bus loading. The signal TNRD selects the direction of the driver which is enabled for all I/O accesses except CMOS RAM and datacomm.

U25 forms the keystatus port located at address 80H. The keystatus port returns the status of 8 keys at a time, which keys are determined by the keyboard/display port (U26). Four bits of the key address (column address) are supplied by U26 (located at address B8H) and three more from the CRTC scan line outputs (row address). As the row address (scan line count) from the CRTC change, keystates are clocked into the keystatus shift register (a high bit indicating key active) from which they are later read. The column address is incremented (during an NMI) for each of the first sixteen display rows thereby scanning the entire range of keyboard addresses.

The keyboard/display port also enables a counter (U114) which counts horizontal sync pulses down to a bell frequency. The bell signal is then shaped by Q4 and its associated circuit. The remaining bits of the keyboard/ display port determine whether enhancements will be enabled and latches the signal which determines the blinkrate of blinking characters.

The NNMI (non-maskable interrupt) signal to the Z80A is masked externally by a D flip-flop (half of U612). Port addresses 88H to 8FH select the NENNMI signal of the port decoder, clocking the latch while address bit TA0 is the data input. This means that a write to port 88H clears the latch, disabling NMI, while a write to port 89H sets the latch enabling NMI.

The system status port, U36, located at address 90H allows the Z80A to read the vertical blank signal (VBLANK) for synchronizing the software with the hardware. It also provides the inputs for the datacomm status signals discussed above and also monitors the integral printer status.

The integral printer port at address 98H buffers data continuously to the printer bus, the data being latched in the printer when the NPRINTER signal is active. The processor writes data and commands to the printer via U16 and half of U15. Printer control is specified by performing a write operation to the printer with address lines TA0 and TA1 and data lines TD0-TD7 selecting the particular function. Printer status is read back from the printer on the upper half of U15 which is enabled for read operations from the printer port. The presence of the printer is detected by reading status from the printer and checking data bit TD1. TD1 will be low if the printer is not connected due to the pullup resistor R1. When the printer is connected to the processor J1 pin 11 is pulled low by the printer therby indicating connection.

Each character in the printer is formed by 30 bytes of dot data, each pair of bytes being made up of the dot data needed to form the character if the character cell is scanned horizontally. The first byte in the pair indicates the state of every other dot while seven bits of the following byte indicate the state of the interstitial dots for the same horizontal scan. Thus fifteen pairs of bytes correspond to fifteen horizontal scans of the character. In this way any character font in a 15 by 15 cell may be created. The printer buffers the data and translates the horizontal dot information into vertical dots for printing. Each 30 bytes of dot data are followed by a print command to print the character. The printer is also able to print in expanded and compressed modes.

The remaining TBUS port located at A8H latches some signals to the video section and one for the datacomm section. The NMODEM signal is inverted to provide the clock for the latch (U35).

3.2 MEMORY SECTION

The Z80A is capable of addressing 65536 (64K) bytes of memory data. The memory map for this processor is shown in the table below.

TABLE 5.0 Terminal Memory Map

0000H	NMI Service Routine Self test code	U63	8K
2000H	Function keys code Datacomm code Configuration code	U64	16K
4000H	Video intrinsics	U65	24K
6000H	Internal printer code	U66	32K
8000H	Not used (CRTC map)	U67	40K
A000H	Not used (CRTC map)	U68	48K
C000H	Dynamic RAM - buffers - display memory - stack - system variables		
	ZD0 : ZD1 : ZD2 : ZD3 : ZD4 : ZD5 : ZD6 : ZD7 U41 : U42 : U43 : U44 : U51 : U52 : U53 : U54		64K

3.2.1 Read-only-memory

As can be seen from the memory map 48 K of address space has been allocated for read-only-memory (ROM). This memory contains the Z80A programs which controls the terminal operation. The ROM space is decoded into six 8K byte blocks by the 74LS138 decoder U76. A jumper on address bit TA12 for each ROM allows the use of either 8K byte or 4K byte ROMs (or EPROMs). Note that 8K bytes of address space is allocated for each ROM device even if it is only a 4K byte ROM (the upper 4K of that block is unusable).

During an instruction (opcode) fetch the Z80A activates the NM1 signal to indicate that an instruction fetch cycle is in process. This signal is used to provide an early enable of the ROM being addressed during an opcode fetch therby allowing the use of ROMs with an access time on 350 ns from address or 300 ns from enable (note that an opcode fetch is one clock cycle shorter than a memory read operation) without wait states. During a memory read from ROM the TNMREQ and TNRD signals go active enabling the addressed ROM. Data is required valid approximately 470 ns from address, therefore no wait states are required for memory reads even when using 450 ns EPROMs. Note that data is placed directly on the Z80A data bus without buffering.

3.2.2 Random-access-memory

The RAM subsystem has been designed around the MK4116-2 (or equivalent) 16K x 1 bit dynamic RAMs. The MK4116-2 has a minimum access time of 150 ns and minimum cycle time of 320 ns. U41-44 and U51-54 supply data bits TD0-TD7 respectively to provide the 16K bytes of RAM data storage.

The RAMs are accessed in three ways: by the Z80A for memory read or write accesses, by the Z80A during a refresh cycle and by the CRTC during a DMA (direct-memory-access) cycle. Each of the three is discussed below. Refer to figure 6.0 for RAM timing.

Z80A READ/WRITE

A Z80A access to RAM is initiated by lowering the TNMREQ signal at an address location between C000H and FFFFH (RAM address range). Prior to TNMREQ going low the output of U77 would be high causing 1's to be shifted through the shift register, U510, by DRCX. As TNMREQ goes low (TNRFSH is high) the output of U77 goes low also. As the clock occurs, 0's are shifted through the shift register causing outputs QA-QD to go low in turn. This produces the RAM timing sequence as follows: NRAS-strobes in row address, MUX-changes RAM address inputs to column address, NCAS-strobes in column address and activates internal RAM circuitry to access the addressed cell. Data ouput on MD0-MD7 is vaild 100 ns from NCAS. When the Z80A is finished accessing the RAM the TNMREQ signal goes high and 1's are shifted through the shift register completing the RAM cycle.

If the Z80A is performing a read operation the TNRD line is lowered along with TNMREQ (TNWR remains high). The TNRD signal is gated with the output of U77 to enable the transparent latch, U62, during the read operation. When the NMUX signal goes high (as MUX goes low) the transparent latch becomes transparent, that is, the outputs follow the inputs, placing the RAM outputs on the Z80A data bus. The latch outputs are enabled until TNRD and TNMREQ go high again.

For a write operation, the Z80A lowers TNMREQ and places the output data on the data bus. Approximately one Z80A clock later the TNWR line goes low strobing the data into the internal data latch in the RAM. The TNRD signal will be high disabling the transparent latch so RAM

outputs will never be on the Z80A data bus. The cycle proceeds as for a read operation with TNMREQ going high, shifting 1's through the shift register to complete the cycle.

Z80A REFRESH

The nature of dynamic RAMs requires that each row must be accessed every two milliseconds to guarantee the contents of that row are held. The Z80A has a built-in refresh function to provide signals which perform dynamic RAM refresh without requiring extra processor overhead. The Z80A maintains a 7 bit memory refresh counter which is incremented following each instruction fetch. While the instruction is being decoded and executed the refresh counter is output on address bits TA0-TA7 while the TNRFSH and TNMREQ signals are brought low, initiating the RAS-MUX-CAS sequence, refreshing that row. Since the TNRD and TNWR signals remain high during the refresh cycle, the memory contents are unaltered and the transparent latch is not enabled so that the accessed byte does not appear on the bus.

CRTC DMA

Twice per video row, on scan lines 6 and 14 (if starting to count from 0), the NBUSREQ signal to the Z80A is activated to allow the CRTC to perform DMA of enhancement and character data (see section 3.3 for more information on the CRTC). The Z80A responds to NBUSREQ at the end of the current machine cycle by tristating its address and control lines and activating the NBUSAK line signalling that the bus is available and will remain so until NBUSREQ is raised. The NBUSAK signal is inverted and buffered by U79 to provide both TBUSAK (active high) and TNBUSAK (active low, buffered). These signals are used to tristate the address and control buffers U47, U57 and U511 and enable the video subsystem for DMA action. TBUSAK enables the CRTC to place the lower 12 bits of the DMA address on the bus and enables the output of the transparent latch, U62, as well as enable the load signal to the shift register, U510. TNBUSAK enables the upper four bits of the DMA address from U74 onto the bus and takes the recirculating line buffer, U38, out of the recirculate mode (see section 3.3 for more information on DMA addressing).

Approximately four character times before the start of the video row the line rate clock (LRC) output of the CRTC goes high enabling the load signal to the shift register through the AND gate U710. The load signal is derived from the character rate clock, LCGAX, which is delayed three dot times through U410 in order to synchronize the RAM access to the video timing and guarantee sufficient address set up time to the RAMs. The load signal causes RAS-CAS shift register , U510, to be parallel loaded on the next rising edge of DRCX (dot rate clock). Upon loading, the shift register output QD is high and QA is low. THis condition forces the output of U77 to go low, causing 0's to be shifted through the shift register. The next three occurances of DRCX produce

the NRAS-MUX-NCAS sequence, accessing the addressed byte. Data is available 100 ns from NCAS, and, since NMUX is high, is placed directly on the Z80A data bus (U62 is in transparent mode), and therefore on the line buffer inputs. As the shift register output QD goes low the output of U77 is forced high and 1's are shifted through the shift register completing the RAM cycle. As MUX goes high again, NMUX goes low causing the data out from the RAM to be latched in the transparent latch, U62, where it is held until the next memory access. As LBCDEL (delayed line buffer clock) goes low the data is clocked into the line buffer U38. The CRTC increments the address and the next load signal occurs 9 dot times from the first, repeating the DMA cycle. In this way 80 sequential bytes of data are fetched from the RAM and loaded into the line buffer during the 80 active video character times of the display.

> Note: Although the shift register load signal is enabled four character times before active video, the CRTC holds the starting address until active video and then increments it during active video. In addition, the data is not clocked into the line buffer until the line buffer clock transitions low during active video.

On the last scan line of a character row, scan line 14, the CRTC lowers the LBRE (line buffer recirculate enable) output, taking line buffers U28 and U39 out of the recirculate mode (where the output is shifted back into the input) thereby allowing data to be clocked into the inputs. During the DMA cycle of scan line 14, as characters are being output from line buffer U39 to the display, characters for the next row are fetched from memory and loaded into line buffer U39. At the same time, as enhancement data is shifted out from U28, the data which was previously stored in the temporary line buffer U38 (during the DMA cycle of scan line 6) is shifted into U28. In this way the display data for the next row of characters is loaded into the line buffers during the last scan line of the previous row as it is being displayed on the screen.

3.3 VIDEO CONTROL SECTION

3.3.1 Overview

The video control section generates the timing signals required to fetch character and enhancement data from memory and drive the analog sweep circuitry to display that information on the CRT.

The display is divided into 26 rows of 80 character cells each. Each character cell is a rectangle, 15 dots vertical by nine dots horizontal. Any character to be displayed is produced by selectively lighting the dots of the character cell which shape that character, leaving the others blank. Dots are left blank on either side and on the top and bottom of the character cell to provide horizontal and vertical seperation between normal characters. This is not true of characters which are continuous across the character boundary, such as line drawing characters (used to display forms).

The analog sweep circuitry sweeps the electron beam from left to right and from top to bottom across the display. As the beam is swept horizontally it is turned on to produce a lighted dot and off to blank a dot position. As the beam reaches the end of its scan a horizontal sync signal is sent to the sweep causing the beam to retrace horizontally and begin sweeping again. During this time the beam is also being swept vertically. The combination of these two produces the display raster. As the beam reaches the bottom of the display a vertical sync signal is sent to the sweep causing the beam to retrace from the bottom right to the top left corner. In this manner the CRT display is written 60 times per second (when configured at 60 Hz) or optionally 50 times per second (configured at 50 Hz).

HORIZONTAL TIMING

After the 80th character position of a scan line the beam is turned off (blanked) and remains so as the horizontal retrace takes place. The beam is enabled again as it reaches the position for the first character of the next scan. This blanking interval is called "horizontal blanking". This blanking allows time for the beam to retrace, settle at the left side and begin tracing again. The portion of the scan where the beam is enabled is known as "active video". The horizontal scan time consists of the 80 character times of active video plus 35 character times of horizontal blanking for a total of 115 character times per scan (1 character time = 349 ns). This produces a horizontal scan frequency of 24.9 KHz.
The horizontal sync signal is activated 16 character times before the last video character of the scan and is active for 7 character times. It is produced in advance of the last character to compensate for the delay in the sweep horizontal centering circuit.

VERTICAL TIMING

The 26 active video rows of the display each require 15 horizontal scans for a total of 390 active video scans. After the last scan line of the last row is displayed, a vertical blank signal is activated which disables the electron beam during the vertical retrace time. The beam is enabled again on the first scan line of the first row. The duration of the vertical blank interval depends upon the occurance of the vertical sync signal which triggers the vertical retrace. This vertical sync timing depends in turn on the frequency with which the frame (one entire display) is refreshed. This frame rate may be configured to either 50 or 60 Hz corresponding to the AC line frequencies in foreign countries or the U.S. to eliminate display interference between the power supply and CRT. The following table describes the timing relationships between the vertical blank and vertical sync signals and the frame rate.

TABLE 6.0 Frame Timing

	Frame Rate 60 Hz	50 Hz
Delay after v. blank to v. sync (# scan lines)	0	38
v. sync width (# scan lines)	19	64
v. blank duration (# scan lines)	25	108
Total # scan lines per frame	415	498

3.3.2 Display memory addressing

Section 3.2.2 describes how the CRTC performs DMA to load the line buffers with character and enhancement data for display. Before it performs DMA, the CRTC must be loaded with a starting address (called the row-start address). Each time the CRTC is enabled it fetches 80 consecutive bytes of data starting from the row start address and places it into one of the recirculating line buffers.

The Z80A maintains a table of 24 row start addresses in memory indicating the addresses of the first byte of character data for each of the character rows being displayed. Rows 25 and 26 contain the soft key labels and are always accessed from fixed locations. This table is actually a subset of a larger table which contains row-start addresses for all 48 display rows. The address of the first enhancement byte of a row is the first character byte address offset by 80.

Two scan lines prior to the NBUSREQ signal being activated a non-maskable interrupt (NMI) is generated which causes the Z80A to branch to the NMI service routine after completing the current instruction. Part of this service routine writes the row-start address for the next DMA into the rowstart register of the CRTC. The row-start address is written into the CRTC via the address bus itself. At the same time, bits TA13 and TA12 are written into the 74LS175 U75, which provides the upper bits of the RAM address for DMA. The Z80A reads the row start address from the table, adds the 80 byte offset for enhancement data DMA, masks bits TA15 and TA14 to a 1 and 0 respectively and then writes a 02H to this address. By masking bits TA15 and TA14 the address corresponds to a ROM location, which of course can't be written. These bits are decoded by part of U27 and U32, along with TNMREQ and TNWR to generate the register load signal (U412 pin 38) which latches the address into the CRTC and U75 for use during the next DMA cycle. The data bits ZD0 and ZD1 select the register to be written to, in this case, the row-start register. The NMI service routine keeps count of the next row to be displayed in order to determine which row start address to send to the CRTC next. Since NMI can be disabled for an indefinate period (for example during a RAM test) it is resynchronized every frame by reading the VBLANK signal through the system status port.

3.3.3 Character display

At any given time the characters for the current row being displayed are held in the recirculating line buffer U39. The character codes output from this line buffer are resynchronized to the character clock through the octal latch, U310, from which they are sent to the character ROM, U311. This ROM contains the dot pattern for each scan line of each each possible character code. The standard character set uses the ASCII character code to represent the 128 possible characters in the set. The first 32 characters of the set are the control characters (escape, line feed, carriage return, etc.) while those remaining are the alphanumeric and punctuation characters. These 128 characters are represented in bits X0-X6 with X7 being a 0. These bits along with the scan line count become addresses for the dot data from the character ROM. Therefore, 11 address bits are required, meaning that a 2K byte ROM may be used to contain the dot data for the standard character set. Bit X7 will then serve as an active low chip select.

By using a 4K byte character ROM, two complete character sets may be displayed. In this case bit X7 selects between the two character sets. Likewise an 8K byte ROM can store four complete, 128 character, character sets. The schematic shows a signal from the enhancement data latch, U29 pin 15, which is inverted by U212, and sent to U311 pin 21. This signal is used to address the 8K byte character ROM on 4K boundaries. This combined with bit X7 from the character data latch allows selection of any of the four character sets. This uppermost address bit becomes a chip select for 2K or 4K character ROMs.

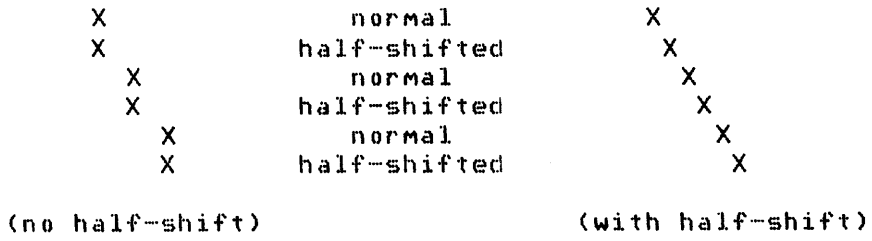
As the character code and scan line count is issued to the character ROM an access time delay is encountered before the dot data is available at the outputs. The character ROM has an access time of 300 ns, therefore one full character time (349 ns) delay is introduced.

As the dot data becomes available out of the character ROM the LVSRX (load video shift register, buffered) signal is brought low which, on the rising edge of DRCX, parallel loads the data from the character ROM into the character shift registers U312 and U313 (and U314 as explained later). Since only seven dots per scan line are required for standard characters, seven dots are loaded from the character ROM (low output means dot is lit) into the shift registers. The MSB (most significant bit) output from the character ROM is latched by U18 (on LCGAX clock) and is used to enable the half-shift function (described below). The MSB output of U312 is connected to the serial input of U313 essentially forming an 8 bit shift register. At the same time that the seven dots are loaded into the shift register a 1 is loaded into the MSB.

The QD output of U313 goes to the character multiplexor, U213. This multiplexor selects one of several inputs to gate to the dot stream. For a normal scan (not half-shift) the multiplexor select inputs will be 101 (C input is most significant) selecting the D5 input. As the dots are loaded into the shift register the first dot (which is high) appears on the D5 input of the multiplexor and is gated to the dot stream. On each of the next 8 dot rate clocks (DRCX) dot data is shifted one bit position in the shift register and therefore to the D5 multiplexor input and to the dot stream. Since the serial input of U312 is tied high, a 1 (blank dot) is shifted into the shift register as the dot data is shifted out. Therefore at the end of the 9 dot clocks comprising the horizontal scan for a standard character, the first and last dots are blanked (1's) with the 7 dots from the character ROM in between.

HALF-SHIFT

To avoid the "stairstep" appearance of characters with long diagonals, a feature known as "half-shift" is implemented which allows and scan line of a character to be delayed by half a dot time. This half-shifted scan line, placed between two normal scan lines, fills in the diagonal as shown below.



In the standard character set the MSB output of the character ROM indicates that a scan line is to be halfshifted. This output is latched (by LCGAX) into U18 where it is held for the 9 dots of the character time. The output of U18 is fed to the character multiplexor select input A which, for half-shifted scan lines, selects the D4 input (U213 pin 15). The QD output of the dot shift register, U313, is sent to the JK flip-flop, U413, clocked on the falling edge of DRCX, which performs the half-shift of the dot data. The output of this flip-flop goes to the D4 input of the character multiplexor. The half-shift flip-flop is preset by LVSRX at the time new dots are loaded into the shift registers.

COPY BIT

Some alternate character sets such as line drawing set or large character set require all nine dots an a scan line to be active. This allows for continuous dots across a character boundary as required for drawing forms, etc. on the display. In order to get nine dots out of eight outputs from the character ROM, a copy bit circuit is activated which copies the MSB output into the first two dots while the remaining seven ROM outputs form the remaining seven dots.

The seven least significant ouputs from the character ROM are loaded into shift registers U312 and U313 as for standard characters. The most significant output is loaded into both the A and B inputs of shift register U314 at the same time as the least significant seven bits. Thus, the MSB is "copied" in shift register U314. The remaining dots are brought from the QC output of U313 into the serial inputs of U314 thereby forming a nine bit shift register with U312, U313, and U314. The QB output from U314 is then fed to the D7 and D6 inputs of the character multiplexor which are selected when the select inputs are 11X. Note that the select A input is a don't care since half-shift cannot be used in these character sets.

The copy bit circuit is activated whenever the X7 output of of the character latch U310 is active. Remember that this bit is activated to select the second character set in a 4K character ROM or the second and fourth sets in an 8K character ROM. The first 32 character of any of the four posible character sets are reserved for control characters and therefore copy bit is deactivated when these positions are accessed. This condition is decoded by bits X5 or X6 being gated with X7 (U34 and U112) to enable copy bit only for the upper 96 characters of the set. The result of this decoding is latched in the JK flip-flop, U413, which allows for the access time of the character ROM. The flip-flop is clocked by the combination of LVSRX and DRCX which are gated together by U411. The output of the copy bit enable latch is then used to select the copy bit shift register output and gate it to the dot stream.

CURSOR

The generation of the cursor for the display is performed by a combination of hardware and software. The CRTC activates its cursor output when the address of the character being fetched during a DMA cycle matches the contents of its internal cursor address register. This output is active for all scan lines. The software maintains and updates this register in the CRTC corresponding to the position of the cursor on the display. In order to make the cursor blink the software alternately writes a valid cursor address and then an invlaid one.

The cursor signal, CUR, output from the CRTC is gated with another signal, ULTIME, to produce a cursor signal, NCUR, which is active on the 13th scan line. ULTIME is decoded from the scan line count by U59 and U411. This signal also enables the underline enhancement during the 13th scan line.

In the normal situation, where the cursor does not lie in an underline field, the NCUR signal is propogated thru U19 to become NCURSOR which is fed to the select C input of the character multiplexor. This input goes low to activate the cursor which for normal characters (not copy bit) selects the D0 or D1 inputs which are tied low. This causes the dot stream to be active for the 13 scan line of the character position in which the cursor lies. In effect this OR's the cursor with the character in the cell (a non-destructive cursor). If the copy bit circuit is active however, the D2 of D3 inputs of the character multiplexor are selected. These inputs provide the inverted series of dots from the copy bit shift register. In essence this inverts the 13th scan line of the character when the cursor is active. This is necessary rather than the OR'd cursor used above due to the fact that some of the characters may have all dots of the 13th scan line lit and the cursor would never be seen.

DOT STRETCH

The dots are inverted by U213, the character multiplexor, to provide an active high dot stream output. This dot stream is then passed through Q1 and its associated circuitry which performs a "dot stretch" function. This dot stretch is used to provide an elongated active dot which has a more pleasant appearance when displayed. It essentially "fattens up" the dots composing a character. The switching time of the transistor from saturation to cutoff is dependent upon the parasitic collector to base capacitance and the external capacitor C2. This capacitance limits the switching speed, essentially stretching the amount of time the transistor is active (in saturation). Capacitor C3 is included to compensate for parasitic base to emitter capacitance. Note that an inversion is introduced by this dot stretch circuit.

After being stretched, the dot stream is gated through U110 where it picks up the underline enhancement and then is sent to the enhancement multiplexor where the remaining enhancements are added before sending the information to the analog sweep circuitry.

3.3.4 Enhancement Display

A one-to-one correspondence exists between each byte of character data and each byte of enhancement data held in recirculating line buffers U39 and U28 respectively. As a byte of character data is sent to the character ROM its corresponding enhancement byte is sent to the enhancement section where it is decoded and recombined with the dot stream in the enhancement multiplexor, U211.

Of the eight available bits in the enhancement byte, only seven are used. Four of these, EN0-EN3, select the blink, inverse, underline and halfbright attributes which may be selected in any combination. Bit EN4 is the set enhancement bit which, when high, causes the current enhancement to be latched and held until another enhancement is set or until the end of the current row. Bit EN5 is the end-of-line bit which causes the display to be from the current character to the end of the row. In this way, to clear the display, end-of-line is set in the first character postion of each row. Bit EN6 as described above forms the most significant address bit for an 8K byte character ROM.

As a character is latched into U310, six of the seven enhancement bits are latched into the hex latch, U29. The set enhancement bit is latched at the same time (by LCGAX) into U18. At this time EN6 is fed to the character ROM to provide the character ROM address selection for its corresponding character. The attribute bits, EN0-EN3, output from U29 are then sent to the 74LS163, U210. In this mode, with the count enable inputs P and T grounded, it acts as a latch with a synchronous load and clear. This latch provides the additional character time delay to compensate for the character ROM access time. If the set enhancement bit, EN4, is set, the output, U18 pin 3, will go low as the bit is latched. This activates the load input of U210 causing the attributes to be loaded on the next character clock (when the character ROM outputs are loaded into the shift register).

VIDEO ATTRIBUTES

The blink attribute output (U210 pin 14) is gated with the blinkrate signal from the I/O section, which alternates high and low to produce the active low NBLINK signal. When active the NBLINK signal allows only the cursor to be displayed, blanking the character. In this way, the blinking characters are alternately displayed and blanked. The inverse bit simply selects the inverted dot stream (ALPHA) or cursor signals.

The underline signal, ULINE, under normal conditions (when cursor is not active) simply causes the dot stream to be turned on during scan line 13. This is accomplished by gating the ULINE signal with ULTIME and using the results to force U110 pin 8 high, thereby activating the dot stream. A problem exists, however, when we want to position the cursor at a character position where underline is active. We can no longer merely "OR" in the cursor into the dot stream because it lies on the same scan line as the underline and therefore would never be seen. What is done instead is that when both are active (NCUR is low and ULINE is high), neither the cursor nor underline appear on the display. This essentially disables the underline at the cursor position on the display producing a blinking hole in the underline. The NCUR signal is sent into U110 pin 3 which, when active, prevents the underline signal from being gated into the dot stream. At the same time the ULINE signal is sent into U19 pin 13 disabling the NCURSOR signal which normally generates the cursor. Thus, both are disabled.

The last attribute, halfbright, selects which of the video inputs on the analog sweep board will receive the dot information. When the halfbright attribute is activated the dot information is inhibited from the NFULLBRT output (which gives full intensity characters), U112 pin 6, by pulling U112 pin 4 low, and is enabled through U110 pin 8 which sends the active low dot information on NHALFBRT to the sweep.

END-OF-LINE

The remaining enhancement bit, EN5, performs the end-of-line function. When set, this bit causes the display to be blanked from the current character position to the end of the row. This eliminates the need to clear both character and enhancement data in order to clear the display. After being latched in U29 the end-of-line signal is gated through U19 and U27 to lower the clear input of U210 (pin 1). This causes the enhancements to be cleared at the next character clock (when character ROM outputs are loaded into the shift registers). At the same time that U210 is cleared, the endof-line signal is latched into U17. The Q' output (U17 pin 8) is sent back to the preset input to hold the flip-flop in the cleared state for the rest of the scan line. At the end of the scan line the NLRCX (inverted line rate clock) clears the flip-flop (clear overrides preset). At the same time the Q' output, NEOLDEL, is gated through U111 to activate the BLANK signal. This signal blanks the display by deselecting the alpha input, only allowing the cursor signal to be gated to the sweep. The cursor signal is allowed since it is necessary to be able to position the cursor even in a blanked field. The Q output, U17 pin 9, is gated to the clear input of U210 in order to hold the enhancement latch in the cleared state.

The horizontal blank signal causes the dot stream to be disabled (blanked) after the 80th character of a row and holds it in the blanked state until the first character of the next row. This signal is obtained by latching the LBCX (line buffer clock) signal in U18 pin 12 and adding a one character delay in U18 pin 5. The LBCX signal is active high at the rising edge of LCGAX during the 80 active video characters. HBLANK is then gated through U27 to activate BLANK and disable NCUR. VBLANK and DISPOFF also blank the display in a similar fashion.

The last part of the video section to consider is the enhancement off circuit which allows the enhancement latches to be disabled. The Z80A sets the ENHOFF signal, output from U26, which is latched by the RECIRC signal into U17. The Q output (U17 pin 5) is gated through U27 to clear U210 while the Q' output (U17 pin 6) clears U29. The RECIRC signal goes low to take the line buffers out of the recirculate mode as they are loaded during scan line 14. This means that the ENHOFF bit is always latched at the start of a new row. The software can then change ENHOFF during an NMI service routine to disable enhancement display on the next row.

4.0 GLOSSARY OF SIGNAL NAMES

This section lists the signal names used on the schematic drawings, figures 1.0 and 2.0, along with a brief description of their use. Note: an 'N' prefix generally indicates an active low signal, otherwise the signal is active high; a 'T' prefix or an 'X' suffix indicate that the signal is buffered.

1.84 MHZ	–	The 1.84 MHz datacomm chip clock
3.68 MHZ	–	The 3.68 MHz Z80A clock
60 HZ	–	Sets the video frame rate, low = 50 Hz
ALPHA	–	video dot stream after dot stretch
BATT+ or BATT–	–	connection to the battery + (or –) terminal for CMOS backup during power off
BELL	–	output signal to drive the keyboard bell
BLANK	–	inhibits the ALPHA dot stream from being sent to the sweep circuitry
BLINKRATE	–	alternates at the blinkrate for blinking character attribute
CE	–	detects presence of loopback hood
CS	–	clear-to-send from host computer
CTS	–	TTL level clear-to-send
CUR	–	cursor output from CRTC
DISBRQ	–	inhibit DMA
DISPOFF	–	blank entire display
DM	–	detect modem connection
DRCX	–	dot rate clock
DSR	–	TTL level detect modem connection

EN0-EN7	-	enhancement data bits from line buffer
ENHOFF	-	inhibit enhancements
ENNMI	-	clock for NMI mask latch
HBLANK	-	horizontal blank signal
ICH	-	TTL level detect datacomm test hood
INVERSE	-	select inverse video attribute
KEY0-KEY6	-	keyboard row/column scan outputs
LBCDEL	-	delayed line buffer clock
LBCX	-	line buffer clock
LCGADEL	-	delayed latch character generator address
LCGAX	-	latch character generator address
LVSRX	-	load video shift register
MD0-MD7	-	RAM data outputs
MUX	-	selects between row and cloumn address for dynamic RAM
NBLINK	-	select blink attribute
NBUSREQ	-	request bus control for DMA
NCAS	-	column address strobe for RAM
NCMOSREQ	-	enable CMOS for read/write
NCUR	-	one line cursor signal
NURSOR	-	cursor active without underline
NENNMI	-	select NMI latch
NEOLDEL	-	end-of-line signal
NFULLBRT	-	normal intensity video output
NHALFBRT	-	half-intensity video output

NHSYNC	-	horizontal synchronization
NINT	-	datacomm interrupt
NKEYACT	-	key active (depressed) on keyboard
NKEYDISP	-	select (clock) keyboard/display latch
NKEYSTAT	-	enable keystatus port
NLRCX	-	line rate clock
NM1	-	opcode fetch machine cycle
NMODEM	-	select (clock) modem/display latch
NMUX	-	clock RAM output latch
NNMI	-	non-maskable interrupt (video)
NPFAIL	-	power fail signal from power supply
NPRINTER	-	printer select signal
NRAS	-	row address strobe for dynamic RAMs
NRESETA	-	power-on reset, driver A
NRESETB	-	power-on reset, driver B
NSELDC	-	datacomm port select
NSYSSTAT	-	system status port select
OCD1	-	optional control driver 1, datacomm
OCR1	-	optional control receiver 1, datacomm
PINT	-	printer interrupt status
PULLUP	-	common pullup resistor
RD	-	receive data, datacomm
RECIRC	-	line buffer recirculate enable
RESET	-	printer reset signal
RS	-	request to send, datacomm
SD	-	send data, datacomm

SELDC	-	datacomm chip select
SG	-	signal ground, datacomm
SHIELD	-	shield (earth) ground, datacomm
SMEM0-SMEM5	-	ROM0-ROM5 chip enable
TA0-TA15	-	address bits 0-15
TBUSAK	-	bus acknowledge, Z80A tristate
TD0-TD7	-	buffered data bus
TNBUSAK	-	active low bus acknowledge
TNMREQ	-	Z80A memory request
TNRD	-	memory or I/O read select
TNRFSH	-	dynamic RAM refresh active
TNWR	-	memory or I/O write select
TR	-	terminal ready, datacomm
ULINE	-	select underline attribute
ULTIME	-	active on scan line 13, indicates scan line for underline or cursor display
VBLANK	-	vertical blank signal
VSYNC	-	vertical synchronization signal
X0-X7	-	character code address to character ROM
ZD0-ZD7	-	Z80A data bus

FIGURE 1.0 PROCESSOR BLOCK DIAGRAM

Figure 1
Block Diagram
JAN-04-82

13220-91087

NOTES:
1. JUMPERS SHOWN IN STD CONFIG.

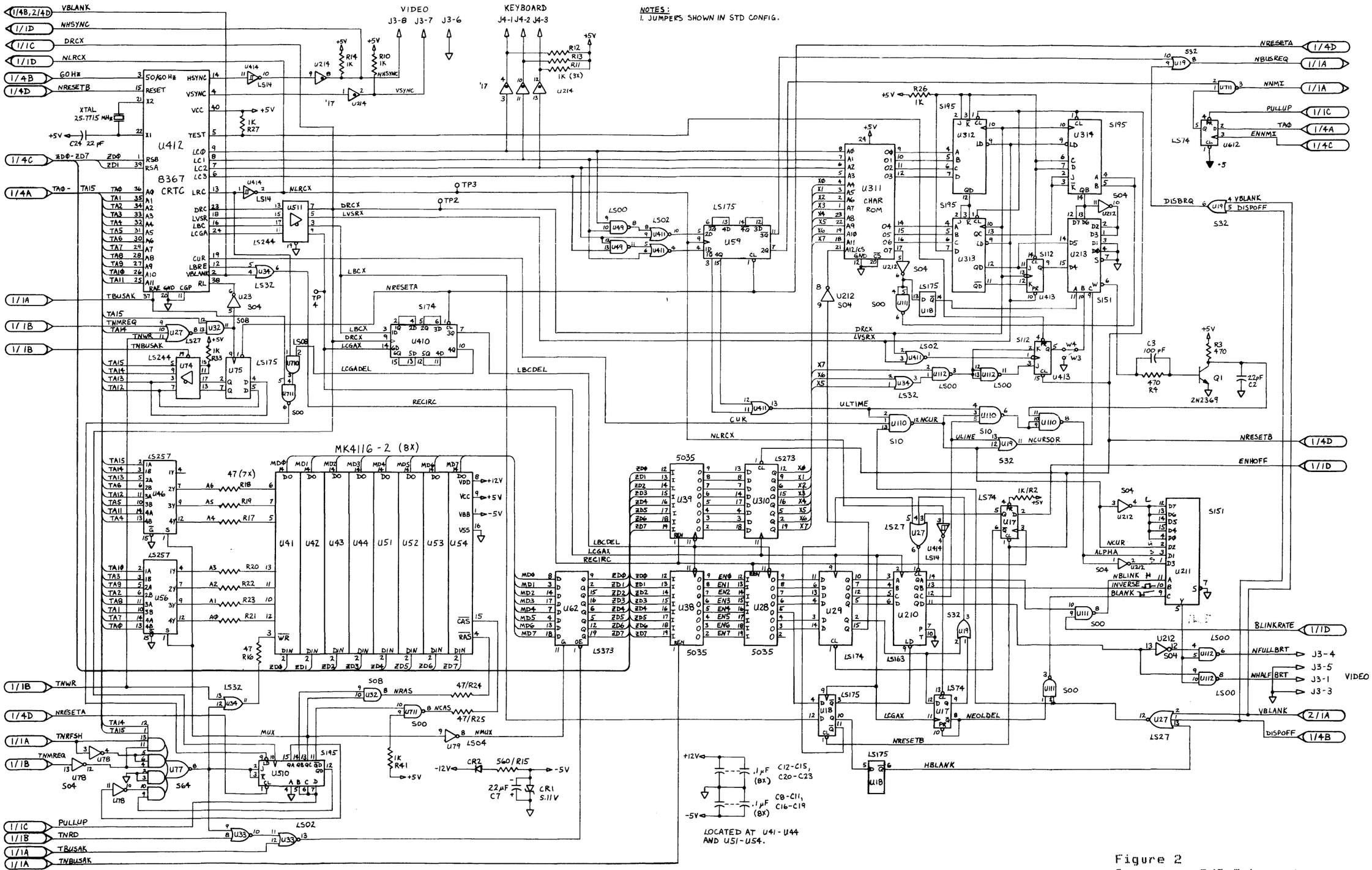


Figure 2
Processor I/O Schematic
JAN-04-82 13220-91087

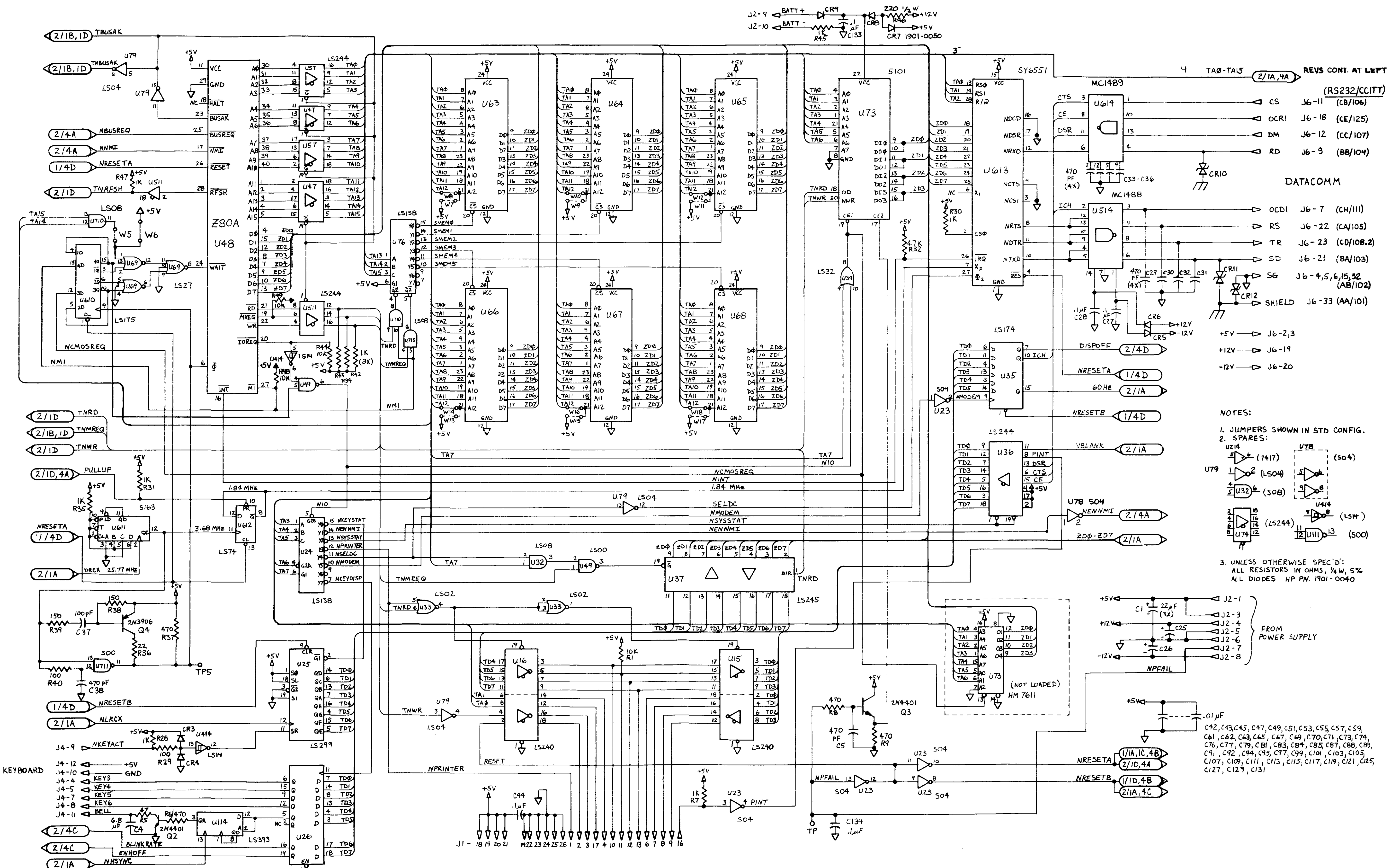


Figure 3
RAM/Video Schematic
JAN-04-82 13220-91087

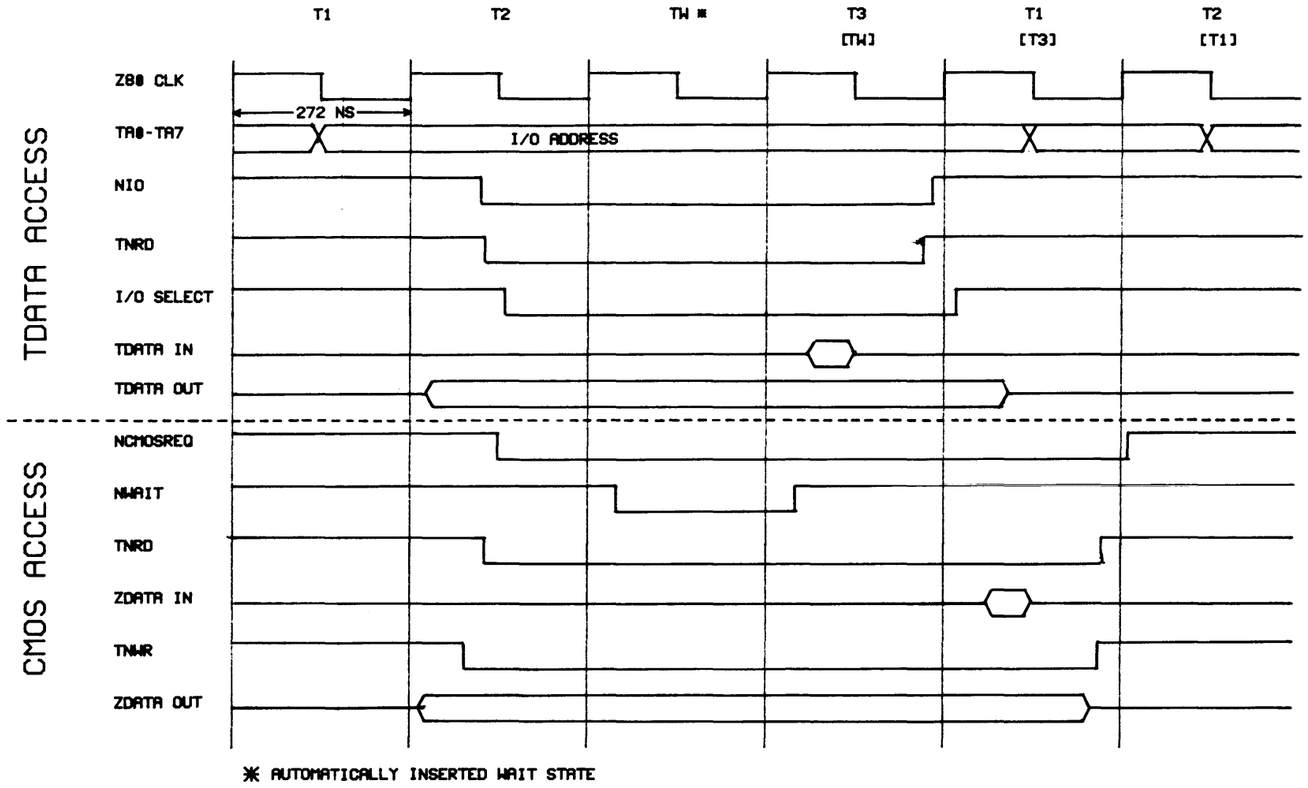


FIGURE 4.0 Z80A I/O TIMING

Figure 4
I/O Timing Diagram
JAN-04-82 13220-91087

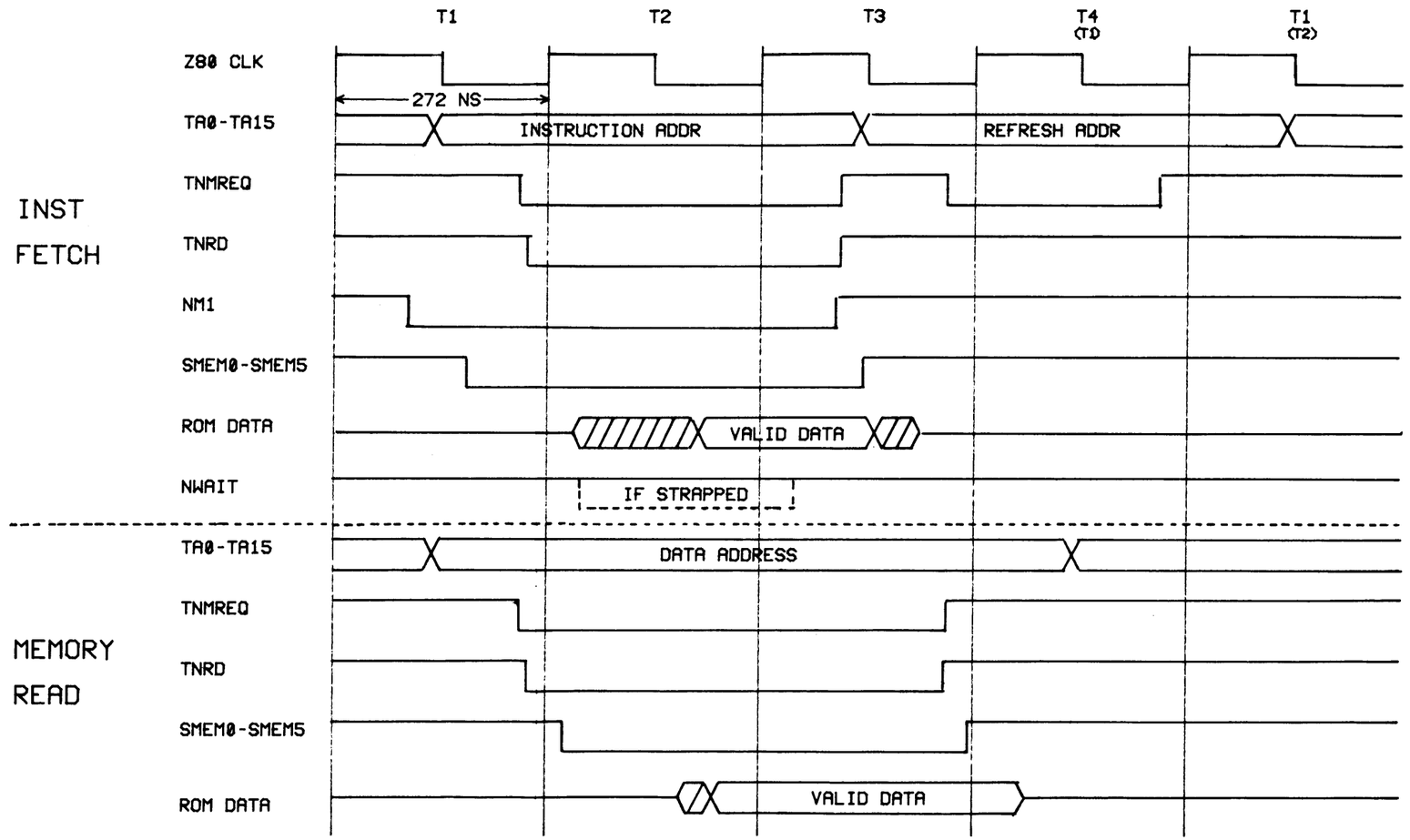


FIGURE 5.0 Z80A ROM TIMING

Figure 5
ROM Timing Diagram
JAN-04-82 13220-91087

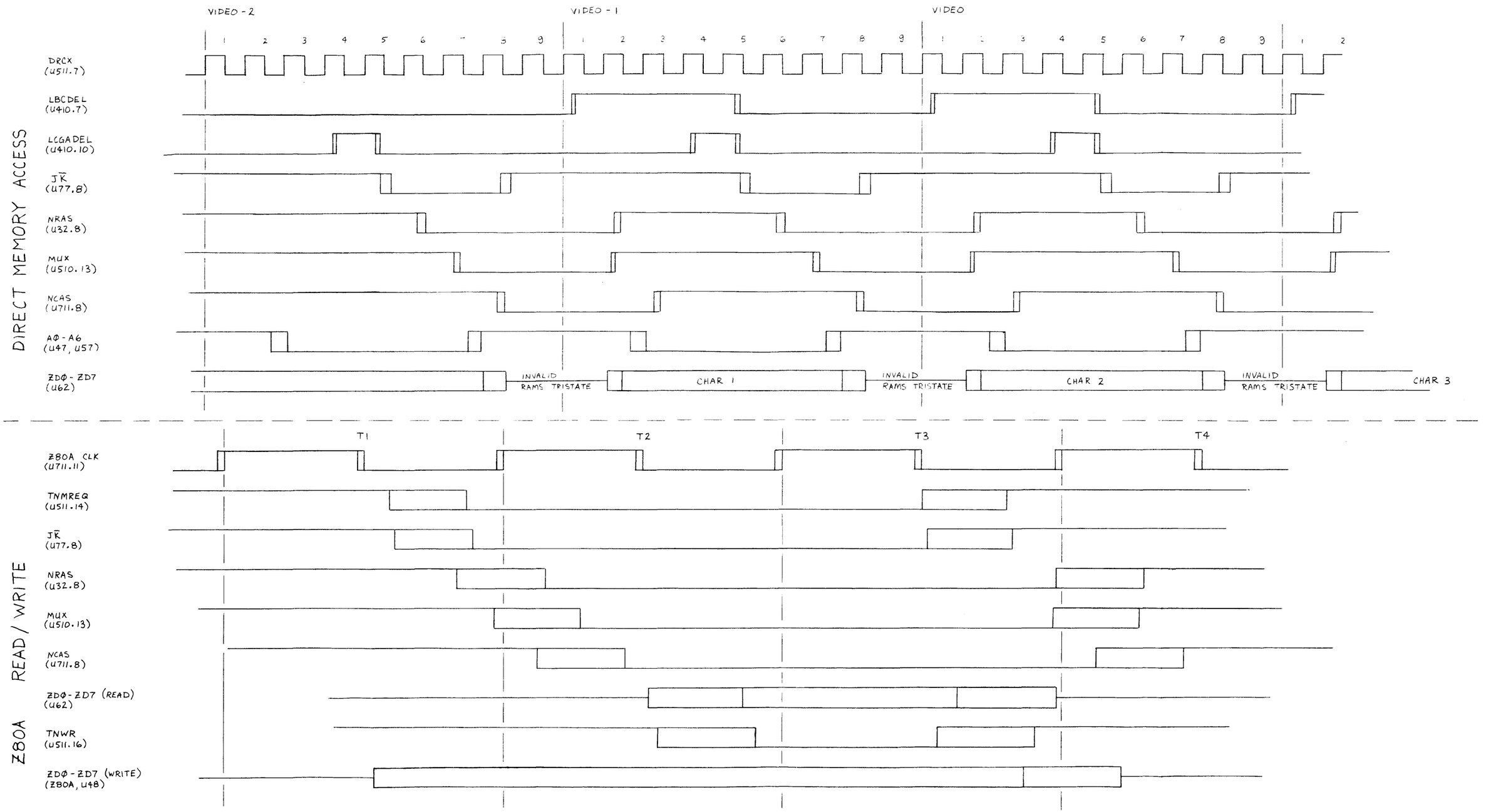


FIGURE 6.0 RAM TIMING

RAM Timing Diagram
JAN-04-82 13220-91087

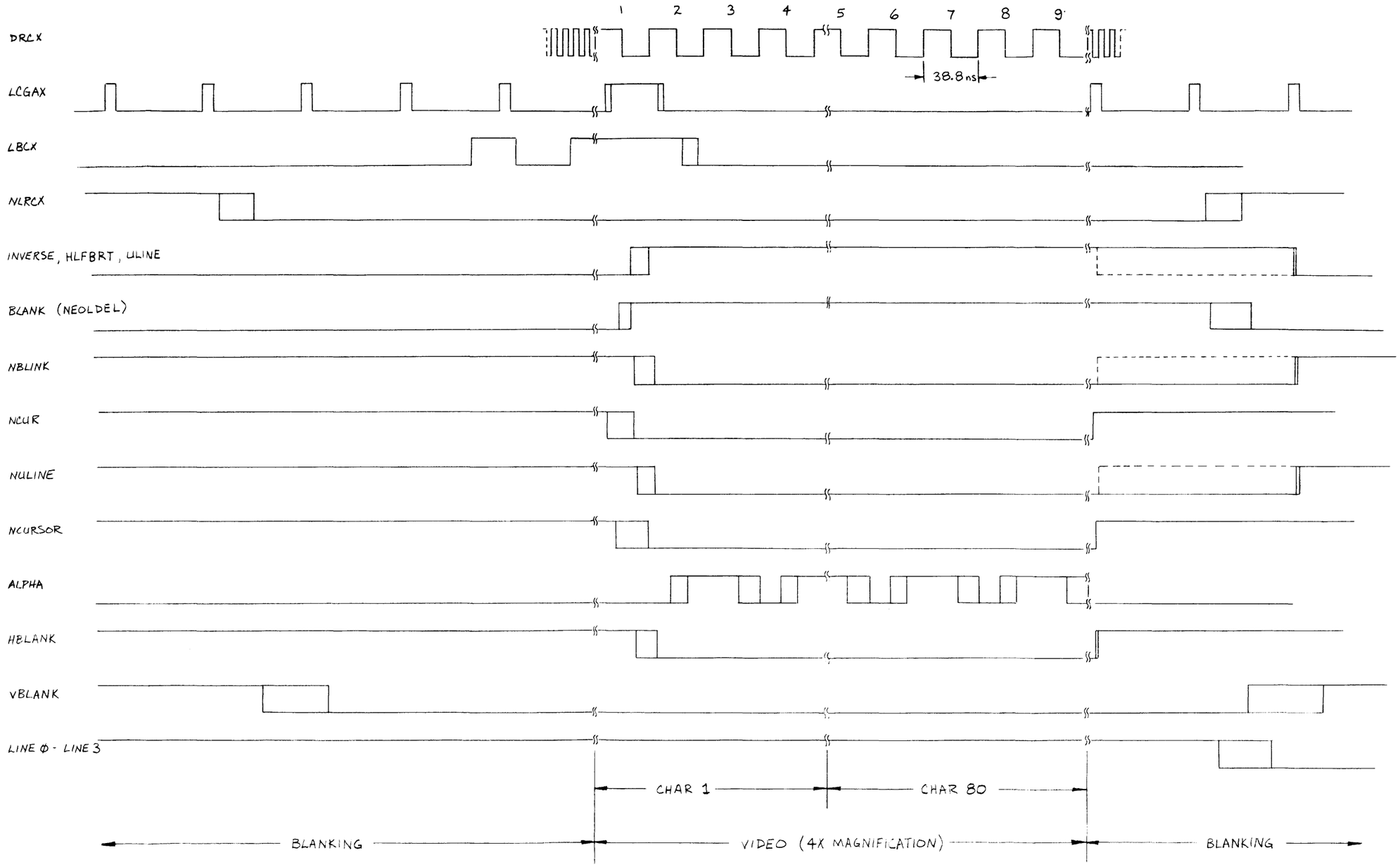


FIGURE 7.0 VIDEO LINE RATE TIMING

Figure 7
Video Line Rate Timing Diagram
JAN-04-82 13220-91087

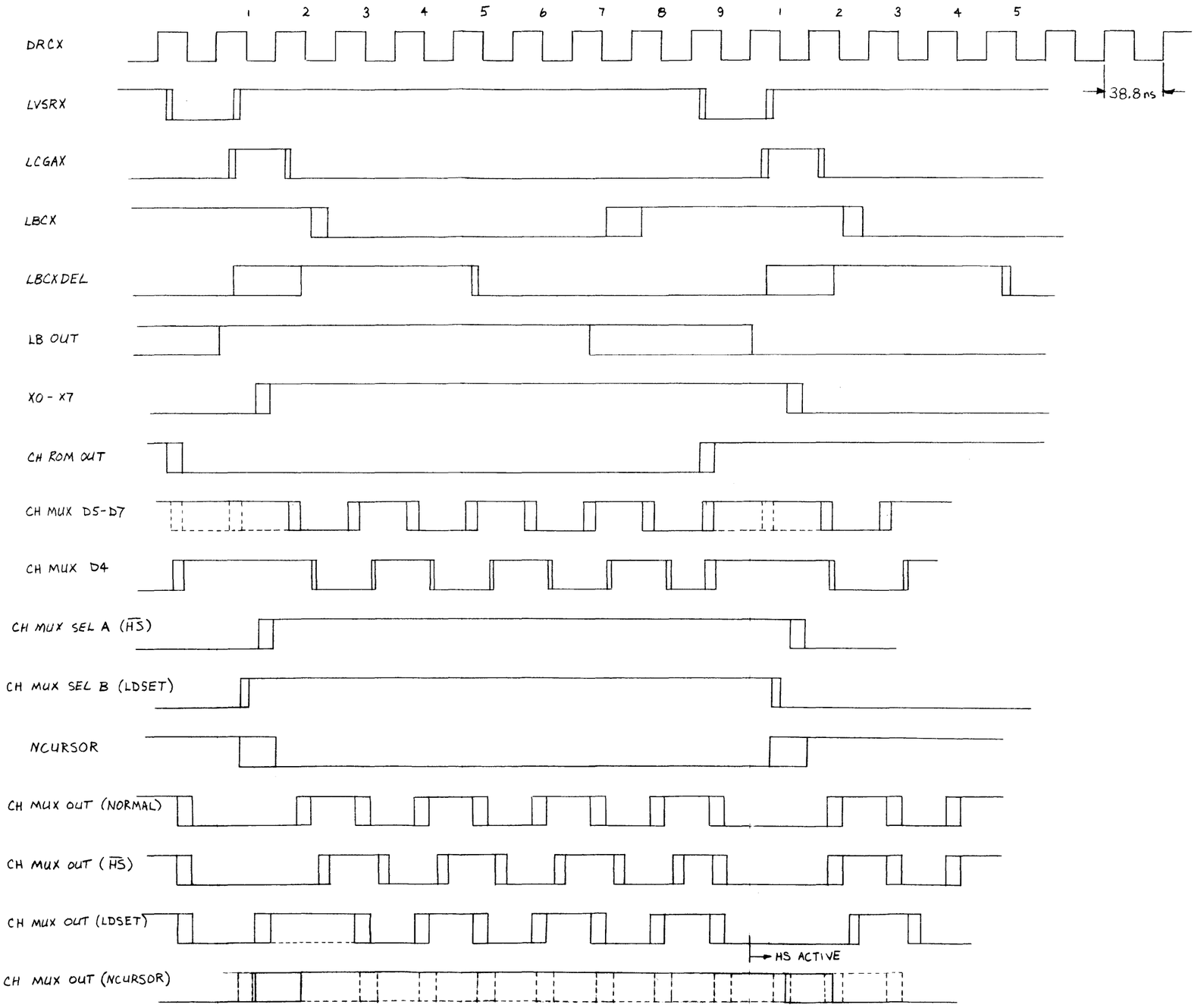
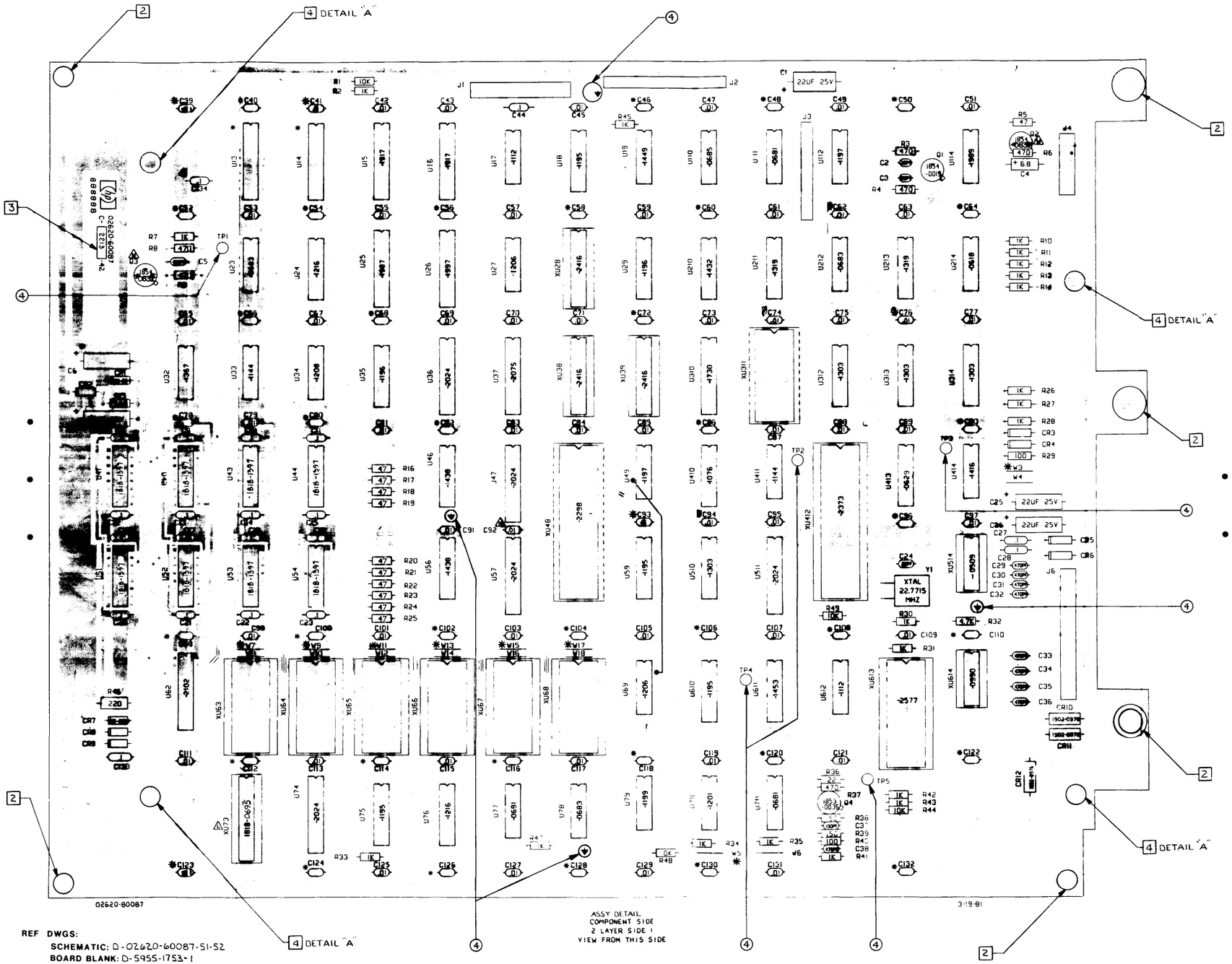
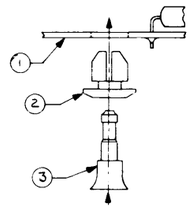


FIGURE 8.0 VIDEO CHARACTER TIMING

Figure 8
Character Timing Diagram
JAN-04-82 13220-91087



REF DWGS:
SCHEMATIC: D-02620-60087-51-52
BOARD BLANK: D-5955-1753-1
DRILL DWG: D-02620-80087-4



DETAIL A NO SCALE

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS,
ALL RESISTORS 1/8W ,1% ¼W, 5%
ALL CAPACITANCE IN MICROFARADS,
ALL IC S PART NUMBERS PREFIXED BY 1820-
ALL TRANSISTORS HP PN 1854-0467
ALL DIODES HP PN 1901-0040
[2] MASK BEFORE LOADING.
[3] MARK DATE CODE (OPER 33)
[4] INSTALL IN POST SOLDER LOADING FROM CIRCUIT SIDE (4 PLACES). PRESS ITEM 2 INTO P.C. BOARD FIRST, THEN INSTALL ITEM 3 INTO ITEM 2, SEE DETAIL 'A'.
5. DO NOT LOAD ITEMS DENOTED BY ASTERISK *.
C6, C39-41, C46, C48, C50, C52, C54, C56, C58, C60, C64, C66, C68, C72, C78, C80, C82, C86, C90, C93, C96, C98, C100, C102, C104, C106, C108, C110, C112, C114, C116, C118, C120, C122-124, C126, C128, C130, C132, W3, W5, W7, W9, W11, W13, W15, W17, U13, U14.
6. LOAD IN PRETEST:
U28, U38, U39, U48, U73, U412, U612
7. CUT U49.5 (COMPONENT SIDE) JUMPER U49.5 TO U69.13
8. VERIFY W6 WAS LOADED.

Figure 9
Component Location Diagram
JAN-04-82 13220-91087

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	02620-60087	9	1	PROCESSOR PCA - 2622A	28480	02620-60087
C2	0160-4787	8	2	CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C3	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C4	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
C5	0160-3335	0	10	CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C7	0180-2879	7	3	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C8	0160-4557	0	21	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C11	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C13	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C21	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C22	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C24	0160-4787	8		CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C25	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C26	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C27	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C28	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C29	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C30	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C31	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C32	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C33	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C34	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C35	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C36	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C37	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C38	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C42	0160-4554	7	52	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C43	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C44	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C45	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C47	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C49	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C51	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C53	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C55	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C57	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C59	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C61	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C62	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C63	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C65	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C67	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C69	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C70	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C71	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C73	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C74	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C75	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C76	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C77	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C79	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C81	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C83	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C84	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C85	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C87	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C88	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C89	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C91	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C92	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C94	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C95	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C97	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C99	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C101	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C103	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C105	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C107	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C109	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C111	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C113	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C115	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C119	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C121	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C125	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C127	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C129	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C131	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C133	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C134	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C176	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
CR1	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
CR2	1901-0040	1	7	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR7	1901-0050	3	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR8	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR9	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR10	1902-0976	4	3	DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR11	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR12	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
J1	1251-5500	9	1	CONNECTOR 26-PIN M POST TYPE	28480	1251-5500
J2	1251-5521	4	1	CONNECTOR 9-PIN M POST TYPE	28480	1251-5521
J3	1251-5520	3	1	CONNECTOR 7-PIN M POST TYPE	28480	1251-5520
J4	1251-5499	5	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5499
J6	1251-5546	3	1	CONNECTOR 34-PIN M POST TYPE	28480	1251-5546
Q1	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1854-0467	5	2	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q3	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q4	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
R1	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R2	0683-1025	9	17	RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R3	0683-4715	0	6	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R4	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R5	0683-4705	8	11	RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R6	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R7	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R8	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R9	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R10	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R11	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R12	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R13	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R14	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R15	0683-5615	1	1	RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
R16	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R17	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R18	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R19	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R20	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R21	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R22	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R23	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R24	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R25	0683-4705	8		RESISTOR 47 5% 25W FC TC=-400/+500	01121	CB4705
R26	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R27	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R28	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R29	0683-1015	7	2	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R30	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R31	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R32	0683-4725	2	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R33	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R34	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025
R35	0683-1025	9		RESISTOR 1K 5% 25W FC TC=-400/+600	01121	CB1025

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R36	0683-2205	9	1	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R37	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R38	0683-1515	2	2	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R39	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R40	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R44	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R45	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R46	0686-2215	7	1	RESISTOR 220 5% .5W CC TC=0+529	01121	EB2215
R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R48	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R49	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
U15	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U16	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U17	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U18	1820-1195	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U19	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U23	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
U24	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U25	1820-1987	5	1	IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT	01295	SN74LS299N
U26	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U27	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U28	1820-2416	7	3	IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U29	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U32	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U33	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U34	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U35	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U36	1820-2024	3	5	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U37	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U38	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U39	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U41	5081-2705	3	8	16K RAM	28480	5081-2705
U42	5081-2705	3		16K RAM	28480	5081-2705
U43	5081-2705	3		16K RAM	28480	5081-2705
U44	5081-2705	3		16K RAM	28480	5081-2705
U46	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U49	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U51	5081-2705	3		16K RAM	28480	5081-2705
U52	5081-2705	3		16K RAM	28480	5081-2705
U53	5081-2705	3		16K RAM	28480	5081-2705
U54	5081-2705	3		16K RAM	28480	5081-2705
U56	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U57	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U59	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U62	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U69	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U74	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U75	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U76	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U77	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U78	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U79	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U110	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U111	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U112	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U114	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U210	1820-1432	5	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U211	1820-1319	7	2	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
U212	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U213	1820-1319	7		IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
U214	1820-0618	7	1	IC BFR TTL NON-INV HEX	01295	SN7417N
U310	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U312	1820-1303	9	4	IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U313	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U314	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U410	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U411	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U412	1820-2373	5	1	IC-NAT 8367 CRT C	28480	1820-2373
U413	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U414	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U510	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U511	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U514	1820-0509	5	1	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U610	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U611	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U612	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U613	1820-2577	1	1	IC-SYP 6551 ACIA	28480	1820-2577
U614	1820-0990	8	1	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U710	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U711	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
W4	8159-0005	0	8	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W8	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W10	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W12	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W14	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W16	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W18	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XU28	1200-0639	8	3	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU38	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU39	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU41	1200-0607	0	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU42	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU43	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU44	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU48	1200-0654	7	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU51	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU52	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU53	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU54	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU63	1200-0541	1	7	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU64	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU65	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU66	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU67	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU68	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU73	1200-0612	7	1	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU311	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU412	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU514	1200-0638	7	2	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU613	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
XU614	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
Y1	0410-1224	3	1	CRYSTAL-QUARTZ 25.7715 MHZ HC-25/U-HLDR	28480	0410-1224
	0360-0124	3	9	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
	1200-0546	6	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
	1390-0104	3	4	FASTENER-SNAP-IN GROM PANEL THKNS	28480	1390-0104
	1390-0281	7	4	FASTENER-SNAP-IN PLGR PANEL THKNS	28480	1390-0281
	1818-0695	5	1	IC CMOS 1024 (1K) STAT RAM 450-NS 3-S	04713	MCM145101-1P

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11961	SEMICON INC	BURLINGTON	MA	01803
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247