HEWLETT PACKARD

SERVICE MANUAL

HP 1650B/1651B

Logic Analyzer

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

2924A

For additional information about serial numbers see
INSTRUMENTS COVERED BY THIS MANUAL
in Section 1.

Manual Part No. 01650-90915
Microfiche Part No. 01650-90815

Printed in U.S.A. August 1989

Agilent Technologies

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This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

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ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CWA789

Safety Considerations

General Operation

This is a Safety Class I instrument (provided with terminal for protective earthing). BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

General Warnings and Cautions

- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Safety Symbols

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates Hazardous Voltages

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

Warning 

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

Caution 

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software and/or firmware code may be printed before the date; this indicates the version level of the software and/or firmware of this product at the time of the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 August 1989 01650-90915

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in Printing History and on the title page.

Pages	**Effective Date**
all	August 1989

Contents

Section 1: General Information

Section 2: Installation

Section 3: Performance Tests

Section 4: Adjustments

Section 5: Replaceable Parts

Section 6: Service

Contents

Section 1 General Information

1

General Information

Introduction

This service manual explains how to test, adjust, and service the HP 1650B and HP 1651B Logic Analyzers. This manual is divided into six sections:

- General Information
- Installation
- Performance Tests
- Adjustments
- Replaceable Parts
- Service

This section of the manual includes a description of the HP 1650B/51B Logic Analyzers, specifications, options, available accessories, and recommended test equipment.

Listed on the title page of this manual is a microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest manual changes supplement and pertinent service notes.

Instruments Covered by this Manual

The instrument serial number is on the rear panel. Hewlett-Packard uses a two part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter (0000A00000). The prefix is the same for all identical instruments and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each instrument. This manual applies directly to instruments with the serial prefix shown on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a manual changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual change supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

Safety Considerations

This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operating. Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this instrument.

Hewlett-Packard assumes no liability if the customer fails to comply with these safety requirements.

Product Description

The HP 1650B is an 80-channel STATE/TIMING (35 MHz/100 MHz) logic analyzer, selectable in 16-channel groupings. The HP 1651B is a 32-channel STATE/TIMING (25 MHz/100 MHz) analyzer, also selectable in 16-channel groupings. The user interface for both models consists of a panel keyboard with an RPG knob and a 9-inch, white-phosphor, high-resolution CRT for information display. A 3.5-inch Sony disk drive, for setup storage and information retrieval, is integral to the analyzers. An RS-232-C port, HP-IB port, and external arming trigger are available on the rear panel. The RS-232-C and HP-IB ports are used for printer hardcopy or for logic analyzer control via a controller. Either port can be used for hardcopy or control.

The following items are other main features of the logic analyzers.

- Simultaneous state/state, or simultaneous state/timing analysis.
- Time interval; number of states; pattern search; minimum, maximum, and average time interval statistics.
- Transitional timing to store data only when there is a transition.
- Clock qualifiers, storage qualification, time and number of state tagging, and prestore.
- Small lightweight, passive probing.

Accessories Supplied

The following accessories are supplied with the HP 1650B/51B Logic Analyzer.

- Woven probe cable (HP part number 01650-61607) with 40-pin connector on each side, 17 signal lines, 17 return lines, 2 power lines, and 2 power ground lines. Each power line supplies + 5 volts for preprocessor power. Each cable supplies 600 milliamperes with a maximum power available from the HP 1650B/51B of 2 amperes. Five probe cables are supplied with the HP 1650B and two are supplied with the HP 1651B.
- Probe Tip Assemblies (HP part number 01650-61608) that provide 16 data channels, 1 clock channel, and 1 ground lead per pod assembly. The probe input specifications are listed in table 1-1. Five Probe Tip Assemblies are supplied with the HP 1650B and two are supplied with the HP 1651B.
- Grabbers for the probe tip assemblies are supplied in packages of 20 (HP part number 5959-0288). 100 grabbers (5 packages) are supplied with the HP 1650B and 40 grabbers (2 packages) are suppied with the HP 1651B.
- Two operating system disks.
- One 2.3 meter (7.5 feet) power cord. See section 2 for available power cords.
- One operating and reference manual set.
- One service manual.
- One RS-232-C Loopback Connector.

Accessories Available

The following accessories are available for the HP 1650B/51B Logic Analyzer.

- Termination Adapter - HP Part Number 01650-63201.
- Soft Carrying Case - HP Part Number 1540-1066.
- HP 1008A /006 Testmobile.
- HP 92192A 3.5-inch Microfloppy Disks (box of ten)
- Rackmount Kit - HP Part Number 5061-6175.
- HP Model 10269C Probe interface to connect the logic analyzer directly to microprocessor preprocessors.
- Preprocessors for specific microprocessors and bus systems (for more information contact your Hewlett-Packard Sales and Service Office).

Logic Analyzer Specifications

The following specifications are the performance standards or limits against which the HP 1650B/51B Logic Analyzer is tested.

Probes

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy:	Voltage Range	Accuracy
	-2.0V to + 2.0V	± 150 mV
	-9.9V to -2.1V	± 300 mV
	+ 2.1V to + 9.9V	± 300 mV

State Mode

Clock Repetition Rate: Single phase is 35 MHz maximum. With time or state counting, minimum time between states is 60 ns (16.67 MHz). Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by ≥ 50 ns.

Clock Pulse Width: ≥ 10 ns at threshold.

Setup Time: Data must be present prior to clock transition, ≥ 10 ns.

Hold Time: Data must be present after rising clock transition; 0 ns.

Data must be present after falling clock transition, 0 ns (HP 1651B); data must be present after falling L clock transition, 0 ns (HP 1650B); data must be present after falling J, K, M, and N clock transition, 1 ns (HP 1650B).

Timing Mode

Minimum Detectable Glitch: 5 ns wide at the threshold.

Operating Characteristics

The following operating characteristics are are typical operating characteristics for the HP 1650B/51B Logic Analyzer.

Probes

Input RC: 100 KΩ ± 2% shunted by approximately 8 pF at the probe tip.

TTL Threshold Preset: + 1.6 volts.

ECL Threshold Preset: -1.3 volts.

Threshold Range: -9.9 to + 9.9 volts in 0.1V increments.

Threshold Setting: Threshold levels may be defined for pods 1 and 2 individually (HP 1651B). Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5 (HP 1650B).

Minimum Input Overdrive: 250 mV or 30% of the input amplitude, whichever is greater.

Maximum Voltage: ± 40 volts peak.

Maximum Power Available Through Cables: (600 mA) 2/3 amp @ 5V per cable; 2 amp @ 5V per HP 1650B/51B.

Measurement Configurations

Analyzer Configurations:

Analyzer 1	Analyzer 2
Timing	Off
Off	Timing
State	Off
Off	State
Timing	State
State	Timing
State	State
Off	Off

Channel Assignment: Each group of 16 channels (a pod) can be assigned to Analyzer 1, Analyzer 2, or remain unassigned. The HP 1650B contains 5 pods; the HP 1651B contains 2 pods.

State Analysis MEMORY

Data Acquisition: 1024 samples/channel.

Trace Specification

Clocks: Five clocks (HP 1650B) or two clocks (HP 1651B) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier: The high or low level of four ORed clocks (HP 1650B) or one clock (HP1651B) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. Eight pattern recognizers are available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on.

Range Recognizers: Recognizes data which is numerically between or on two specified patterns (ANDed combination of 0s and/or 1s). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits and on a maximum of 2 pods.

Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels: There are eight levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first seven sequence levels.

Branching: Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.

Occurrence Counter: Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.

Storage Qualification: Each sequence level has a storage qualifier that specifies the states that are to be stored.

Enable/Disable: Defines a window of post-trigger storage. States stored in this window can be qualified.

Prestore: Stores two qualified states that precede states that are stored.

Tagging

State Tagging: Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4 X (10 to the 12th power).

Time Tagging: Measures the time between stored states, relative to either the previous state or the trigger. Maximum time between states is 48 hours.

With tagging on, the acquisition memory is halved; minimum time between states is 60 ns.

Symbols

Pattern Symbols: User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs. Bit pattern can include 0s, 1s, and don't cares.

Range Symbols: User can define a mnemonic covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of 0s and 1s. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.

Number of Pattern and Range Symbols: 200 total used for both analyzers.

Symbols can be down-loaded over RS-232-C or HP-IB.

Timing Analysis

Transitional Timing Mode

Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period: 10 ns.

Maximum Time Covered By Data: 5000 seconds.

Minimum Time Covered by Data: 10.24 us.

Glitch Capture Mode

Data sample and glitch information stored every sample period.

Sample Period: 20 ns to 50 ms in a 1-2-5 sequence dependent on sec/div and delay settings.

Memory Depth: 512 samples/channel.

Time Covered by Data: Sample period X 512.

Waveform Display

Sec/div: 10 ns to 100 s; 0.01% resolution.

Delay: -2500 s to 2500 s; presence of data dependent on the number of transitions in data between trigger and trigger plus delay (transitional timing).

Accumulate: Waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. Primary use is to view summary of bus activity.

Maximum Number Of Displayed Waveforms: 24

Time Interval Accuracy

Channel to Channel Skew: 4 ns typical.

Time Interval Accuracy: ± (sample period + channel-to-channel skew + 0.01% of time interval reading).

Trigger Specification

Asynchronous Pattern: Trigger on an asynchronous pattern less than or greater than specified duration. Pattern is the logical AND of specified low, high, or don't care for each assigned channel. If pattern is valid but duration is invalid, there is a 20 ns reset time before looking for patterns again.

Greater Than Duration: Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is + 0 ns to -20 ns. Trigger occurs at pattern + duration.

Less Than Duration: Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is + 20 ns to -0 ns. Trigger occurs at the end of the pattern.

Glitch/Edge Triggering: Trigger on glitch or edge following valid duration of asynchronous pattern while the pattern is still present. Edge can be specified as rising, falling or either. Less than duration forces glitch and edge triggering off.

Measurement and Display Functions

Autoscale (Timing Analyzer Only)

Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming: Each analyzer can be armed by the run key, the other analyzer, or the external trigger on rear panel.

Trace Mode: Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until stop is pressed or until time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels

Channels may be grouped together and given a six character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. Primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and 0) are shown as dashed lines on the display.

Trigger: Displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval: The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (State Analyzer Only): The X and 0 markers measure the number of tagged states between one state and trigger, or between two states.

Patterns: The X and 0 markers can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The 0 marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: X to 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

Run/Stop Functions

Run: Starts acquisition of data in specified trace mode.

Stop: In single trace mode or the first run of a repetitive acquisition, STOP halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts acquisition of data and does not change current display.

Data Display/Entry

Display Modes: State listing; timing waveforms; interleaved, time-correlated listing of two state analyzers (time tagging on); time-correlated state listing and timing waveform display (state listing in upper half, timing waveform in lower half, and time tagging on).

Timing Waveform: Pattern readout of timing waveforms at X or 0 marker.

Bases: Binary, Octal, Decimal, Hexadecimal, ASCII (display only), and User-defined symbols.

General Characteristics

The following general characteristics for the HP 1650B/51B are the environmental operating conditions, shipping weights, and instrument dimensions.

Operating Environment

Temperature: Instruments, 0° to 55° C (+ 32° to 131°F); probes and cables, 0° to 65°C (+ 32° to 149°F). Recommended temperature range for disk media, 10° to 50°C (+ 50° to 149°F).

Humidity: Instruments up to 95% relative humidity at + 40°C; (104°F). Recommended humidity range for disk media, 8% to 80% relative humidity at + 40°C (+ 104°F).

Altitude: To 4600 m (15,000 ft).

Vibration:

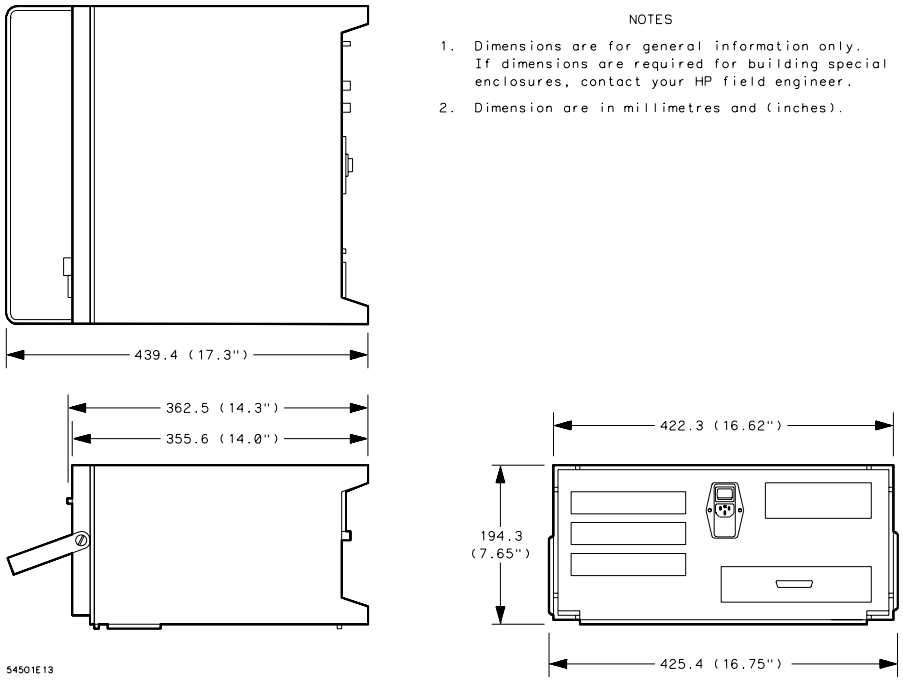
Operating: Random vibration 5-500 Hz, 10 minutes per axis, &2.41 g (rms).

Non-operating: Random vibration 5-500 Hz, 10 minutes per axis, & 2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

Weight: 10.0 kg (22 lbs) net; 18.2 kg (40 lbs) shipping.

Power: 115V/230V, 48-66 Hz, 200 W maximum.

Dimensions: See outline drawing below.



Recommended Test Equipment

Table 1-1 lists the test equipment required to test performance, make adjustments, and troubleshoot the HP 1650B/51B Logic Analyzers. The table includes the critical specifications of the test equipment and lists each procedure in which the equipment is required. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Recommended Test Equipment

Equipment Required	Critical Specifications	Recommended Model	Use *
Oscilloscope	dual channel dc to 300 MHz	HP 54502A	P,T
Pulse Generator	5 ns pulse width 20 ns period 1.3 ns risetime double pulse 100 kHz Repetition Rate Overshoot: 5% of Amp.	HP 8161A/020	P
Power Supply	+ or - 10.2 V output current: 0 - 0.4 amperes	HP 6216B	P
Adapter	BNC(f)-to-Dual Banana	HP Part Number 1251-2277	P
DMM	5.5 digit resolution	HP 3478A	A
Resistor	2 ohms, 25 watts	HP Part Number 0811-1390	T
BNC Cable (2)	50 ohms with UG-88C/U BNC (m) connectors	HP 10503A	P
BNC Adapter (2)	BNC tee (m) (f) (f)	HP Part Number 1250-0781	P
BNC Feedthrough	50 ohm BNC	HP 10100C	P

* P = Performance Tests, A = Adjustments, T = Troubleshooting

Section 2

Installation

2

Installation

Introduction

This section of the manual contains information and instructions necessary for setting up the HP 1650B/51B Logic Analyzer. This includes inspection procedures, power requirements, hardware connections and configurations, and packaging information.

Safety Considerations

The safety symbols used with Hewlett-Packard instruments are illustrated in the front of this manual. WARNING and CAUTION symbols and instructions should be reviewed before operating the instrument. These warnings and cautions must be followed for your own protection and to avoid damaging the instrument.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, keep it until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment are listed under "Accessories Supplied" in Section 1. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate properly, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

Power Requirements

The HP 1650B/51B Logic Analyzer requires a power source of either 115 Vac or 230 Vac, -22% to + 10%; single phase, 48 to 66 Hz, 200 Watts maximum power.

Caution

BEFORE CONNECTING POWER TO THIS INSTRUMENT, be sure the Line Voltage Select switch on the rear panel of the instrument is set properly and the correct fuse is installed.

Line Voltage Selection

When shipped from the factory, the line voltage selector is set and an appropriate fuse is installed for operating the instrument in the country of destination.

To operate the instrument from a power source other than the one set at the factory:

1. Turn the rear power switch to the OFF position and remove the power cord from the instrument.
2. Remove the fuse module by carefully prying it at the top center of the module until you can grasp it and pull it out by hand as shown below.

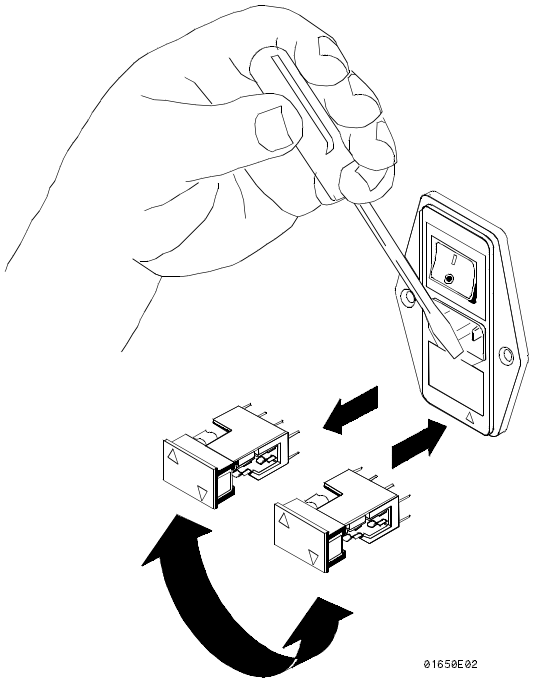


Figure 2-1. Fuse Module Removal

3. Reinsert the fuse module with the arrows aligned for your application. See fuse module below.

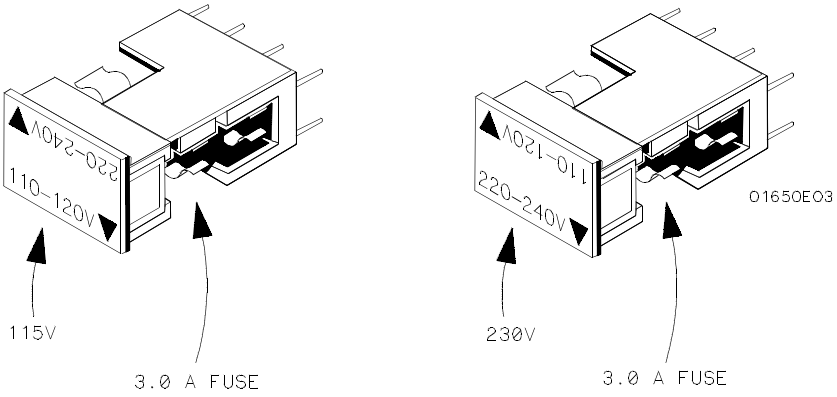


Figure 2-2. Fuse Module

4. Reconnect the power cord, turn the rear power switch to the ON position, and continue normal operation.

Power Cable

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See Table 2-1 for the option numbers of available power cables and plug configurations.

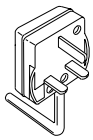
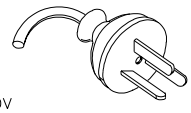
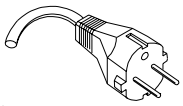
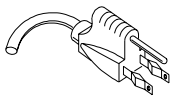
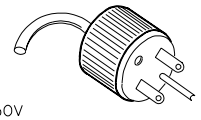
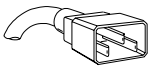
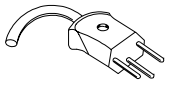
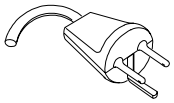
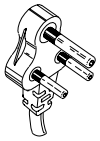
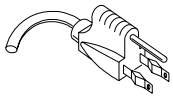
Operating Disk Installation

This instrument is shipped with a yellow protective disk in the disk drive. Before applying power to the instrument, remove the protective disk from the disk drive and install the operating disk. Reinstall the protective disk whenever the instrument is to transported.

Applying Power

When power is applied to the HP 1650B/51B, a power-up self test is automatically performed. For information on the power-up self test, refer to section 3.

Table 2-1. Power Plug Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900  250V	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 901  250V	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia New Zealand
OPT 902  250V	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So. Africa, India (Unpolarized in many nations)
OPT 903**  125V	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Phillipines, Taiwan
OPT 904**  250V	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 905  250V	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 906  250V	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 912  220V	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 917  250V	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 918  100V	8120-4753 8120-4754	Straight Miti 90°	90/230 90/230	Dark Gray	Japan

Rev.11NOV88 ART00019

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP part number for complete cable including plug.

**These cords are included in the CSA certification approval of the equipment.

E=Earth Ground
L=Line
N=Neutral

User Interface

The front-panel user interface of the HP 1650B/51B consists of front-panel keys, the KNOB, and display. The interface allows configuration of each analyzer (machine) within the logic analyzer. It also displays acquired data and measurement results.

Use the front-panel interface with the following process:

- select the desired menu with menu keys
- place the cursor on the desired field within the menu by rotating the KNOB
- display the field options or current data by pressing the SELECT key
- select the desired option by rotating the KNOB or entering new data by using the KNOB or the keypad
- Start and stop data acquisition by using the RUN and STOP keys

HP-IB Interfacing

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programming Instrumentation." HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. The interface makes it possible to transfer messages between two or more HP-IB compatible devices. HP-IB is a parallel bus of 16 active signal lines divided into three functional groups according to function.

Eight signal lines, called data lines, are in the first functional group. The data lines are used to transmit data in coded messages. These messages are used to program the instrument function, transfer measurement data, and coordinate instrument operation. Input and output of all messages, in bit parallel-byte serial form, are also transferred on the data lines. A 7-bit ASCII code normally represents each piece of data.

Data is transferred by means of an interlocking "Handshake" technique which permits data transfer (asynchronously) at the rate of the slowest active device used in that transfer. The data byte control lines coordinate the handshaking and form the second functional group.

The remaining five general interface management lines (third functional group) are used to manage the devices connected to the HP-IB. This includes activating all connected devices at once, clearing the interface, and other operations.

The HP-IB connector and on the rear panel are shown in figure 2-3.

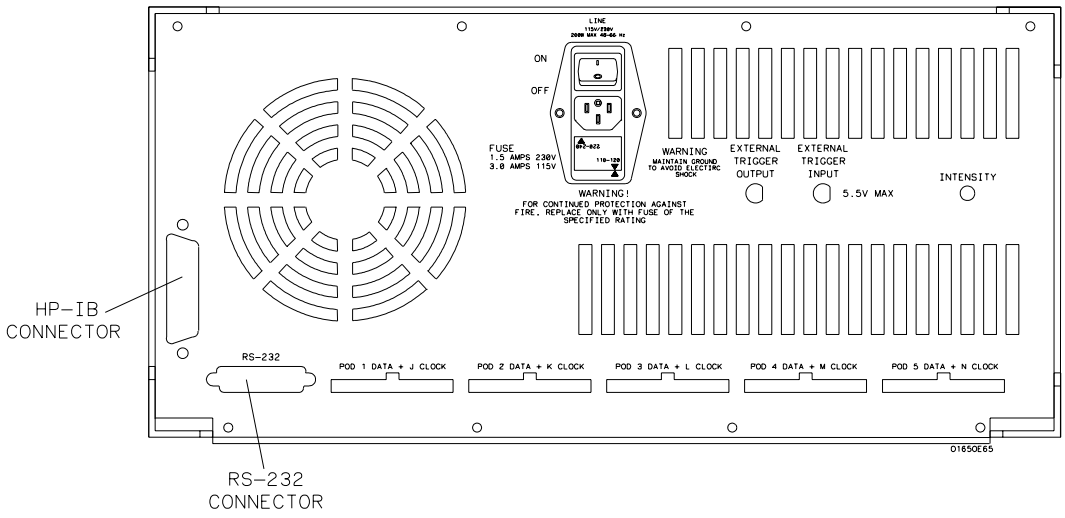


Figure 2-3. HP 1650B Rear Panel

HP-IB Address Selection

Each instrument connected to the HP-IB interface bus requires a unique address. The address provides a method for the system computer to select individual instruments on the bus. The address of the HP 1650B/51B defaults at power up to decimal "07". The corresponding ASCII code is a listen of "" and a talk address of "G." To change the address of the HP 1650B/51B proceed as follows:

1. Press the I/O key on the front-panel keypad and the I/O menu will appear on screen.
2. Rotate the KNOB until "I/O Port Configuration" is highlighted.
3. Press the SELECT key and the External I/O Port Configuration menu will appear on screen.

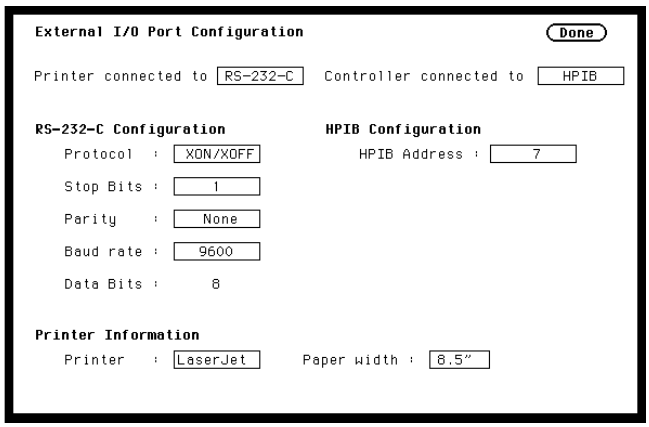


Figure 2-4. External I/O Port Configuration Menu

4. Select the HP-IB Address field with the KNOB and press the SELECT key.
5. When the pop-up field appears on screen, rotate the KNOB to select the desired HP-IB address.
6. Press the SELECT key to enter the new address.
7. Select the DONE field in the upper-right corner with the KNOB to exit the External I/O Port Configuration menu.

RS-232-C Interface

The HP 1650B/51B interfaces with RS-232-C communication lines through a standard 25 pin D connector. The HP 1650B/51B is compatible with RS-232-C protocol. When a hardwire handshake method is used, the Data Terminal Ready (DTR) line (pin 20 on the Computer/Modem connector) is used to signal whether space is available in the logical I/O buffer for more data. Pin outs of the RS-232-C connectors are listed in table 2-4.

Table 2-1. RS-232-C Signal Definitions

Pin No.	RS-232-C Function	Standard	Signal Direction and Level
1	Protective Ground	AA	Not applicable
2	Transmitted Data (TD)	BA	Data from Logic Analyzer High = Space = "0" = + 12 V Low = Mark = "1" = -12 V
3	Received Data (RD)	BB	Data to Logic Analyzer High = Space = "0" = + 3 V to + 25 V Low = Mark = "1" = -3 V to -25 V
4	Request to Send (RTS)	CA	Signal from Logic Analyzer High = ON = + 12 V Low = OFF = -12 V
5	Clear to Send (CTS)	CB	Signal to Logic Analyzer High = ON = + 3 V to + 12 V Low = OFF = -3 V to -25 V
6	Data Set Ready (DSR)	CC	Signal to Logic Analyzer High = ON = + 3 V to + 25 V Low = OFF = -3 V to -25 V
7	Signal Ground	AB	Not applicable
8	Data Carrier Detect (DCD)	CF	Signal to Logic Analyzer High = ON = + 3 V to + 25 V Low = OFF = -3 V to -25 V
20	Data Terminal Ready (DTR)	CD	Signal from Logic Analyzer High = ON = + 12 V Low = OFF = -12 V
23	Data Signal Rate Selector	CH/CI	Signal from Logic Analyer Always High = ON = + 12 V

RS-232-C Configuration

At power up, the RS-232-C interface is configured as shown in previous figure. To change the RS-232-C configuration:

1. Press the I/O key on the front-panel keypad and the I/O menu will appear on screen.
2. Rotate the KNOB until "I/O Port Configuration" is highlighted.
3. Touch the SELECT key and the External I/O Port Configuration menu will appear on screen.

4. Using the KNOB and SELECT key, configure the RS-232-C interface as desired.

5. Select the DONE field in the upper-right corner with the KNOB to exit the External I/O Port Configuration menu.

Operating Environment

The operating environment for the HP 1650B/51B is described in table 1-2. Note the non-condensing humidity limitation. Condensation within the instrument cabinet can cause poor operation or malfunction. Protection should be provided against temperature extremes which cause condensation within the instrument.

The HP 1650B/51B operates at all specifications within the temperature and humidity range given in table 1-2.

Storage and Shipment

The instrument may be stored or shipped in environments within the following limits:

Temperature:-40 degrees C to + 75 degrees C.

Humidity:Up to 90% at 65 degrees C.

Altitude:Up to 15,300 metres (50,000 feet).

Tagging for Service

If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag to the instrument identifying the owner, address of the owner, complete instrument model and serial numbers, and a description of the service required.

Original Packaging

If the original packaging material is unavailable or unserviceable, materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-packard office for service, attach a tag identifying the owner, address of the owner, complete instrument model and serial numbers, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Other Packaging

The following general instructions should be followed for repacking the instrument with commercially available materials.

- Remove discs from disk drives and install yellow shipping discs.
- Wrap the instrument in heavy paper or plastic.
- Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.
- Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard.
- Seal the shipping container securely.
- Mark the shipping container FRAGILE to ensure careful handling.
- In any correspondence, refer to the instrument by model number and serial number.

Cleaning Requirements

Use MILD SOAP AND WATER to clean the HP 1650B/51B cabinet and front panel. Care must be taken to not use a harsh soap which may damage the water-base paint finish of the instrument.

Contents

Section 3 Performance Tests

3

Performance Tests

Introduction

These procedures test the electrical performance of the logic analyzer by using the specifications in table 1-1 as the performance standards. All tests may be performed without access to the interior of the instrument.

Recommended Test Equipment

Equipment required for the performance tests in this section is listed in the Recommended Test Equipment table in Section 1. Any equipment that satisfies the critical specification listed in the table may be substituted for the recommended model.

Test Connector

The performance tests and adjustments require connecting pulse generator outputs to probe pod inputs. Figure 3-1 is a test connector that may be built to allow testing of multiple channels (up to eight at one time). The test connector consists of a BNC connector and a length of wire. Connecting more than eight channels to the test connector at a time will induce loading of the circuit and true signal representation will degrade. Test results may not be accurate if more than eight channels are connected to the test connector.

The Hewlett-Packard part number for the BNC connector in figure below is 1250-1032. An equivalent part may be used in place of the Hewlett-Packard part.

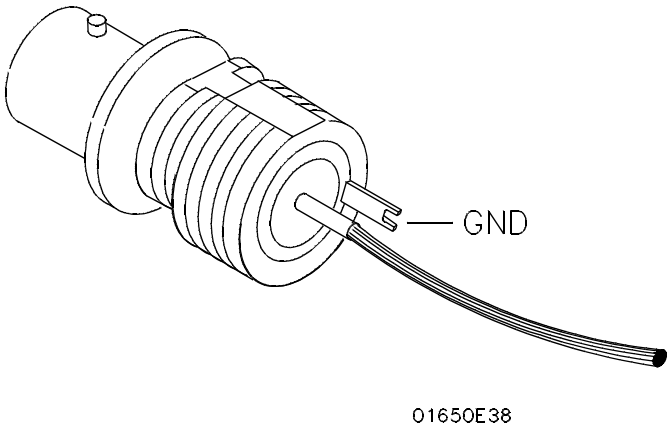


Figure 3-1. Test Connector

Test Record

The results of the performance tests may be tabulated on the Test Record provided at the end of this section. The Test Record lists the performance tests and provides an area to mark whether the pod passed or failed the test. The results recorded in the table at incoming inspection may be used for later comparisons of the tests during periodic maintenance, troubleshooting, and after repairs or adjustments.

Self Tests

The power-up self test is automatically performed upon applying power to the logic analyzer. Since the performance tests require test equipment, self tests may be performed individually to provide a higher level of confidence that the instrument is operating properly. A message that the instrument has failed the test will appear if any problem is encountered during the test. The individual self tests may be performed for functions listed in the self test menu which is invoked via the I/O menu. The HP 1650B/51B self test is located on the operating system disk and is required to run the tests.

Power-up Self Test

The power-up self test is automatically invoked at power-up of the HP 1650B/51B Logic Analyzer. The revision number of the operating system firmware is given in the upper right of the screen during the power-up self test. As each test completes, either passed or failed is printed in front of the name of the test in the following manner:

PERFORMING POWER-UP SELF TESTS

passed ROM test

passed RAM test

passed Interrupt test

passed Display test

passed Keyboard test

passed Acquisition test

passed Threshold test

passed Disk test

LOADING SYSTEM FILE

As indicated by the last message, the HP 1650B/51B automatically loads the operating system disk in the disk drive. If the operating system disk is not in the disk drive, the message SYSTEM DISC NOT FOUND is displayed at the bottom of the screen and NO DISK is displayed in front of disk test in place of "passed".

If the above message appears, turn off the instrument, insert the operating system disk into the disk drive, and again apply power.

Selectable Self Tests

Seven self tests may be invoked individually via the Self Test menu. The seven selectable self tests are:

- Data Acquisition
- RS-232-C
- External Trigger BNCs
- Keyboard
- RAM
- ROM
- Disk Drive
- Cycle through all tests

The required test is selected by moving the cursor to the test and pressing the front panel SELECT key. A pop-up menu appears with a description of the test to be performed. The self test does not begin until the cursor is placed on **Execute** and the front panel SELECT key is pressed.

After the test has been completed, either **Passed**, **Failed**, or **Tested** is displayed on the Self Test menu in front of the test. These tests are used as troubleshooting aids. Section 6 contains information on the individual tests used for troubleshooting.

Performance Test Interval

The calibration cycle for the logic analyzer is two years, therefore, periodic performance verification of the HP 1650B/51B is recommended at two year intervals. The instrument's performance should be verified after it has been serviced, or if improper operation is suspected. Calibration should be performed before any performance verification tests. Further checks requiring access to the interior of the instrument are included in the adjustment section, but are not required for the performance verification.

Test Record

The results of the performance tests may be tabulated on the Test Record provided at the end of this section. The Test Record lists the performance tests and provides an area to mark whether the pod passed or failed the test. The results recorded in the table at incoming inspection may be used for later comparisons of the tests during periodic maintenance, troubleshooting, and after repairs or adjustments.

Clock, Qualifier, and Data Inputs Test 1

Description: This test verifies maximum clock rate with counting mode for the HP 1650B/51B. This test also verifies the setup and hold times for the falling edge of the HP 1650B L clock specification, and the falling edge of the HP 1651B J and K clock specification.

Specification: Clock repetition rate: with time or state counting mode on, minimum time between states is 60 ns.

Setup time: Data must be present prior to clock transition; ≥ 10 ns.

HP 1650B hold time: Data must be present after falling edge of L clock transition; 0 ns.

HP 1651B hold time: Data must be present after falling edge of J and K clock transition; 0 ns.

Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscilloscope ................................... HP 54502A
50 Ohm Feedthru (2) ............................ HP 10100C
Test Connector  see figure 3-1....................... (2)
```

Procedure:

1. Connect the HP 1650B\ 51B and test equipment as in figure 3-2.

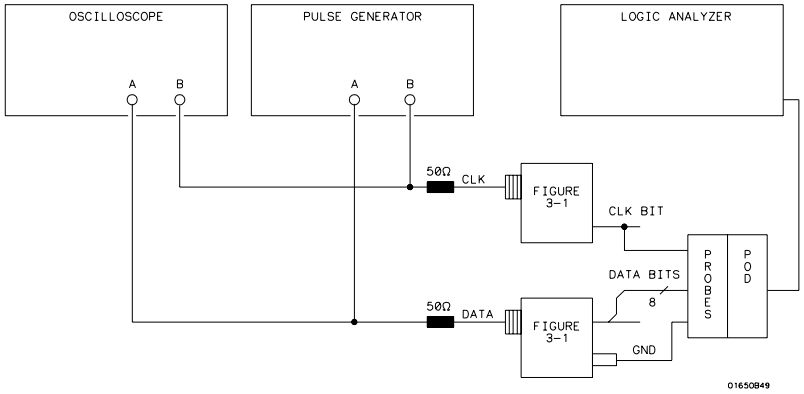


Figure 3-2. Setup for Data Test 1

Note In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be connected to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-3.

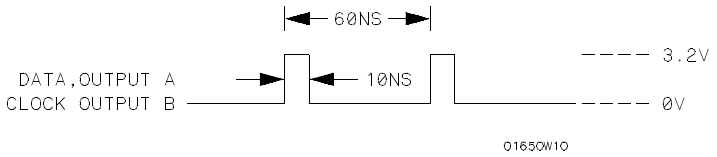


Figure 3-3. Waveform for Data Test 1

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	60 ns	---
Width (WID)	10 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	0 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in 3-4. Refer to steps a through c if unfamiliar with menu.

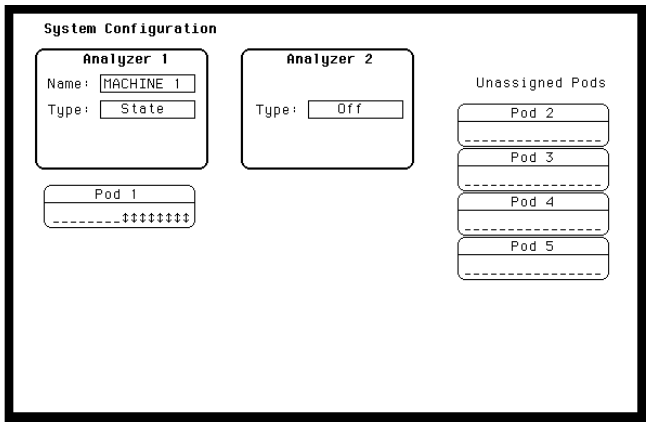


Figure 3-4. System Configuration for Data Test 1

a. Move cursor to **Type** field of **Analyzer 1** and SELECT.

b. Set the analyzer **Type** to **State** using cursor and SELECT.

c. Move cursor to **Pod** to be tested and assign to **Machine 1**.

4. In the **State Format Specification** assign **Clock Period > 60 ns**. Also assign lower 8 channels of the pod under test to a label as shown in next figure . If testing HP 1650B then assign falling edge of L clock for all pods. If testing HP 1651B then assign falling edge of J clock for all pods. Refer to steps a through c if unfamiliar with the menus.

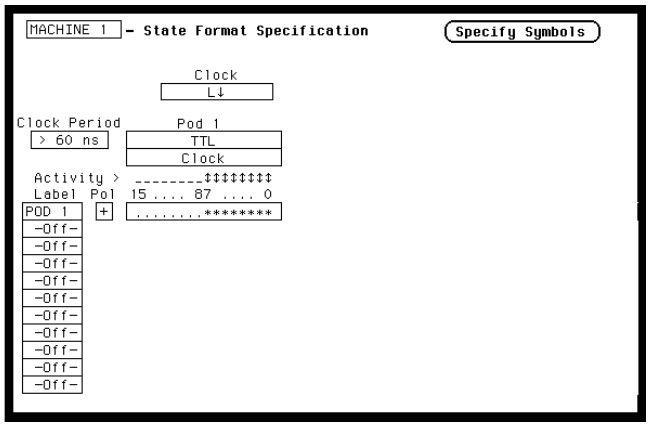


Figure 3-5. State Format Specification for Data Test 1

a. Press front-panel FORMAT key.

b. Move cursor to **Clock** field of menu. Use cursor and SELECT key to set appropriate clock for falling edge as in next figure.

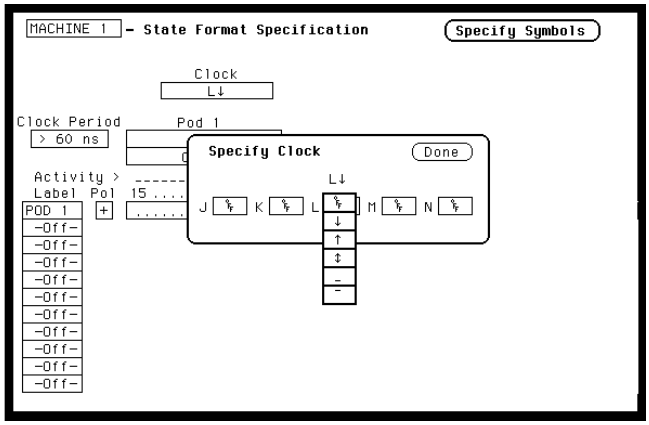


Figure 3-6. Clock Assignment for Data Test 1

c. Move cursor to the bit assignment field and turn on appropriate eight bits to be tested (* = on; . = off) as in figure below.

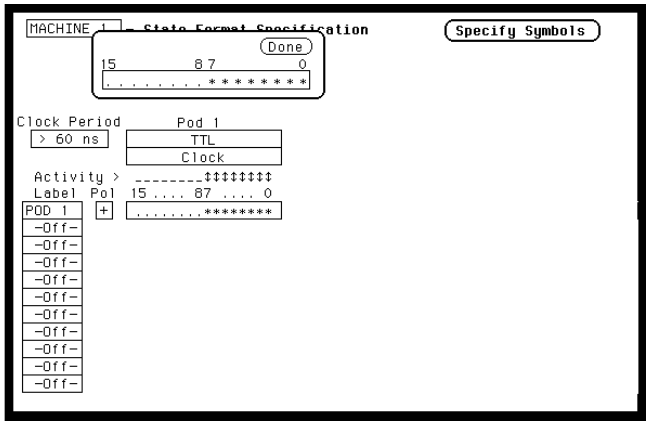


Figure 3-7. Bit Assignment for Data Test 1

5. Set up the **State Trace Specification** without sequencing levels and set **Count States** as in next figure.

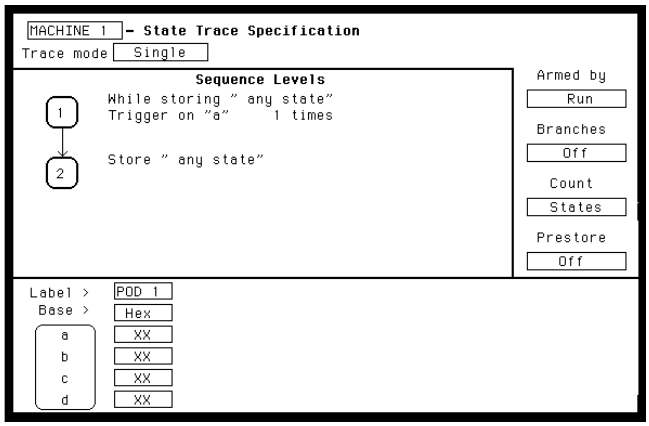


Figure 3-8. Trace Specification for Data Test 1

a. Press front-panel TRACE key.

b. Move cursor to **Coun**t, press SELECT, then move cursor to **States**, press SELECT, and set to **any state** by pressing SELECT again.

6. Press RUN. The **State Listing** is displayed and shows Fs for the channels under test, when test is passed, as in figure 3-9.

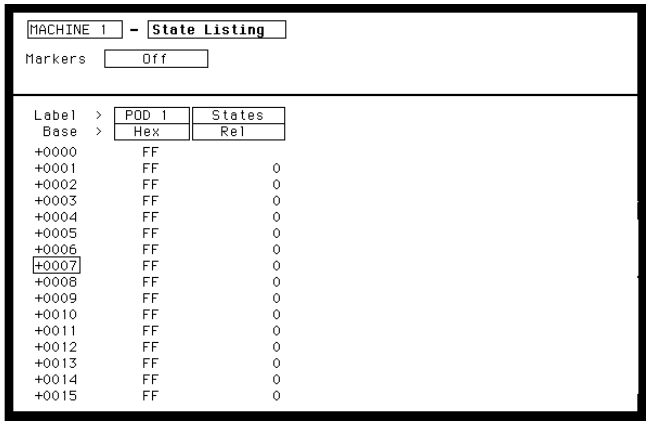


Figure 3-9. State Listing for Data Test 1

Note To ensure consistent pattern of Fs in listing, use front-panel ROLL field and knob to scroll through **State Listing**.

7. If testing the HP 1651B, connect the K clock of Pod 2 to the test connector and repeat steps 4 and 6 for the falling edge of K clock.
8. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector. If testing the HP 1651B then re-assign the falling edge of J clock.
9. Repeat steps 3, 4, 6 and 7 until all pods have been tested.
10. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector.
11. Repeat steps 3, 4, 6, 7 and 8 until the upper bits of all pods have been tested.

Clock, Qualifier, and Data Inputs Test 2

Description: This test verifies the setup and hold time specification for the rising edge transition of all clocks on the HP 1650B/51B.

Specification:

Setup time: Data must be present prior to clock transition; ≥ 10 ns.

Hold time: Data must be present after rising clock transition; 0 ns.

Equipment:

```
Pulse Generator ........................... HP 8161A/020
Oscilloscope .............................. HP 54502A
50 Ohm Feedthru (2) ....................... HP 10100C
Test Connectors  (2).....................see figure 3-1
```

Procedure:

1. Connect the HP 1650B\ 51B and test equipment as in figure 3-10.

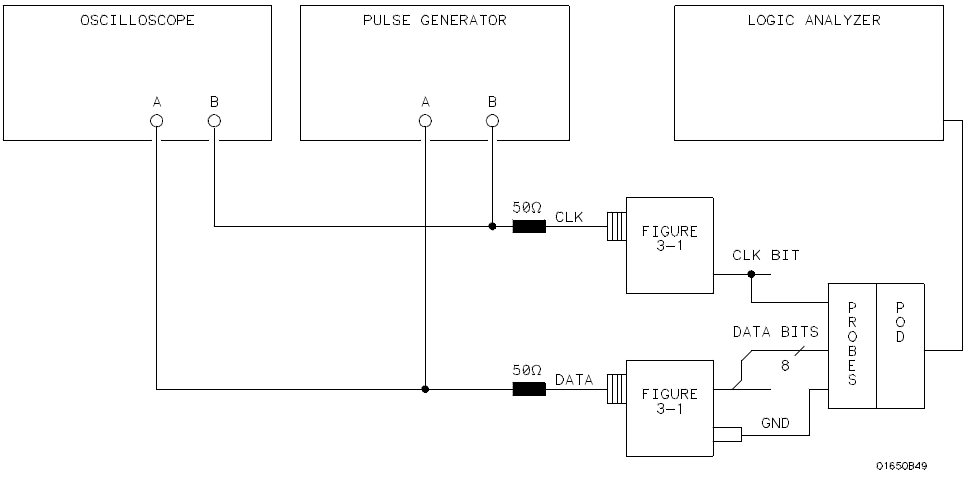


Figure 3-10. Test Setup for Data Test 2

Note

In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be connected to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-11. Pulse generator settings

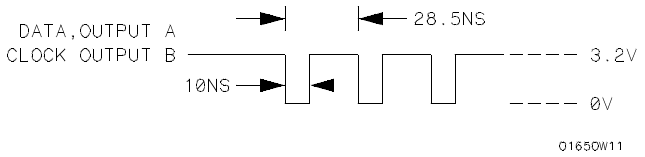


Figure 3-11. Waveform for Data Test 2

are different for HP 1650B and HP 1651B.

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)		
HP 1650B	28.5 ns	---
HP 1651B	40 ns	---
Width (WID)		
HP 1650B	18.5 ns	18.5ns
HP 1651B	30 ns	30 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	0 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in **System Configuration** as in previous test figure 3-4.

4. In the **State Format Specification** assign **Clock Period < 60 n**s, and rising edge of J clock. Also, assign lower 8 channels of the pod under test to a label as in figure 3-12.

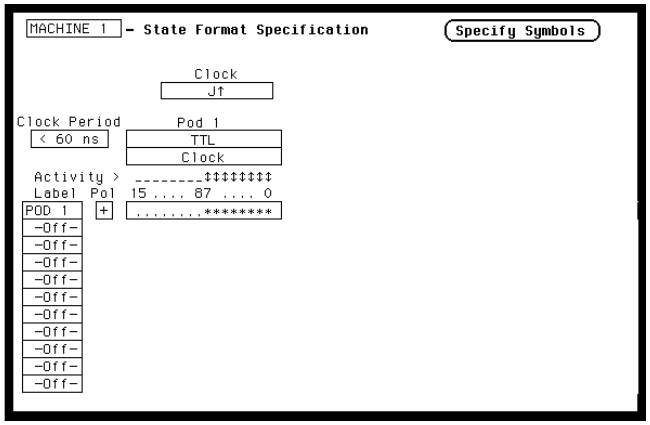


Figure 3-12. State Format Specification for Data Test 2

5. Set the **State Trace Specification** without sequencing levels and set **Count** to **Off** as in Figure 3-13.

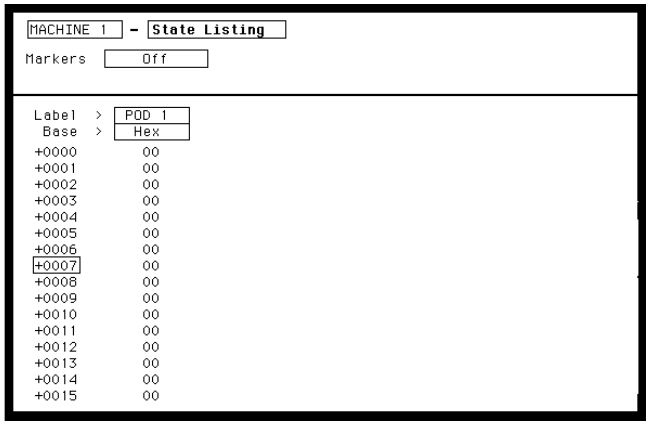


Figure 3-13. State Listing for Data Test 2

6. Press RUN. The **State Listing** is displayed and lists all 0s for the channels under test, if passed test, as in figure 3-14.

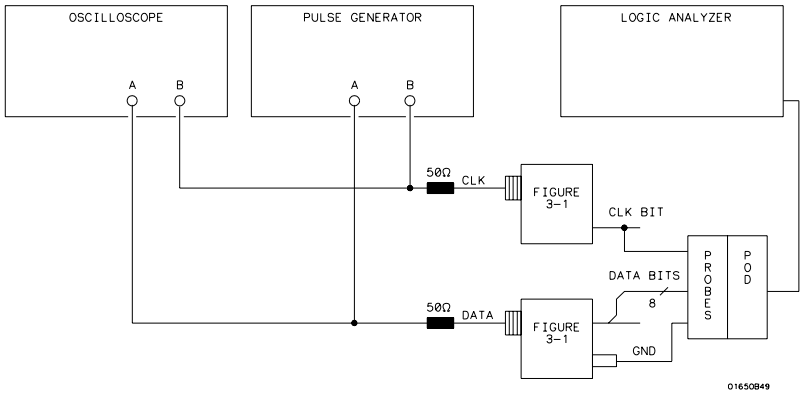


Figure 3-14. Setup for Data Test 3

Note To ensure consistent pattern of 0s in listing, use front-panel ROLL keys and knob to scroll through **State Listing**.

7. Connect the next clock to the test connector and repeat steps 4 and 6 for the appropriate clock. Repeat until all clocks have been tested (clocks J, K, L, M and N).

8. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

9. Repeat steps 3, 4, 6 and 7 until all pods have been tested (pods 1 through 5). Start again with the rising edge of J clock and test the pod with all clocks.

10. Repeat until the lower bits of all pods have been tested (pods 1 through 5).

11. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector. Repeat steps 3, 4, 6, 7, and 8 until the upper bits of all pods have been tested (pods 1 through 5).

Clock, Qualifier, and Data Inputs Test 3 (HP 1650B Only)

Description: This performance test verifies the hold time specification for the falling clock transitions of the J, K, M and N clock on the HP 1650B.
Specification: HP 1650B Hold time: Data must be present after falling J, K, M and N clock transition; 1 ns.
Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscilloscope ................................ HP 54502A
50 ohm Terminators........................... HP 10100C
Test Connectors  see figure 3-1.....................(2)
```

Procedure:

1. Connect the HP 1650B and test equipment as in figure 3-15.

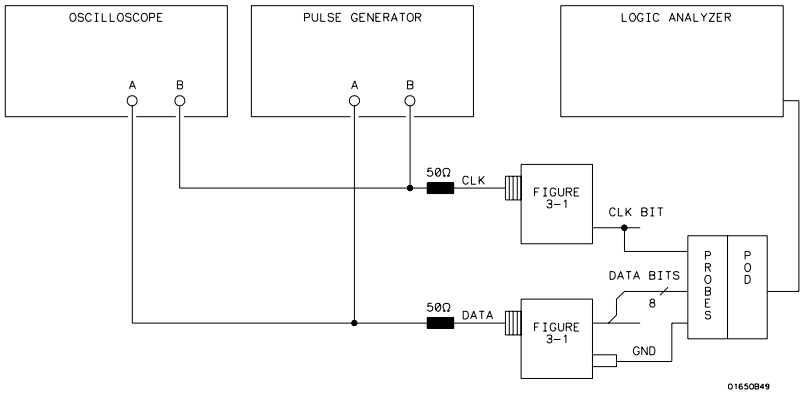


Figure 3-15. Setup for Data Test 3

Note 

In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be connected to ensure accurate test results.

2. Adjust pulse generator for the outputs in figure 3-16.

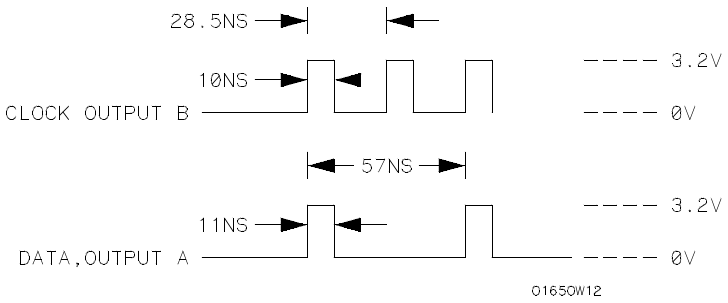


Figure 3-16. Waveform for Data Test 3

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	57 ns	---
Width (WID)	11 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	---
Double Pulse (DBL)	---	28.5 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in previous test figure 3-4.

4. In the **State Format Specification** menu assign **Clock Period < 60 ns**, and falling edge of J clock. Also, assign the lower 8 channels of the pod under test to a label as in figure 3-12.

5. Set the **State Trace Specification** without sequencing levels and set **Count Off** as in previous figure 3-13.

6. Press RUN. The **State Listing** is displayed and lists alternating Fs and 0s as in figure 3-17, if test has passed.

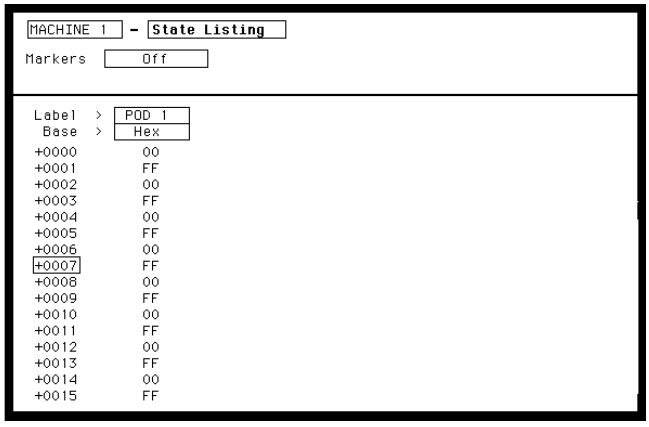


Figure 3-17. State Listing for Data Test 3

Note 

To ensure consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through **State Listing**.

7. Connect the next clock to the test connector and repeat steps 4 and 6 for the appropriate clock. Repeat until the J, K, M and N clocks have been tested.

8. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector. Repeat steps 3, 4, 6 and 7 until all pods have been tested (pods 1 through 5). Start again with the falling edge of the J clock and test the pod with all clocks except L clock.

9. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector. Repeat steps 3, 4, 6, 7 and 8 until the upper bits of all pods have been tested (pods 1 through 5).

Clock, Qualifier, and Data Inputs Test 4

Description: This test verifies the minimum swing voltages of the input probes and the maximum clock rate of the HP 1650B\51B when it is in single phase mode.

Specification:

Minimum swing: 600 mV peak-to-peak.

HP 1650B Clock repetition rate: Single phase is 35 MHz maximum.

HP 1651B Clock repetition rate: Single phase is 25 MHz maximum.

Clock pulse width: ≥ 10 ns at threshold.

Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscilloscope ................................... HP 54502A
50 Ohm Feedthru (2) ............................ HP 10100C
Test Connectors  see figure 3-1.....................(2)
```

Procedure:

1. Connect the HP 1650B\51B and test equipment as in figure 3-18. In order to most accurately measure the amplitude of the test signals from the pulse generator, high impedance scope probes should be used to look at the signal levels at the output of the pulse generator.

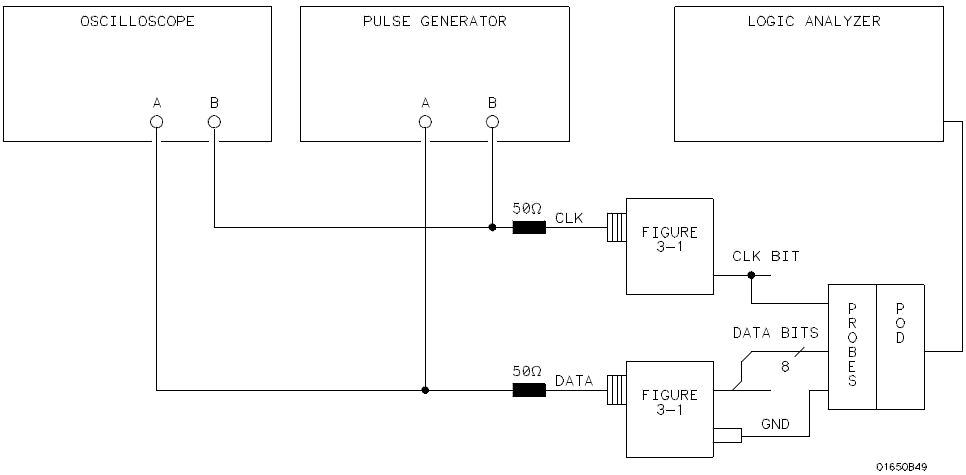


Figure 3-18. Setup for Data Test 4

Note In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be connected to ensure accurate test results. It is recommended that all eight channel grounds be connected.

2. Adjust pulse generator for the output in figure 3-19. Pulse generator settings are different for HP 1650B and HP 1651B.

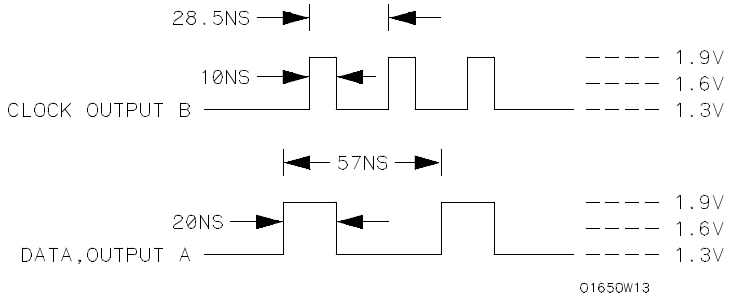


Figure 3-19. Waveform for Data Test 4

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)		
HP 1650B	57 ns	---
HP 1651B	80 ns	---
Width (WID)	20 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	1.9V	1.9V (see Note)
Low Level (LOL)	1.3V	1.3V (see Note)
Delay (DEL)		
HP 1650B	18.5 ns	---
HP 1651B	30 ns	---
Double Pulse (DBL)		
HP 1650B	---	28.5 ns
HP 1651B	---	40 ns
Output Mode	ENABLE	ENABLE

Note The voltage levels of the waveforms must have the correct amplitude at the logic analyzer probe tips. The pulse generator output may have to be increased slightly to compensate for loading by the logic analyzer.

3. Assign the pod under test to **Analyzer 1** in **System Configuration** as in previous figure 3-4.

4. In the **State Format Specification** assign **Clock Period < 60 ns**, and rising edge of J clock. Also, assign lower 8 channels of the pod under test to a label as in previous figure 3-12.

5. Set the **State Trace Specification** without sequencing levels and set **Count Off** as in previous test figure 3-13.

6. Press RUN. The **State Listing** is displayed and shows alternating Fs and 0s for the channels under test as in figure 3-20.

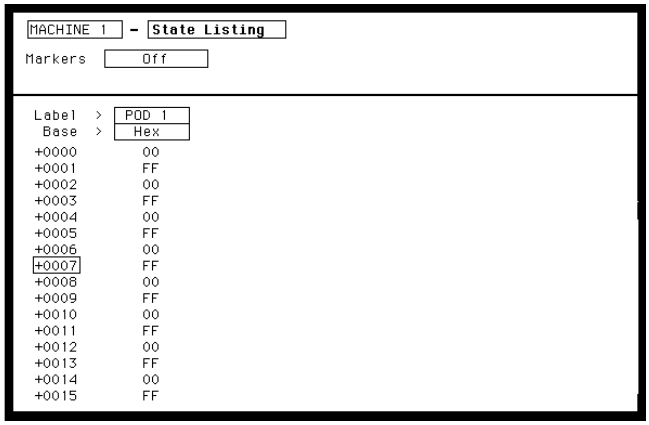


Figure 3-20. State Listing for Data Test 4

Note To ensure consistent pattern of alternating Fs and 0s, use the front-panel ROLL keys and knob to scroll through **State Listing**.

7. Connect the next clock to the test connector and repeat steps 4 and 6. Repeat until all clocks have been tested (clocks J, K, L, M and N).
8. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
9. Repeat steps 3, 4, 6 and 7 until all pods have been tested (pods 1 through 5). Start again with the rising edge of J clock and test the pod with all clocks.
10. Repeat until the lower bits of all pods have been tested (pods 1 through 5).
11. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector.
12. Repeat steps 3, 4, 6, 7 and 8 until the upper bits of all pods have been tested (pods 1 through 5).

Clock, Qualifier, and Data Inputs Test 5

Description: This performance test verifies the maximum clock rate for mixed mode clocking during state operation.

Specification:

Clock repetition rate: HP 1650B single phase is 35 MHz maximum, HP 1651B is 25 MHz. With time or state counting, minimum time between states is 60 ns (16.7 MHz maximum). Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by 50 ns.

Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscilloscope ................................... HP 54502A
50 Ohm Feedthru (2) ............................ HP 10100C
Test Connectors  see figure 3-1.....................(2)
```

Procedure:

1. Connect the HP 1650B/51B and test equipment as in figure 3-21 by connecting channels 0-3 and 8-11 of the pod under test to the test connector. On the slave clock transition the four bits of the lower byte are transferred to the logic analyzer, and on the master clock transition the four bits of the upper byte are transferred to the logic analyzer.

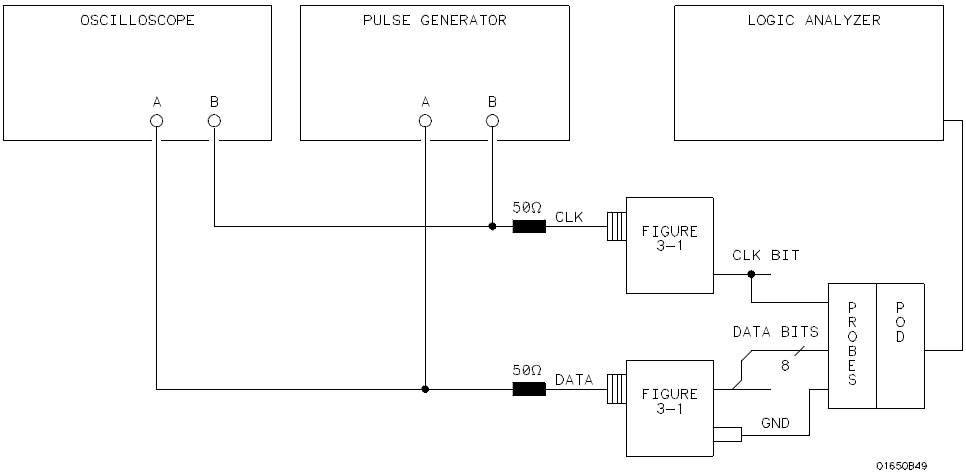


Figure 3-21. Setup for Data Test 5

Note In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be connected to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-22.

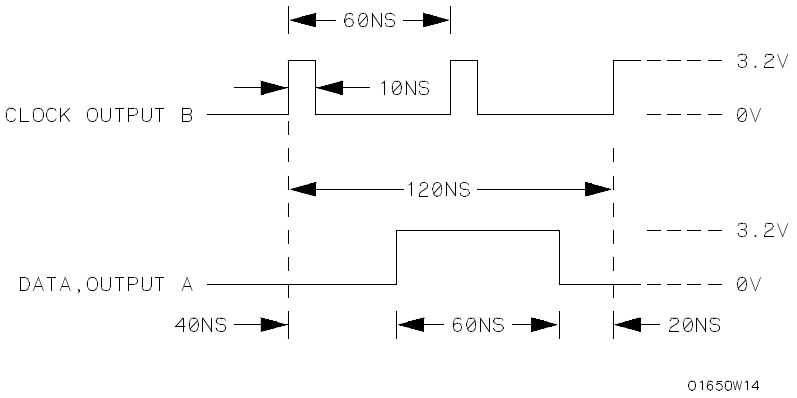


Figure 3-22. Waveform for Data Test 5

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	120 ns	---
Width (WID)	60 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	40 ns	---
Double Pulse (DBL)	---	60 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in previous figure 3-4.

4. Set up the **State Format Specification** as in figure 3-23, assigning the falling J clock to **Master Clock** and the rising J clock to **Slave Clock**. Refer to steps a through d after figure if unfamiliar with the menu.

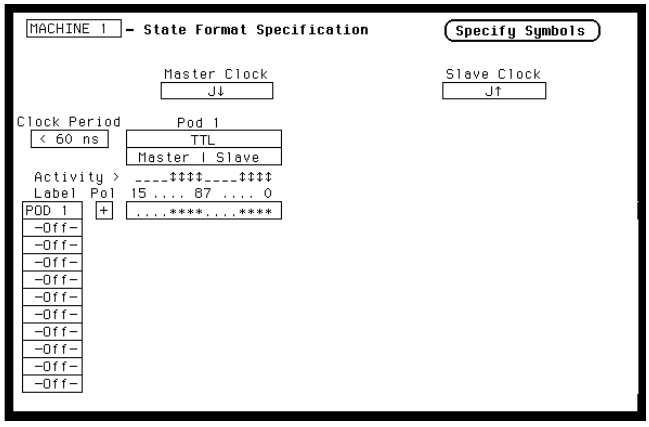


Figure 3-23. State Format Specification for Data Test 5

a. Move cursor to **Clock** field and SELECT, then assign **Mixed Clocks**.

b. Assign falling transition of the J clock to **Master Clock** and rising transition of the J clock to **Slave Clock**.

c. Assign channels 0-3 and 8-11 of the pod under test.

d. Set **Clock Period to > 60 ns.**

5. Set the **State Trace Specification** without sequencing levels and **Count Off** as in previoius figure 3-13.

6. Press RUN. The **State Listing** displays alternating Fs and 0s for the channels under test as in figure 3-24.

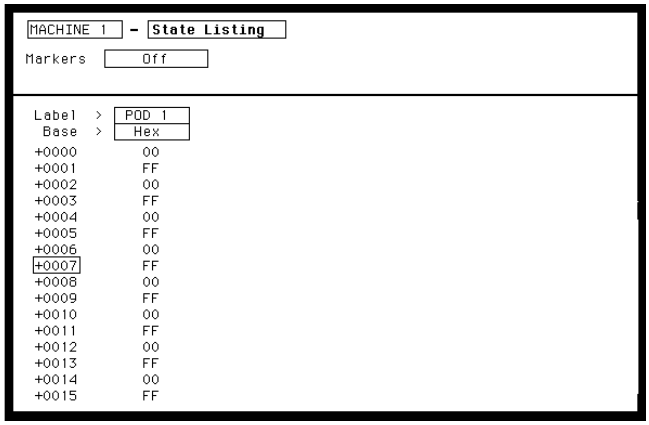


Figure 3-24. State Listing for Data Test 5

Note To ensure consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through **State Listing**.

7. Connect the next clock to the test connector and repeat steps 4 and 6. Repeat until all clocks have been tested (clocks J, K, L, M and N).

8. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

9. Repeat steps 3, 4, 6 and 7 until all pods have been tested (pods 1 through 5). Start again with the falling edge of J clock as the Master and rising edge of the J clock as the Slave clock. Repeat until channels 0 - 3 and 8 - 11 of all pods have been tested (pods 1 - 5).

10. Disconnect bits 0-3 and bits 8-11 from the test connector. Attach bits 4-7 and bits 12-15 to the test connector. Repeat steps 3, 4, 6, 7 and 8 until all pods have been tested (pods 1 through 5).

Clock, Qualifier, and Data Inputs Test 6

Description: This performance test verifies the maximum clock rate for demultiplexed clocking during state operation.

Specification:

Clock repetition rate: HP 1650B single phase 35 MHz maximum, HP 1651B single phase 25 MHz. With time or state counting, minimum time between states is 60 ns (16.7 MHz maximum). Both mixed and demultiplexed clocking use master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede the next slave clock by 50 ns.

Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscillscope..................................... HP 54502A
50 Ohm Feedthru (2) ............................ HP 10100C
Test Connectors  (2).....................see figure 3-1
```

Procedure:

1. Connect the HP 1650B/51B and test equipment as in figure 3-25 by connecting channels 0-7 of the pod under test to the test connector. During demultiplexed clocking only the lower eight bits of each pod are used.

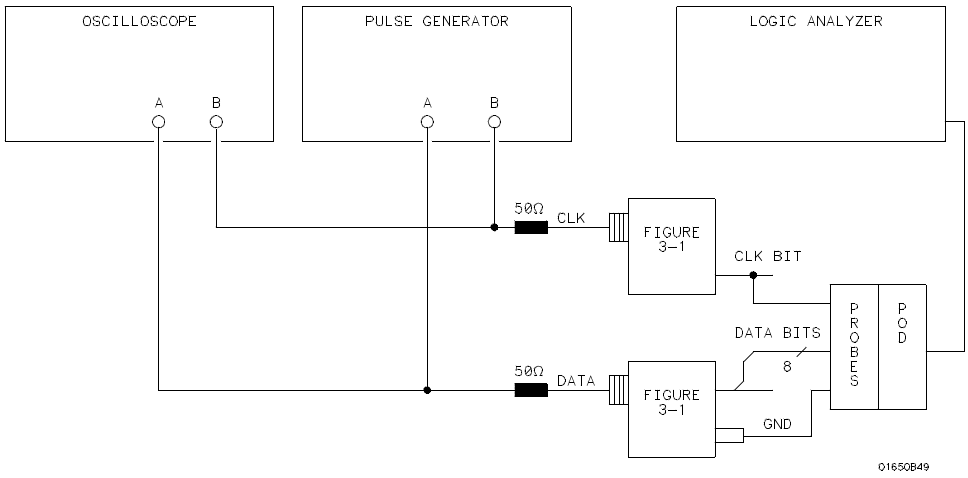


Figure 3-25. Setup for Data Test 6

2. Adjust pulse generator for the output in figure 3-26.

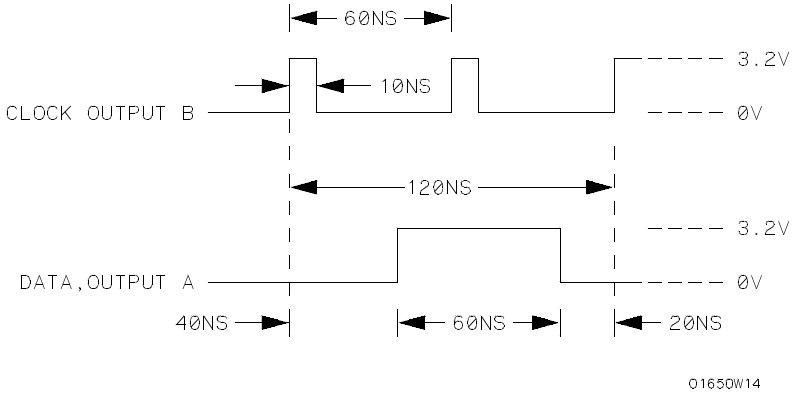


Figure 3-26. Waveform for Data Test 6

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	120 ns	---
Width (WID)	60 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	40 ns	---
Double Pulse (DBL)	---	60 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in **System Configuration** as in previous figure 3-4.

4. Set up **State Format Specification** as in figure 3-27, assigning the falling J clock as **Master Clock** and the rising J clock as **Slave Clock.** Refer to steps a through d after figure if unfamiliar with the menus.

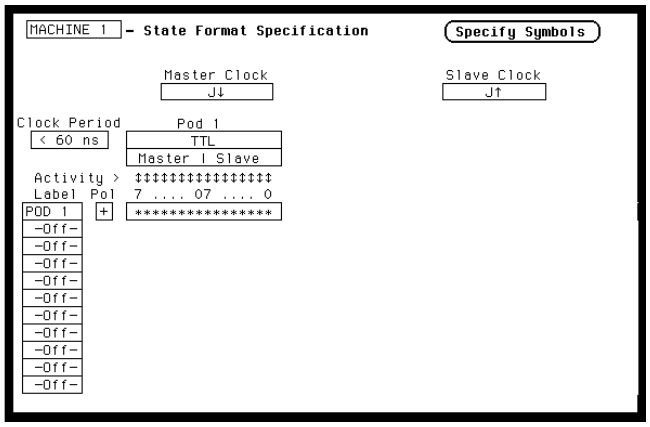


Figure 3-27. State Format Specification for Data Test 6

a. Move cursor to **Clock** field and SELECT, then assign **Demultiplex**.

b. Assign falling clock transition of J clock to **Master Clock** and rising J clock transition to **Slave Clock.**

c. Assign ALL channels to pod under test (only bits 0 through 7 are be available for assignment).

d. Set **Clock Period** to **< 60 ns.**

5. Set **State Trace Specification** without sequencing levels and set **Count Off** as in previous figure 3-13.

6. Press RUN. The **State Listing** shows alternating Fs and 0s for the pod under test as in figure 3-28.

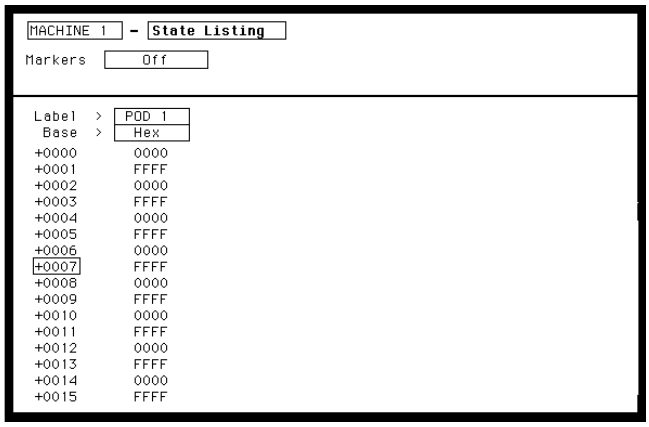


Figure 3-28. State Listing for Data Test 6

Note To ensure consistent pattern of alternating Fs and 0s in listing, use front-panel ROLL field and knob to scroll through **State Listing.**

7. Connect the next clock to the test connector and repeat steps 4 and 6.

8. Repeat until all clocks have been tested (clocks J, K, L, M and N).

9. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

10. Repeat steps 3, 4, 6 and 7 until all pods have been tested (pods 1 through 5). Start again with the falling edge of J clock as the **Master Clock** and rising edge of the J clock as the **Slave Clock**.

Glitch Test

Description:

This performance test verifies the glitch detection specification of the HP 1650B/51B.

Specification:

Minimum detectable glitch: 5 ns wide at the threshold.

Equipment:

```
Pulse Generator ............................. HP 8161A/020
Oscilloscope..................................... HP 54502A
50 ohm Feedthrough.(1)........................... HP 10100C
Test Connector (1) .........................see figure 3-1
```

Procedure:

1. Connect the test equipment as in figure 3-29. The clock inputs are not used for the glitch test since glitch detection is part of timing analysis. Use the oscilloscope to make sure pulses are 5 ns wide at the threshold (1.6 V).

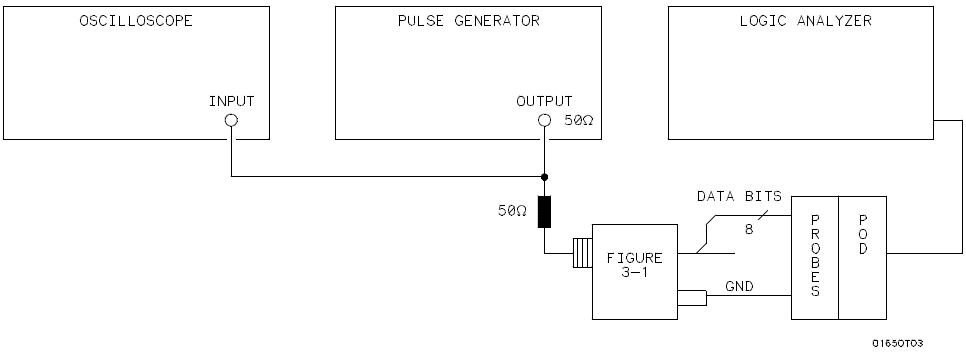


Figure 3-29. Setup for Glitch Test

Note In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be grounded to ensure accurate test results.

2. Adjust pulse generator for the output in figure 3-30.

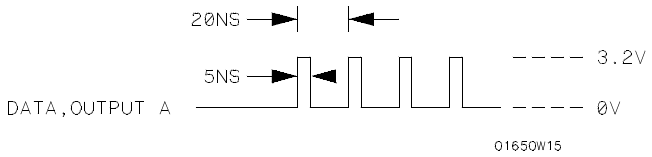


Figure 3-30. Waveform for Glitch Test

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	20 ns	---
Width (WID)	5 ns	---
Leading Edge (LEE)	1 ns	---
Trailing Edge (TRE)	1 ns	---
High Level (HIL)	3.2 V	---
Low Level (LOL)	0 V	---
Delay (DEL)	0 ns	---
Output Mode	ENABLE	---

3. Assign the pod under test to **Analyzer 1** in **System Configuration** as in figure 3-31. Refer to steps a and b if unfamiliar with menus.

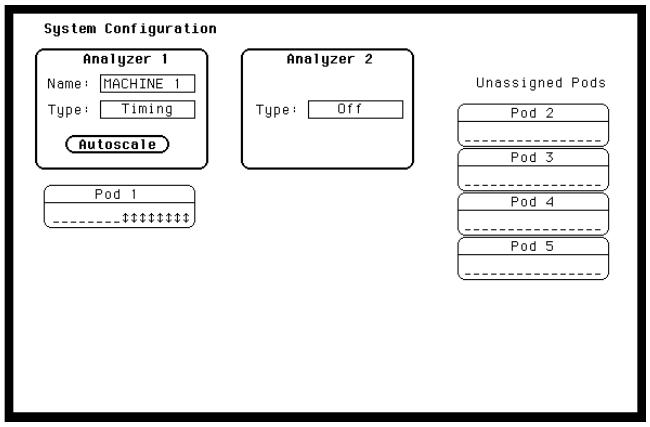


Figure 3-31. System Configuration for Glitch Test

a. Move cursor to **Type** field of **Analyzer 1** and SELECT.

b. Set the analyzer **Type** to **Timing** using cursor and SELECT.

c. Move cursor to pod to be tested and assign to **Machine 1.**

4. In **State Format Specification** assign the lower eight bits of the pod under test to a label as shown in figure 3-32. Make sure the appropriate eight bits in the bit assignment field are turned on.

5. Set **Timing Trace Specification** as in figure 3-33. Follow steps a through c if

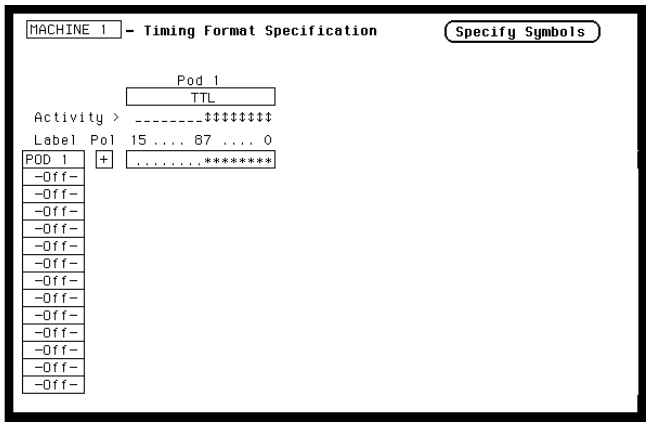


Figure 3-32. Glitch Test Timing Format Specification

unfamiliar with menu.

a. Move cursor to **Acquisition mode** field and SELECT **Glitch.**

b. Move cursor to **Find Pattern** field and SELECT. Push DON'T CARE (all Xs) snd SELECT. Set **Present for** field to **> 30 ns**.

c. Set **Then find Glitch** on all channels (all ***** s).

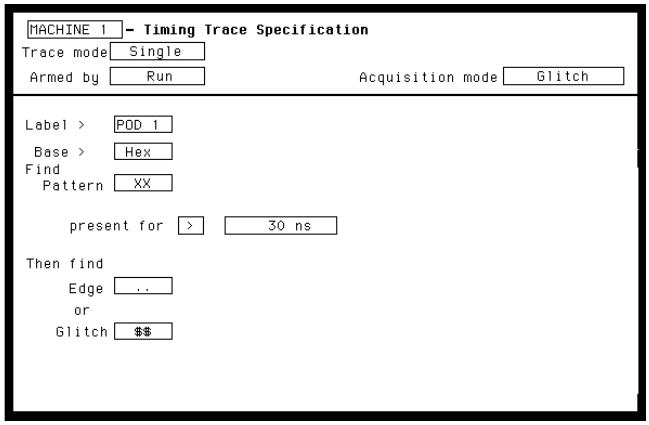


Figure 3-33. Glitch Test Timing Trace Specification

6. Press RUN. The timing analyzer acquires data and shows glitches for channels under test as in figure 3-34. SELECT **Delay** field and rotate knob to assure consistent glitch detection.

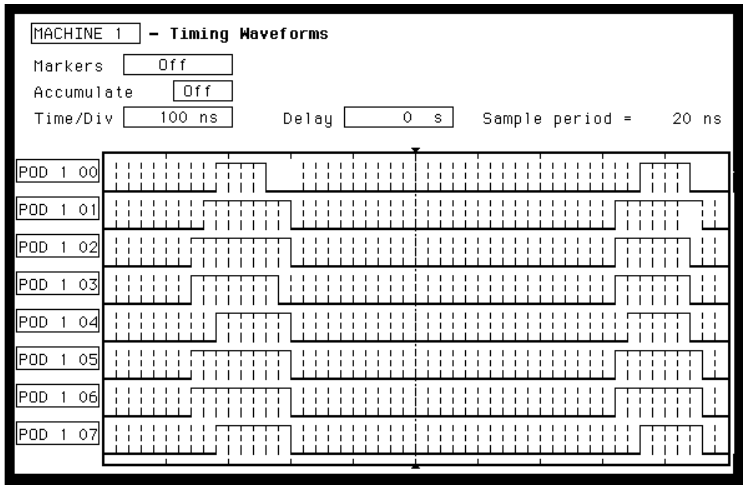


Figure 3-34. Glitch Test Timing Waveforms

Note If sample clock and data synchronize, glitches may be displayed on the timing screen as valid data transitions.

7. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
8. Repeat steps 3, 4, and 6 until all pods have been tested (pods 1 through 5). Make sure to assign correct pod to be tested in **System Configuration.**
9. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector.
10. Repeat steps 3, 4, 6 and 7 until the upper bits of all pods have been tested (pods 1 through 5).

Threshold Accuracy Test

Description: This performance test verifies the threshold accuracy within the three ranges stated in the specification.

Specification:

Threshold accuracy: 150 mV accuracy over the range -2.0 to + 2.0 volts; 300 mV accuracy over the ranges -9.9 to -2.1 volts and + 2.1 to + 9.9 volts.

Equipment:

```
Power Supply ..................................... HP 6216B
Test Connector (1)........................ see figure 3-1
```

Procedure:

1. Connect the test equipment as in figure 3-35.

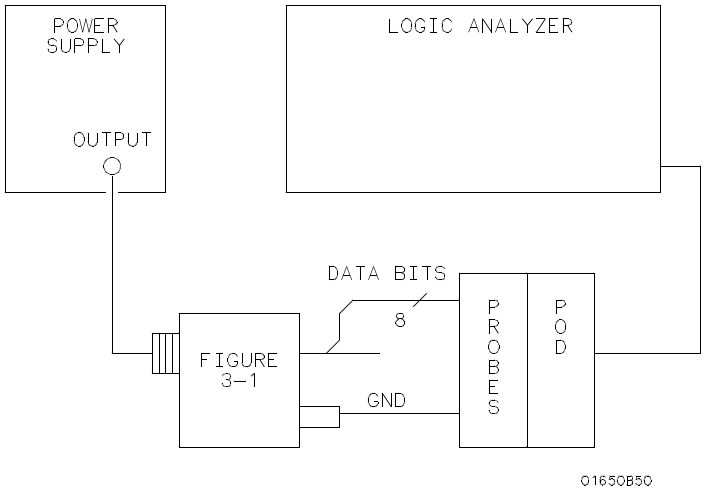


Figure 3-35. Threshold Accuracy Test Setup

Note

In this setup, only eight channels are tested at a time to minimize loading. Ground lead must be grounded to ensure accurate test results.

2. Assign the pod under test to **Analyzer 1** in **System Configuration** as in previous figure 3-31.
3. Configure **Timing Format Specification** for **User Define**d pod threshold of **0.0 V** for the pod under test and assign the lower eight bits in the bit assignment field as in figure 3-36. Refer to steps a and b if unfamiliar with menu.
    a. Move cursor to Pod Threshold field and SELECT. Move cursor to User-defined field and SELECT. Enter the appropriate voltage threshold.

b. Move cursor to bit assignment field and turn on the appropriate eight bits to be tested (* = on; . = off).

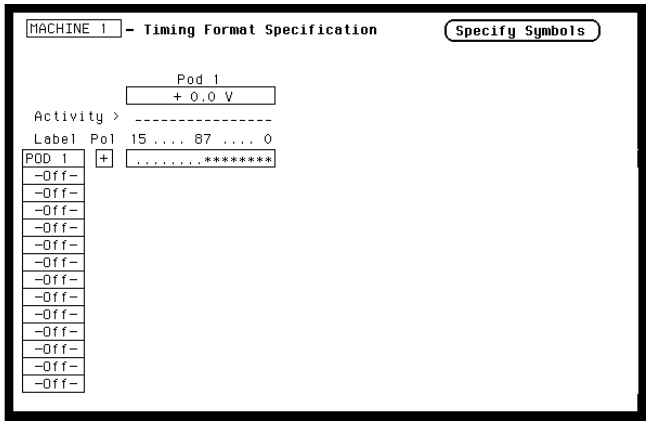


Figure 3-36. Threshold Accuracy Format Specification

4. Set **Timing Trace Specification** as in figure 3-37. Follow steps a through c if unfamiliar with menus.

   a. Move cursor to **Acquisition mode** and SELECT **Glitch**.

   b. Move cursor to **Find Pattern** and SELECT. Push DON'T CARE (all X s) and SELECT. Set **present for** field to **> 30 ns**.

   c. Set **Then find Glitch** to all DON'T CARES (all • s).

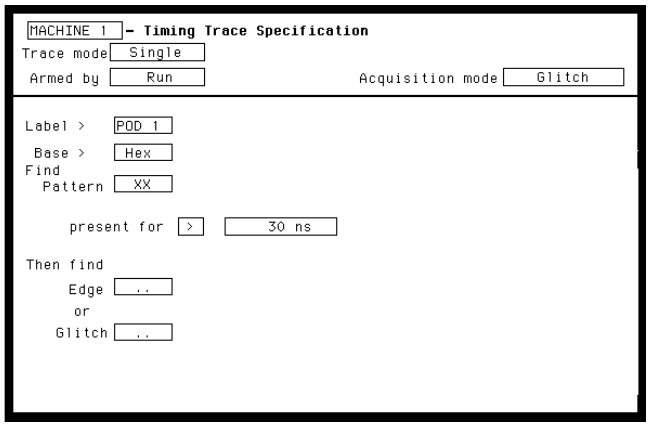


Figure 3-37. Threshold Accuracy Trace Specification

5. Adjust the power supply output for + 150 mV.

6. Press RUN. Data displayed on **Timing Waveforms** is be high for the pod and channels under test as in figure 3-38.

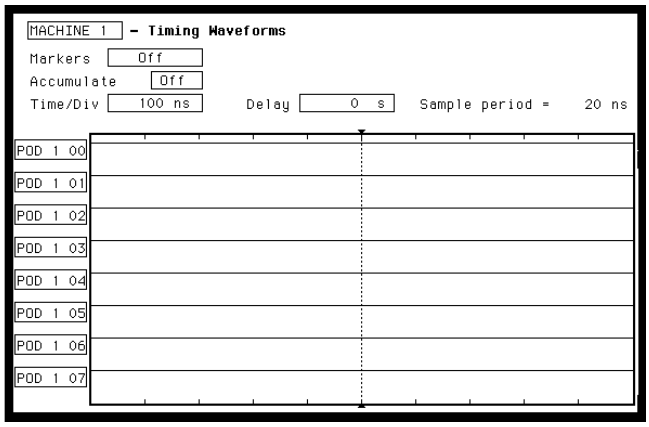


Figure 3-38. Threshold Accuracy Timing Waveforms 1

7. Adjust power supply output for -150 mV.

8. Press RUN. Data displayed on **Timing Waveforms** is all low for the channels under test as in figure 3-39.

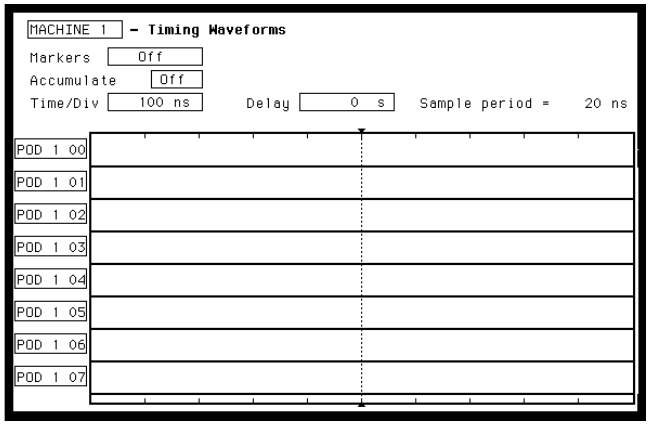


Figure 3-39. Threshold Accuracy Timing Waveforms 2

9. Return to **Timing Format Specification** and change **User Defined Pod Threshold** to **+ 9.9 V**.

10. Adjust power supply for output of + 10.2 V.

11. Press RUN. Data displayed on **Timing Waveforms** all high for the pod and channels under test as in previous test figure 3-37.

12. Adjust power supply for output of + 9.6 V.

13. Press RUN. Data displayed on **Timing Waveforms** is all low for the pod and channels under test as in previous test figure 3-40.

14. Return to the **Timing Format Specification** and change the **User Defined** pod threshold to **-9.9 V**.

15. Adjust power supply for output of -9.6 V.

16. Press RUN. Data displayed on **Timing Waveform**s is all high for the pod and channels under test as in previous test figure 3-39.

17. Adjust power supply for output of **-10.2 V**.

18. Press RUN. Data displayed on **Timing Waveforms** is all low for the pod and channels under test as in previous test figure 3-40.

19. Remove the probe tip assembly from the logic analyzer probe cable and attach to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

20. Repeat steps 2 through 18 until all pods have been tested (pods 1 through 5).

21. Disconnect lower eight bits (bits 0 through 7) from test connector. Attach upper eight bits (bits 8 through 15) to the test connector.

22. Repeat steps 2 through 19 until the upper bits of all pods have been tested (pods 1 through 5).

Table 3-1. Performance Test Record

Hewlett-Packard
Model 1650B/51B
Logic Analyzer

Serial
Number
_____

Tested by
_____

Work Order No.
_____

Date Tested
_____

Recommended Calibration
Interval 24 Months

Test		Results	
Clock, Qualifier, and Data Inputs Test 1		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 2		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 3		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 4		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 5		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____

Table 3-1. Performance Test Record (continued)

Test	Results		
Clock, Qualifier, and Data Inputs Test 6		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Glitch Test		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Threshold Accuracy Test		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____

Contents

Section 4

Adjustments

Adjustments 4

Introduction

This section provides adjustment procedures for the HP 1650B/51B. The assemblies with adjustments are: the power supply, CRT monitor, and the system board. Figures in this section are the testpoint and adjustment locations for the HP 1650B/51B.

Calibration Interval

The recommended calibration interval for the HP 1650B/51B is two years. The adjustments are set at the factory on assemblies when they are tested. However, adjustments may be necessary after repairs have been made to the instrument. Usually the only assembly that may require adjustments is the assembly that has been replaced.

Note 

An instrument warm-up of 15 minutes is recommended, but not required, before adjustment procedures are performed.

Warning 

Read the Safety Summary at the beginning of this manual before performing any adjustment procedures.

Caution 

The adjustment procedures are performed with the top cover of the instrument removed. Take care to avoid shorting or damaging internal parts of the instrument.

Safety Requirements

Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These must be observed during all phases of operation, service, and repair of the module. Failure to comply with them violates safety standards of design, manufacture, and intended use of this module. Hewlett-Packard assumes no liability for the failure of the customer to comply with these safety requirements.

Recommended Test Equipment

Recommended test equipment for calibration and adjustment is listed in table 1-3. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended models.

Warning 

Read the safety summary at the front of this manual before any adjustment, replacement, maintenance, or repair is performed.

Instrument Warmup

Adjust and calibrate the instrument at it's environmental ambient temperature and after a 15 minute warm-up.

Calibration

The calibration procedures in this section should be followed in their entirety and in the same sequence as in this section.

Power Supply Assembly Adjustment

1. Disconnect power cord from HP 1650B/51B. Refer to figure 4-1.
2. Connect the negative lead of the voltmeter to Power Supply Assembly ground.
3. Connect the positive lead of the voltmeter to + 5V on the Power Supply Assembly.
4. Connect the power cord to the HP 1650B/51B and put power switch in ON position.
5. Voltmeter should indicate voltage within the range of + 5.180 V to + 5.220 V.
6. If voltmeter reading is out of this range, adjust + 5 ADJ on Power Supply Assembly to + 5.200 V % .050 V (+ 5.180 V to + 5.220 V).

Caution 

High voltages exist on the sweep board that can cause personal injury. Avoid contact with the CRT monitor sweep board when adjusting the + 5V.

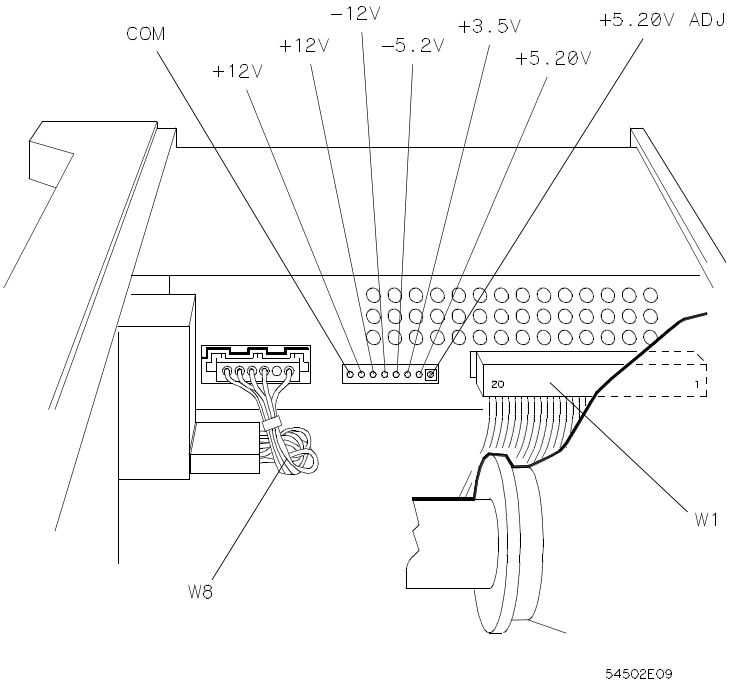


Figure 4-1. Power Supply Adjustments

CRT Monitor Assembly Adjustments

Intensity, Sub-bright, and Contrast Adjustment

1. Refer to figure for adjustment locations.

2. Place **TIMING WAVEFORMS** menu on the screen of the HP 1650B/51B, by pressing front-panel DISPLAY key.

Note

This menu is used because it has characters throughout the screen which are watched during the procedures. Any other menu may be used; however, the adjustments may not be as accurate if characters and/or lines are not displayed throughout the screen.

3. Set rear-panel INTENSITY to the minimum setting.

4. Adjust sweep board SUB BRIGHT control to the lowest setting of brightness where menu is visible on the CRT screen.

Caution

High voltages exist on the sweep board. Avoid contact with the sweep board when making CRT adjustments.

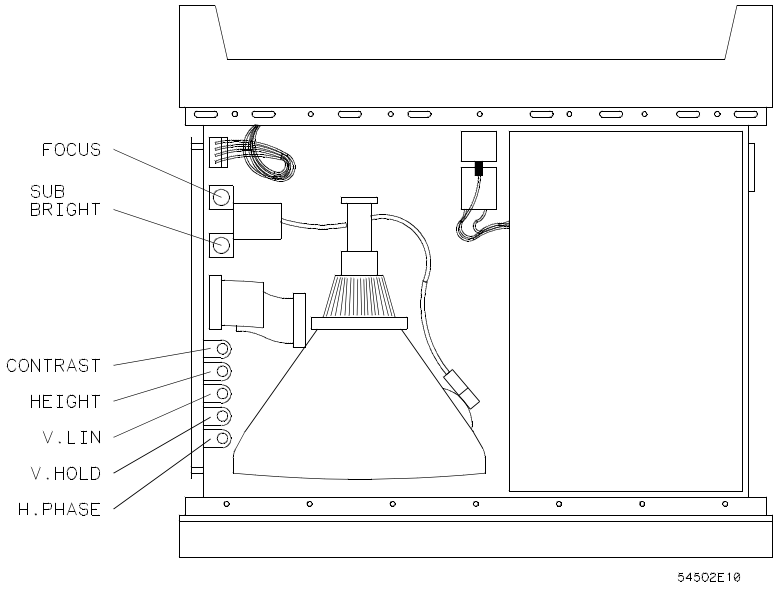


Figure 4-2. CRT Adjustment Locations

5. Turn rear-panel INTENSITY to bring up the intensity level on screen. Screen intensity should be at a comfortable viewing level and the position of both adjustments should be close to mid-range.

6. Press RUN and then STOP.

7. Adjust CONT so the error message is easily seen.

Focus Adjustment

1. Refer to figure for adjustment locations.

2. Place **TIMING WAVEFORMS** menu on the screen of the HP 1650B/51B by pressing the front-panel DISPLAY key.

3. Adjust sweep board FOCUS control for sharp pixels in the center of the screen menu. Note FOCUS control position.

4. Adjust sweep board FOCUS for sharp pixels at the corners of the screen. Note FOCUS control position.

5. Set sweep board FOCUS control for mid-position between the two positions noted in steps 3 and 4 for best over-all pixel focus.

Horizontal Phase, Vertical Linearity, and Height Adjustments

1. Refer to figure for adjustment locations.

2. Place TIMING WAVEFORMS menu on the screen of the HP 1650B/51B by pressing front-panel DISPLAY key.

Note

This menu is used because it has characters and lines throughout the menu which are watched during the procedures. Any other menu may be used, however, the adjustments may not be as accurate.

3. Adjust sweep board H. PHASE to center the menu horizontally on the CRT screen.

4. Adjust sweep board V. LIN so top and bottom rows of text are equal in height. Text height should be approximately 1mm.

Note

The V. LIN and HEIGHT adjustments are interactive and may need to be repeated as necessary.

5. Adjust sweep board HEIGHT to give the screen menu top and bottom borders equal to the side borders of the menu.

6. Readjust steps 4 and 5 as necessary for a uniform display of the screen menu.

System Board Assembly Threshold Adjustment

1. Disconnect power cord from HP 1650B/51B.

2. Connect negative (-) lead of voltmeter to TP GND. Refer to figure 4-3 for testpoint and adjustment locations.

3. Connect positive (+) lead of voltmeter to HP 1650B A1TP3, or HP 1651B A1TP2 on the System Board Assembly.

4. Connect power cord to logic analyzer and turn instrument power to ON.

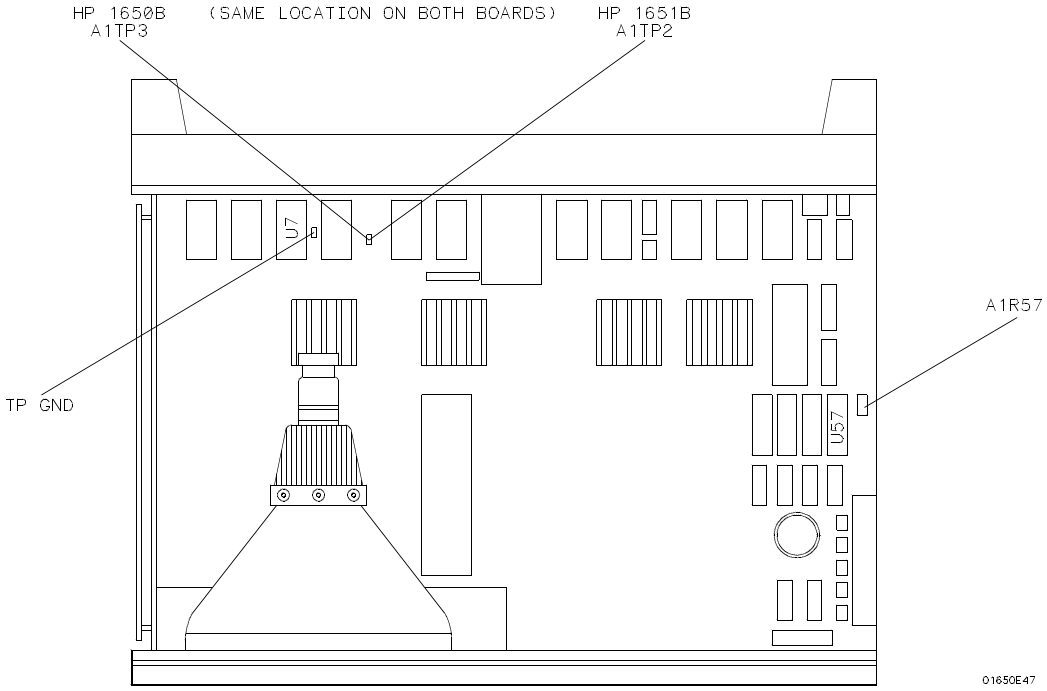


Figure 4-3. System Board Testpoints and Adjustments

5. Assign HP 1650B POD 3, or HP 1651B POD 2, to a machine in the System Configuration menu by using front-panel knob and SELECT key.

6. Set User defined Pod Threshold of the pod assigned in the previous step to -9.9 V in the Format Specification menu by using the following steps if unfamiliar with the menus.

a. Press front-panel FORMAT key.

b. Move cursor to TTL (threshold field) and press SELECT.

c. Assign User defined threshold by using front-panel knob and SELECT key.

7. Voltmeter readout should indicate voltage within the range of -.975 V to -1.005 V (-.990 V % .015 V).

8. Set User defined Pod Threshold of the pod assigned in the previous step to + 9.9 V in the Format Specification menu.

9. Note voltmeter readout. Voltage reading should be within the range of + .975 V to + 1.0005 V (+ .990 V % .015 V).

10. If either voltage reading is not within the given range, use the procedure below to adjust the threshold level.

a. Set User defined Pod threshold of the pod assigned to -9.9 V.

b. Adjust A1R57 for reading of -.9900 V % .0005 V. Refer to figure 4-3 for adjustment locations.

c. Set User defined Pod threshold to + 9.9 V.

d. Note the difference between this reading and + .9900 V.

e. Adjust A1R57 so the difference in step d is halved, % .0005 V.

EXAMPLES If reading is + .9952 V, the difference is .0052 V. Adjust A1R57 for + .9926 V % .0005 V.

If reading is + .9834 V, the difference is .0066 V. Adjust A1R57 for + .9867 V % .0005 V.

Contents

Section 5 Replaceable Parts

Replaceable Parts 5

Introduction

This section contains information for ordering parts. Service support for this instrument is to the assembly level. The replaceable parts include assemblies and chassis parts. Figure 5-1 shows an exploded view of the instrument.

Abbreviations

Table 5-1 lists the abbreviations used in the parts list and throughout this manual. Abbreviations in the replaceable parts list are in capital letters. In other sections of this manual abbreviations may be in uppercase or lowercase letters.

Replaceable Parts List

Table 5-2 is a list of replaceable parts and is organized as follows:

1. Electrical assemblies in alphanumerical order by reference designation.
2. Chassis-mounted parts in alphanumerical order by reference designation.

Information given for each part consists of the following:.

- Reference designation.
- HP part number.
- Part number Check Digit (CD).
- Total quantity (Qty) in the instrument or on the assembly. The total quantity is given once at the first appearance of the part number in the list.
- Description of the part.
- Typical manufacturer of the part in a five digit code. All parts in this list (except hardware) is manufactured by or for Hewlett-Packard, code is 28480. No list of manufacturers is provided.

Exchange Assemblies

Some of the assemblies used in this instrument have been set up on the exchange program. This allows the customer to exchange his faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly. The exchange assemblies have a part number in the form XXXXX-695XX.

After receiving the repaired exchange assembly from Hewlett-Packard, a United States customer has 30 days to return the faulty assembly. For orders not originating in the United States, contact the local HP service organization. If the faulty assembly is not returned within the warranty time limit, the customer will be charged an additional amount. The additional amount will be the difference in price between a new assembly and that of an exchange assembly.

Ordering Information

To order a replaceable part, indicate the HP part number, check digit, and quantity required. Send the order to the nearest HP Sales/Service office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, serial number, description and function of part, and total quantity required. Address an order to the nearest HP Sales/Service office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

- Direct ordering and shipment from HP Parts Center, California, U.S.A. Call your local Hewlett-Packard office for the toll free number.
- No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local HP offices when orders require billing and invoicing).
- Prepaid transportation (there is a small handling charge for each order).
- No invoices.

To provide these advantages, check or money order must accompany each order. Mail order forms and specific ordering information are available through your local HP offices.

Table 5-1. Reference Designator and Abbreviations

REFERENCE DESIGNATOR

A	= assembly	F	= fuse	Q	= transistor;SCR; triode thyristor	U	= integrated circuit; microcircuit
B	= fan;motor	FL	= filter			V	= electron tube; glow lamp
BT	= battery	H	= hardware	R	= resistor		
C	= capacitor	J	= electrical connector (stationary portion);jack	RT	= thermistor	VR	= voltage regulator; breakdown diode
CR	= diode;diode thyristor; varactor	L	= coil;inductor	S	= switch;jumper	W	= cable
DL	= delay line	MP	= misc. mechanical part	T	= transformer	X	= socket
DS	= annunciator;lamp;LED	P	= electrical connector (moveable portion);plug	TB	= terminal board	Y	= crystal unit(piezo-electric or quartz)
E	= misc. electrical part			TP	= test point		

ABBREVIATIONS

A	= amperes	DWL	= dowel
A/D	= analog-to-digital	ECL	= emitter coupled logic
AC	= alternating current	ELAS	= elastomeric
ADJ	= adjust(ment)	EXT	= external
AL	= aluminum	F	= farads;metal film (resistor)
AMPL	= amplifier		
ANLG	= analog	FC	= carbon film/ composition
ANSI	= American National Standards Institute	FD	= feed
		FEM	= female
ASSY	= assembly	FF	= flip-flop
ASTIG	= astigmatism	FL	= flat
ASYNCHRO	= asynchronous	FM	= foam;from
ATTEN	= attenuator	FR	= front
AWG	= American wire gauge	FT	= gain bandwidth product
BAL	= balance		
BCD	= binary-code decimal	FW	= full wave
BD	= board	FXD	= fixed
BFR	= buffer	GEN	= generator
BIN	= binary	GND	= ground(ed)
BRDG	= bridge	GP	= general purpose
BSHG	= bushing	GRAT	= graticule
BW	= bandwidth	GRV	= groove
C	= ceramic;cermet (resistor)	H	= henries;high
		HD	= hardware
CAL	= calibrate;calibration	HDND	= hardened
CC	= carbon composition	HG	= mercury
CCW	= counterclockwise	HGT	= height
CER	= ceramic	HLCL	= helical
CFM	= cubic feet/minute	HORIZ	= horizontal
CH	= choke	HP	= Hewlett-Packard
CHAM	= chamfered	HP-IB	= Hewlett-Packard Interface Bus
CHAN	= channel		
CHAR	= character	HR	= hour(s)
CM	= centimeter	HV	= high voltage
CMOS	= complementary metal-oxide-semiconductor	HZ	= Hertz
		I/O	= input/output
CMR	= common mode rejection	IC	= integrated circuit
		ID	= inside diameter
CNDCT	= conductor	IN	= inch
CNTR	= counter	INCL	= include(s)
CON	= connector	INCAND	= incandescent
CONT	= contact	INP	= input
CRT	= cathode-ray tube	INTEN	= intensity
CW	= clockwise	INTL	= internal
D	= diameter	INV	= inverter
D/A	= digital-to-analog	JFET	= junction field-effect transistor
DAC	= digital-to-analog converter		
		JKT	= jacket
DARL	= darlington	K	= kilo(10^3)
DAT	= data	L	= low
DBL	= double	LB	= pound
DBM	= decibel referenced to 1mW	LCH	= latch
		LCL	= local
DC	= direct current	LED	= light-emitting diode
DCDR	= decoder		
DEG	= degree	LG	= long
DEMUX	= demultiplexer	LI	= lithium
DET	= detector	LK	= lock
DIA	= diameter	LKWR	= lockwasher
DIP	= dual in-line package	LS	= low power Schottky
DIV	= division	LV	= low voltage
DMA	= direct memory access	M	= mega(10^6);megohms; meter(distance)
DPDT	= double-pole, double-throw		
		MACH	= machine
DRC	= DAC refresh controller	MAX	= maximum
DRVR	= driver		

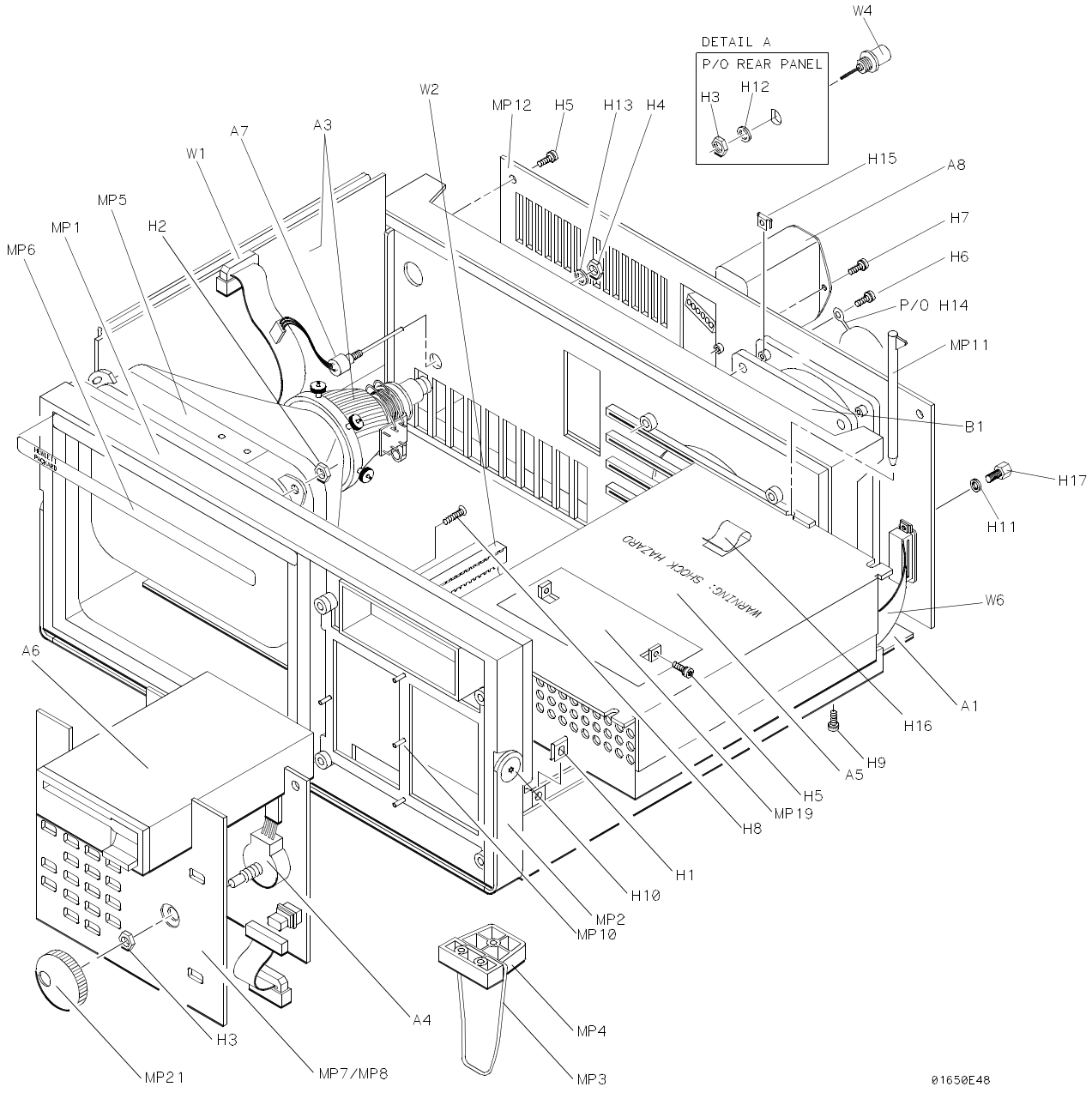


Figure 5-1. HP 1650B/51B Exploded View

Table 5-2. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	01652-66501	0	1	SYSTEM BOARD ASSEMBLY – 80 CHANNEL (1650B)	28480	01652-66501
A1	01653-66501	1	1	SYSTEM BOARD ASSEMBLY – 32 CHANNEL (1651B)	28480	01653-66501
A2	01650-66503	0	1	KEYBOARD CIRCUIT BOARD ASSEMBLY	28480	01650-66503
A3	2090-0204	9	1	MONITOR ASSEMBLY	28480	2090-0204
A4	0960-0753	6	1	ROTARY PULSE GENERATOR	28480	0960-0753
A5	0950-1879	8	1	POWER SUPPLY ASSEMBLY	28480	0950-1879
A6	0950-1798	0	1	DISK DRIVE ASSEMBLY	28480	0950-1798
A7	01650-61614	4	1	INTENSITY ADJUSTMENT ASSEMBLY	28480	01650-61614
A8	9135-0325	8	1	LINE FILTER SWITCH ASSEMBLY	28480	9135-0325
A9	01650-61608	6	5	PROBE TIP ASSEMBLY (1650B)	28480	01650-61608
A9	01650-61608	6	2	PROBE TIP ASSEMBLY (1651B)	28480	01650-61608
B1	3160-0429	0	1	FAN-TUBEAXIAL 100-CFM 12VDC	28480	3160-0429
E1	5959-9333	8	0	REPLACEMENT PROBE LEADS (PKG OF 5)	28480	5959-9333
E2	5959-9334	9	0	REPLACEMENT PROBE GROUNDS (PGK OF 5)	28480	5959-9334
E3	5959-9335	0	0	REPLACEMENT POD GROUNDS (PKG OF 5)	28480	5959-9335
E4	5959-0288	4	5	GRABBER ASSEMBLY SET – 20	28480	5959-0288
E4	5959-0288	4	2	GRABBER ASSEMBLY SET-20 (1651B)	28480	5959-0288
F1	2110-0003	0	1	FUSE 3A 250V NTD FE UL	28480	2110-0003
H1	0535-0113	1	10	NUT "U"-TP M3 X 0.500.3MM-THK (TOP COVER)	28480	0535-0113
H2	0535-0056	1	4	NUT-HEX PRVLG-TRQ M4 X 0.7 5MM-THK (CRT)	28480	0535-0056
H3	2950-0001	8	3	NUT-DBL-CHAM 3/8-32-THD0.094-IN-THK (RPG, BNC)	28480	2950-0001
H4	2950-0072	3	1	NUT-DBL-CHAM 1/4-32-THD0.062-IN-THK (INTEN ADJ)	28480	2950-0072
H5	0515-0372	2	10	SCREW M3 X 0.5 8MM-LG (DISK DRIVE, REAR PANEL)	28480	0515-0372
H6	0515-0821	6	4	SCREW- M3.5 X 0.6 (FAN)	28480	0515-0821
H7	0515-1035	6	22	SCREW-M3 X 0.5 8MM- (FEET, LINE FIL, TOP COVER)	28480	0515-1035
H8	0515-1135	7	4	SCREW- M3 X 0.5 25MM-LG (KEYPAD)	28480	0515-1135
H9	0515-1951	5	8	SCREW-TAPPING M4.2 (SYSTEM BOARD)	28480	0515-1951
H10	01650-82401	1	2	M5 SHOULDER SCREW (HANDLE)	28480	01650-82401
H11	2190-0009	4	2	WASHER-LK INTL T NO. 80.168-IN-ID	28480	2190-0009
H12	2190-0016	3	2	WASHER-LK INTL T 3/8 IN0.377-IN-ID (BNC)	28480	2190-0016
H13	2190-0027	6	1	WASHER-LK INTL T 1/4 IN0.256-IN-ID (INTEN ADJ)	28480	2190-0027
H14	3160-0092	3	1	FAN GUARD	28480	3160-0092
H15	0590-1868	1	4	FAN MOUNTING CLIP	28480	0590-1868
H16	1400-0611	0	1	CLAMP-FL-CA 1-WD (DISK DRIVE CABLE)	28480	1400-0611
H17	0380-1482	5	2	HEX STANDOFF .0340 (HP-IB CABLE)	28480	0380-1482
H18	01650-00203	3	2	NUT PLATE (HANDLE)	28480	01650-00203
MP1	01650-45201	1	1	ELAN CABINET MOLDED PLASTIC	28480	01650-45201
MP2	01650-04901	2	1	BALE HANDLE	28480	01650-04901
MP3	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP4	01650-47701	0	2	MOLDED FOOT	28480	01650-47701
MP5	01650-01202	0	1	GROUND BRACKET	28480	01650-01202
MP6	01650-94307	1	1	IDENTIFICATION LABEL (1650B)	28480	01650-94307
MP6	01651-94302	7	1	IDENTIFICATION LABEL (1651B)	28480	01651-94302
MP7	01650-94306	0	1	KEYBOARD LABEL	28480	01650-94306
MP8	01650-45206	6	1	KEYBOARD HOUSING	28480	01650-45206
MP9	01650-41901	0	1	ELASTOMERIC KEYPAD	28480	01650-41901

Table 5-2. Replaceable Parts List (continued)

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
MP10	01650-45205	5	1	KEYBOARD SPACER	28480	01650-45205
MP11	01650-46101	2	2	LOCKING PIN PCB	28480	01650-46101
MP12	01650-00205	1	1	REAR PANEL (1650B)	28480	01650-00205
MP12	01651-00203	0	1	REAR PANEL (1651B)	28480	01651-00203
MP13	7120-4835	0	1	CSA CERTIFICATION LABEL	28480	7120-4835
MP14	01650-04101	4	1	TOP COVER	28480	01650-04101
MP15	01650-84501	6	1	ACCESSORY POUCH	28480	01650-84501
MP16	01650-94303	7	1	PROBE LABELS	28480	01650-94303
MP17	01650-29101	6	5	GROUND SPRING (SYSTEM BOARD 1650B) -	28480	01650-29101
MP17	01650-29101	6	2	GROUND SPRING (SYSTEM BOARD 1651B)	28480	01650-29101
MP18	01650-29102	7	1	CLIP RS-232 ESD	28480	01650-29102
MP19	01650-25401	1	1	INSULATOR-ELAN DISK	28480	01650-25401
MP20	01650-63202	0	1	RS-232 LOOPBACK CONNECTOR	28480	01650-63202
MP21	01650-47401	7	1	RPG KNOB	28480	01650-47401
W1	01650-61601	9	1	SWEEP CABLE	28480	01650-61601
W2	54503-61606	7	1	POWER SUPPLY CABLE	28480	54503-61606
W3	01650-61604	2	1	DISK CABLE	28480	01650-61604
W4	01650-61605	3	2	BNC CABLE	28480	01650-61605
W5	01650-61607	5	5	PROBE CABLE (1650B)	28480	01650-61607
W5	01650-61607	5	2	PROBE CABLE (1651B)	28480	01650-61607
W6	01650-61613	3	1	HP-IB CABLE	28480	01650-61613
W7	01650-61616	6	1	FAN CABLE	28480	01650-61616

Section 6

Service

6

Service

Introduction

This section provides troubleshooting, service, and repair information for the HP 1650B/51B Logic Analyzer. Troubleshooting consists of flowcharts, self- test descriptions and instructions for use, and signal level tables. The troubleshooting information is provided to isolate a faulty assembly. When a faulty assembly has been located, the disassembly/assembly procedures help direct replacement of the assembly.

Safety

Read the Safety Summary at the front of this manual before servicing the instrument. Before performing any procedure, review it for cautions and warnings.

Warning 

Maintenance should be performed by trained service personnel aware of the hazards involved (for example, fire and electric shock). When maintenance can be performed without power applied, the power cord should be removed from the instrument.

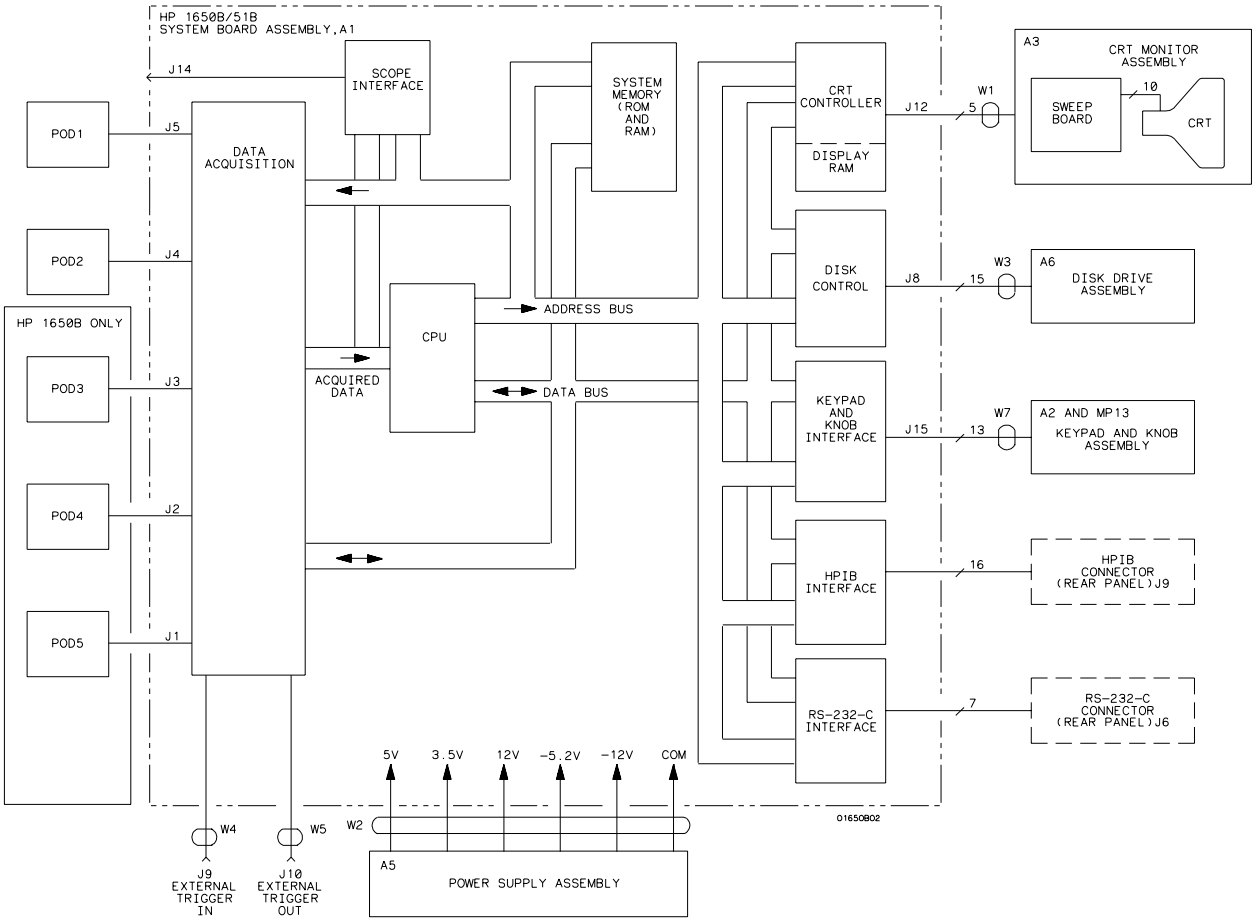


Figure 6-1. Simplified Block Diagram

Theory of Operation

The HP 1650B/51B Logic Analyzer is an 80/32 channel state and timing logic analyzer. The human interface is a front-panel keypad and knob for instrument control and 9" (diagonal) white phosphor CRT for information display. Available on the rear panel are RS-232-C and HP-IB ports for communication to a printer or from a controller. Also on the rear panel are two BNCs for input or output of an external trigger.

The System Assembly Board is built around the 68000 microprocessor and powerful data acquisition ICs that probe, shape, store, and analyze data from a target system. An acquisition interface to the 68000 makes the acquisition system fully compatible with the architecture of the 68000 microprocessor. The System Assembly contains the necessary circuitry to interface the keypad, CRT monitor, disk drive, RS-232-C and HP-IB ports.

Figure 6-1 is a simplified block diagram of the instrument. The hardware of the HP 1650B/51B consists of four main assemblies. Also shown are rear panel connectors. This manual supports troubleshooting to assembly level. Theory of operation for the System Assembly is included for information only and is not intended for troubleshooting purposes.

Data Acquisition

The data acquisition of the System Assembly consists of the data acquisition pods, acquisition ICs, and the interface to the 68000. The interface to the target system is through any of the data acquisition pods. There are five pods available on the HP 1650B (80 channels) and two pods available on the HP 1651B (32 channels). Each pod contains 16 input data probes and one external clock input for state mode measurements. The data probes can be used for state or timing measurements.

Each pod consists of a probe tip assembly and a 4.5 foot woven cable. A probe tip assembly includes 17 twelve-inch probes and a common ground return. This is connected to one end of the cable. The other end of the woven cable terminates at the rear panel of the logic analyzer. The woven cable consists of 17 nichrome signal lines, 34 signal return lines and 2 power supply lines. All are woven together with polyarmid yarn.

Each probe input has an input impedance of 100k ohms in parallel with approximately 8 pF. The probes can be grounded in two ways: with a common pod ground for state measurements, or a probe tip ground for higher frequency measurements.

The input signals are attenuated by a factor of 10 in the passive probe. The signals are applied to a comparator where they are compared against a voltage threshold to determine if the voltage level is above or below the threshold level. The comparator then shapes the single-ended signal and outputs it at an ECL level to the acquisition IC. The input data is then stored at the acquisition IC.

Arming Control

The two BNCs on the rear panel are used for arming control of the logic analyzer acquisition ICs. An arm signal may be output from the ICs to the rear panel EXTERNAL TRIGGER OUT (J10), or input to the ICs from EXTERNAL TRIGGER IN (J9).

Memory

The memory of the logic analyzer consists of three separate memories: one ROM and two RAMs. The system (EP)ROM is 64K long by 8 wide and is used primarily for booting-up the system and self-test storage. The system (D)RAM is 1M long by 8 wide and contains the operating system and the acquired data from the target system. Since the RAM is a volatile memory, the operating system is loaded loaded at each power-up of the instrument via the built-in disk drive and a mini floppy disk.

The display (D)RAM is 64K long by 4 wide and is cycle shared between the 68000 and the display refresh cicuitry. This is why the display bus is separate from the local bus. The two buses are separated by a set of address multiplexers and data buffers.

CRT Controller

The CRT controller provides the synchronization and timing signals needed by the CRT Monitor Assembly to drive the CRT.

The controller generates four signals: Horizontal sync, vertical sync, display enable and a 6.25 kHz signal. The horizontal and vertial sync signals are applied to the CRT monitor assembly and to display PALs. The display PALs use the sync signals to generate the timing signals for the display RAM.

The CRT Monitor Assembly consists of the sweep board circuitry, a 9-inch white phosphor display CRT, and the CRT yoke. The assembly requires + 5 and + 12 volts, which it receives from the power supply via the System Board Assembly.

Disk Controller

The disk controller performs the necessary functions for reading or writing data to the built-in disk drive of the logic analyzer. The disk controller interface to the 68000 is an 8-bit bidirectional bus for data, status, and control word transfers.

The built-in disk drive is a 3.5-inch double-sided Sony disk drive. The main features of the disk drive are low power consumption, low height, and high reliability with simple mechanism and electronic circuitry.

Keypad and Knob Interface

The keypad and knob interface provide the circuitry to latch and send the keypad and knob data to the 68000.

The keypad is elastomeric and each key has a single function.

RS-232-C Interface

The controlling IC of the RS-232-C Interface is a Signetics SCN2661 Enhanced Programmable Communications Interface (EPCI), a universal synchronous/asynchronous receiver/transmitter (USART) data communications IC.

The SCN2661 serializes parallel data from the 68000 for transmission. At the same time, it also receives serial data and converts it to parallel data characters for the 68000.

The IC contains a baud rate generator which can be programmed from the logic analyzer I/O menu for one of eight baud rates. Protocol, word length, stop bits length, and parity are also programmed via the I/O menu.

The DS14C88 and DS14C89 are line drivers/receivers used by the logic analyzer for interface of terminal equipment with data communications equipment. Slew rate control is provided on the ICs eliminating the need for external capacitors.

Power Supply Assembly

The switching power supply provides 120 W (200 W maximum) for the instrument. The ac input to the power supply is 115V or 230 V, -25 to + 15%. Maximum input power is 350 VA maximum. The ac input frequency is 48 - 66 Hz.

All voltages necessary to operate the instrument are applied first to the System Assembly. Unfiltered voltages of + 12V, -12V, + 5.2V, -5.2V and + 3.5V are supplied to the board where they are then filtered and distributed throughout the board and to the CRT Monitor Assembly. Filtered voltages of approximately + 5 V and + 12 V are routed through the System Assembly to the CRT Monitor Assembly. The + 5.2 V supply is adjustable on the supply.

Trouble Isolation Flowcharts

The trouble isolation flowcharts are the troubleshooting guide. Start there when repairing a defective instrument.

The flowcharts refer to other tests, tables, and procedures to help isolate trouble. Disassembly procedures are included to direct in replacing faulty assemblies. The circled numbers on charts indicate the next chart to use for isolating a problem.

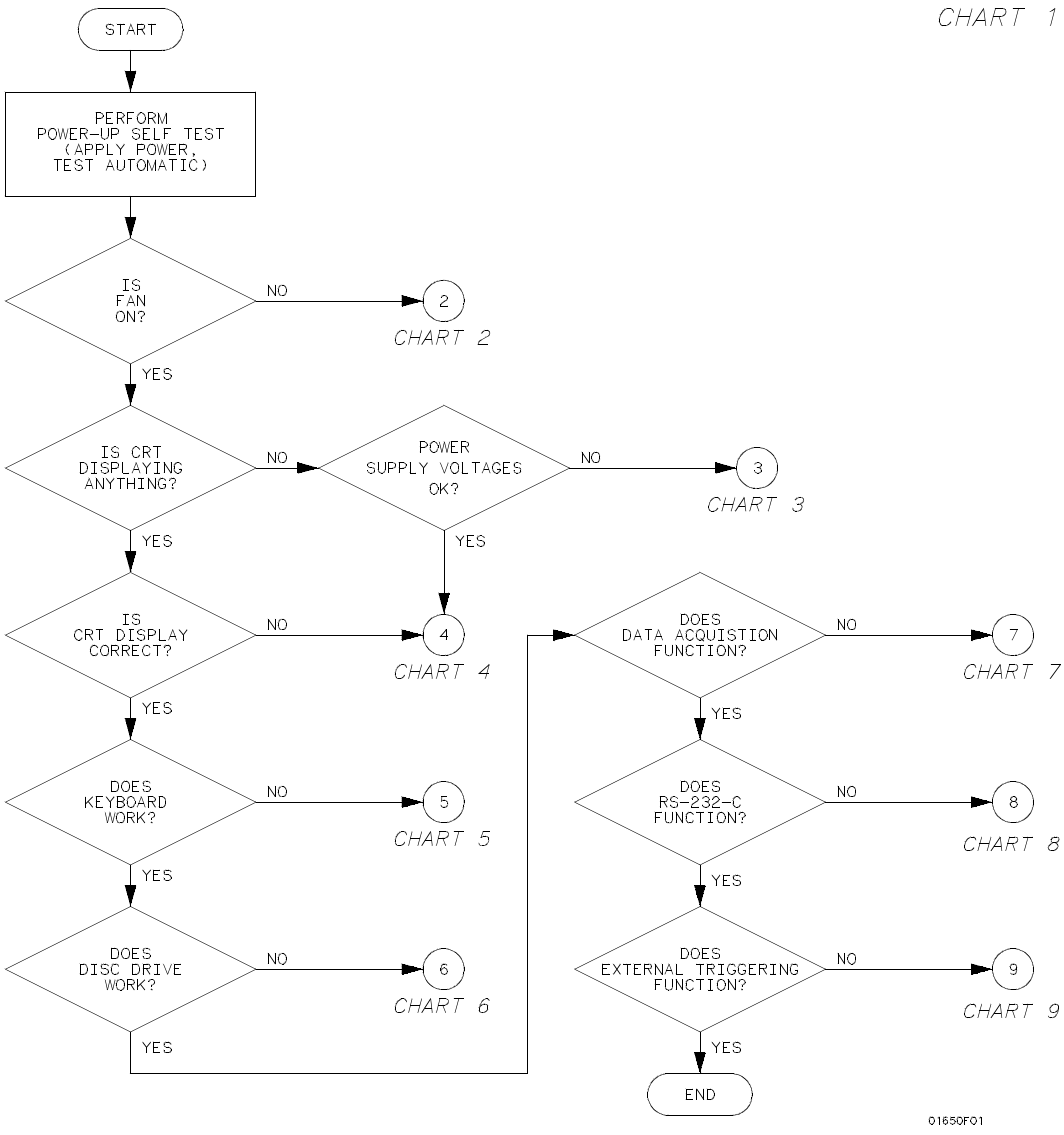


Figure 6-2. Primary Troubleshooting Flowchart

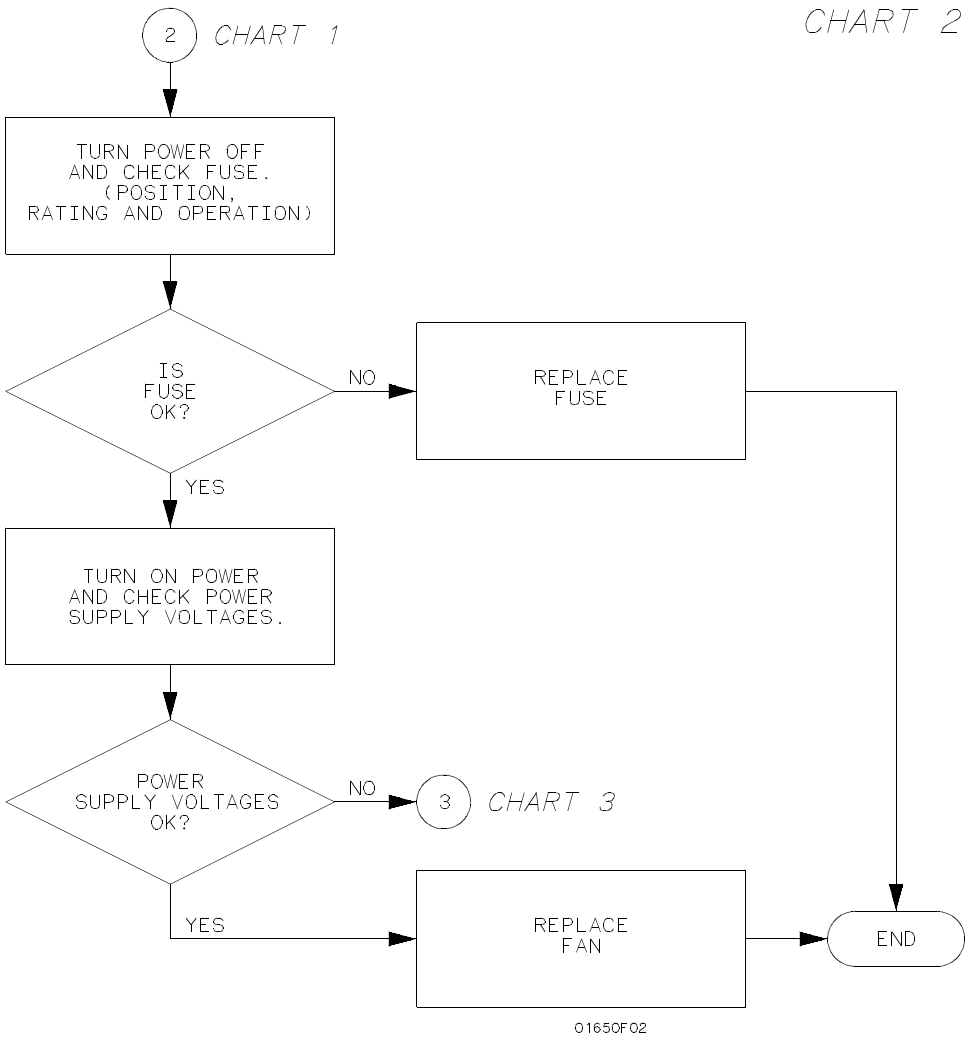


Figure 6-3. Trouble Isolation Flowchart for Fan/Fuse

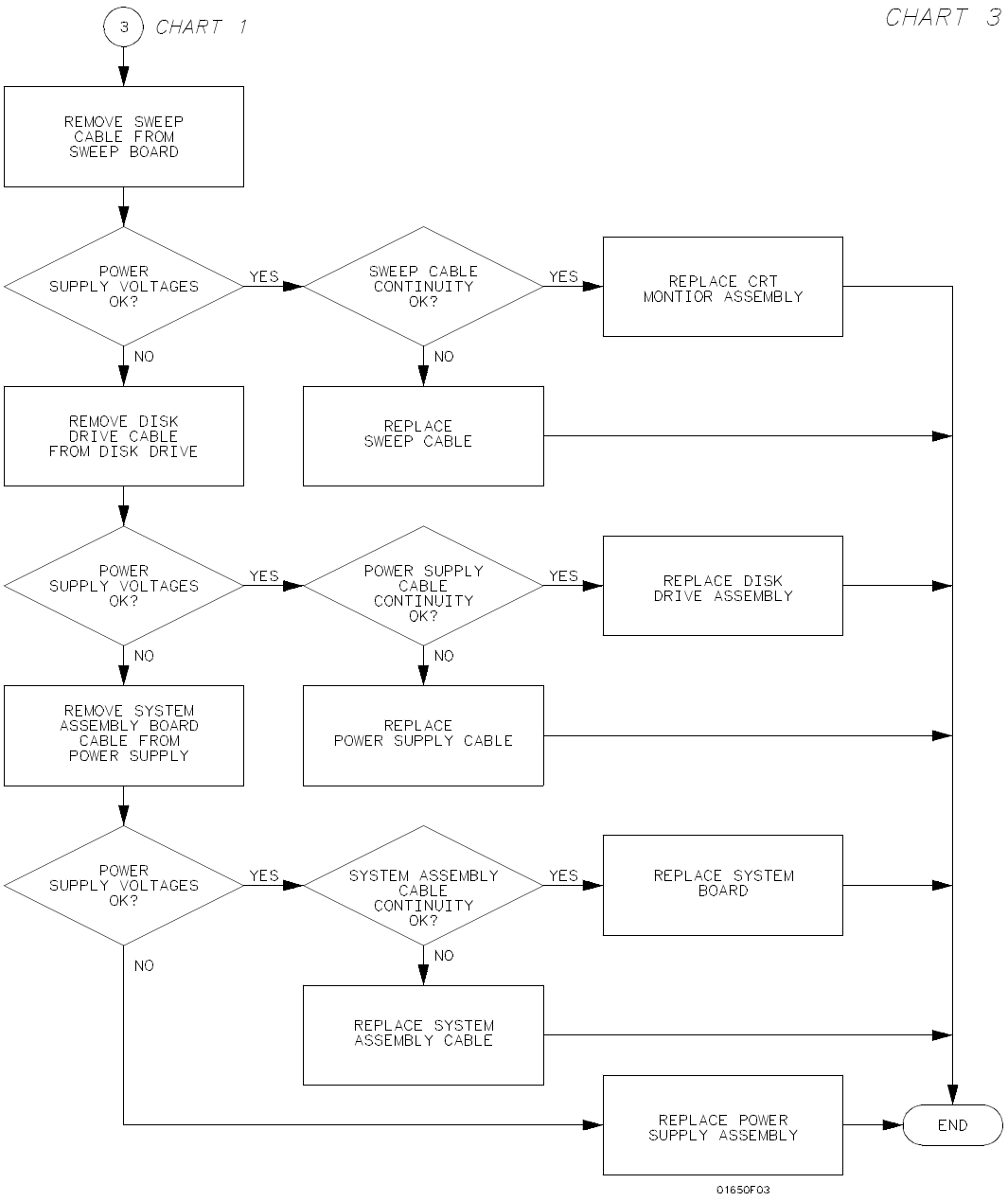


Figure 6-4. Trouble Isolation for Power Supply

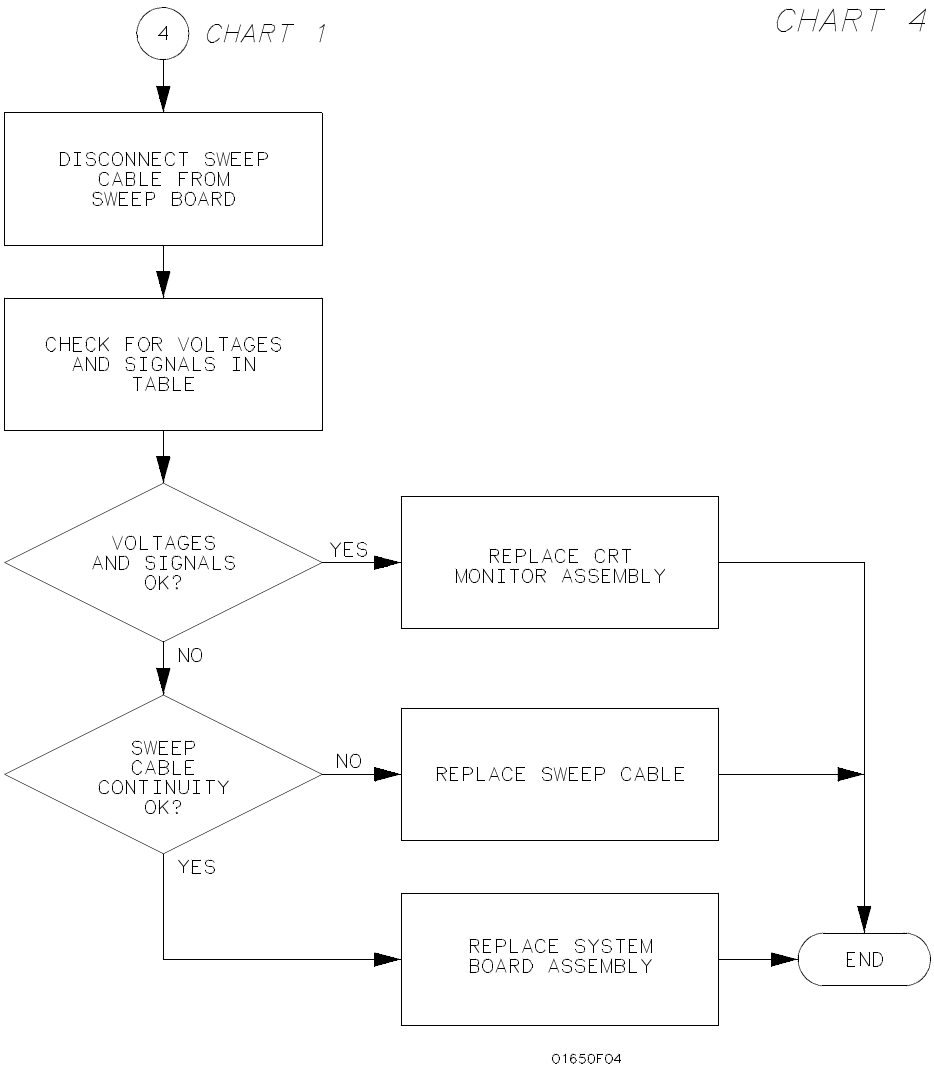


Figure 6-5. Trouble Isolation for CRT Monitor

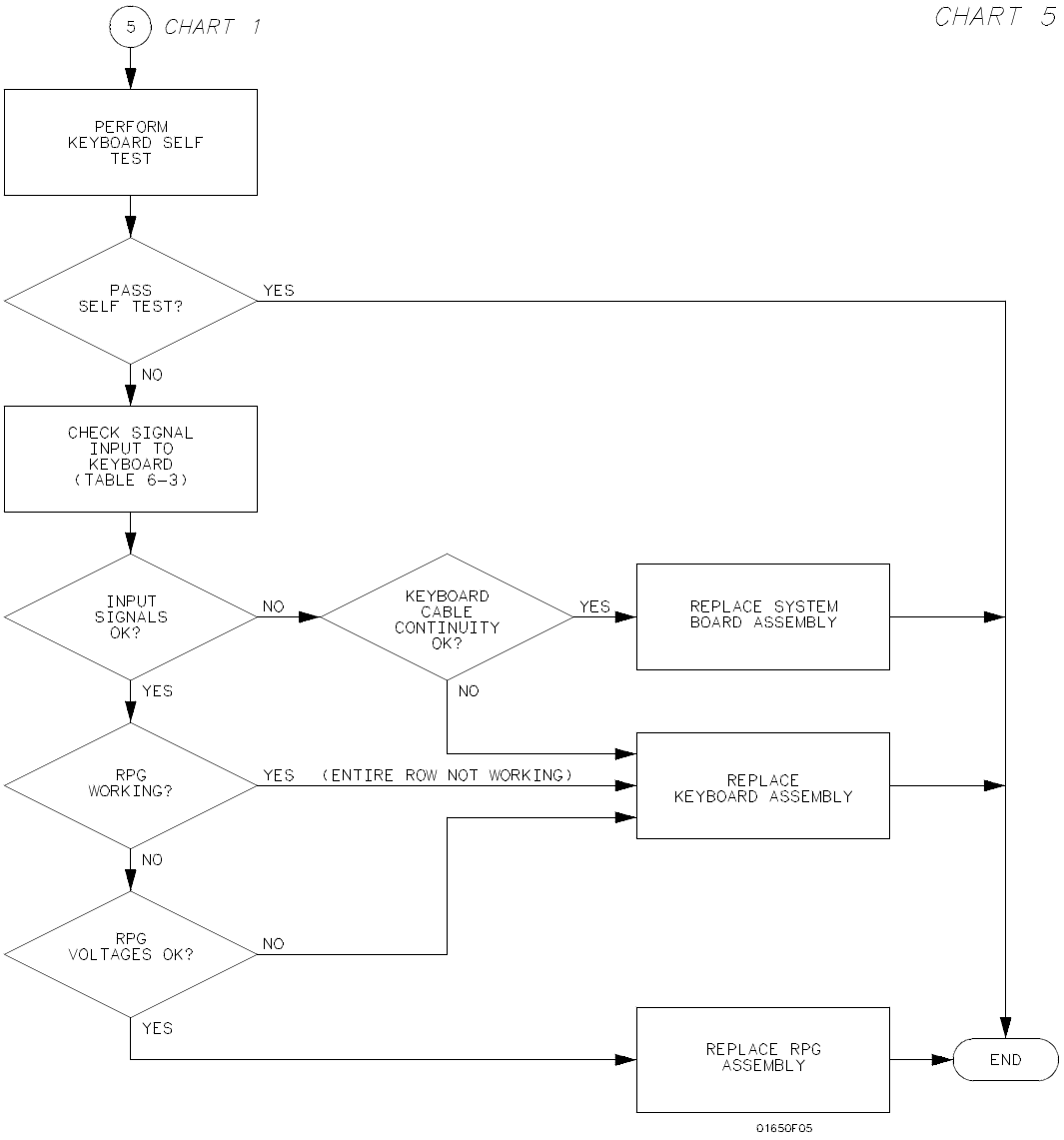


Figure 6-6. Trouble Isolation for Flowchart

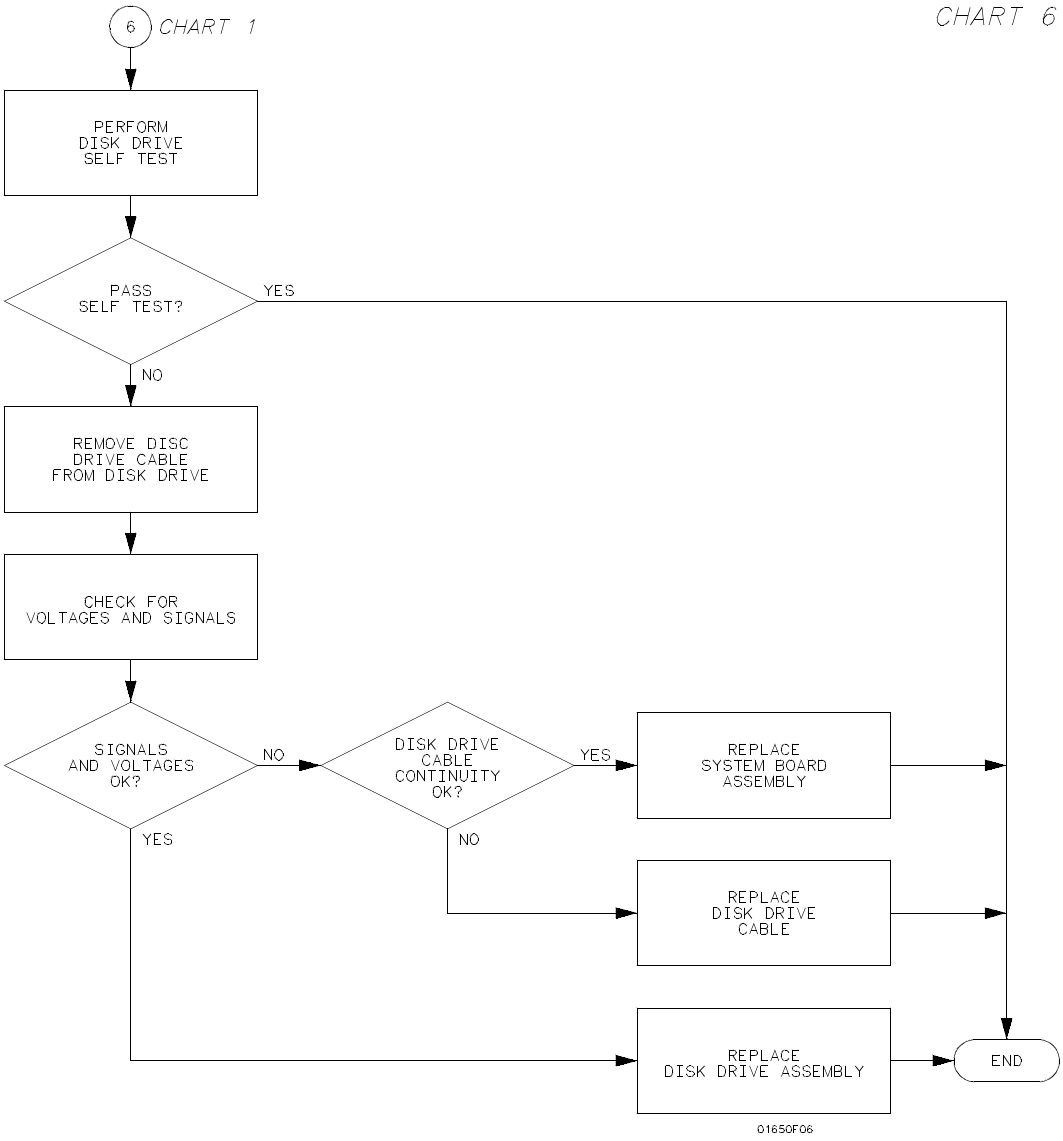


Figure 6-7. Trouble Isolation for Disk Drive

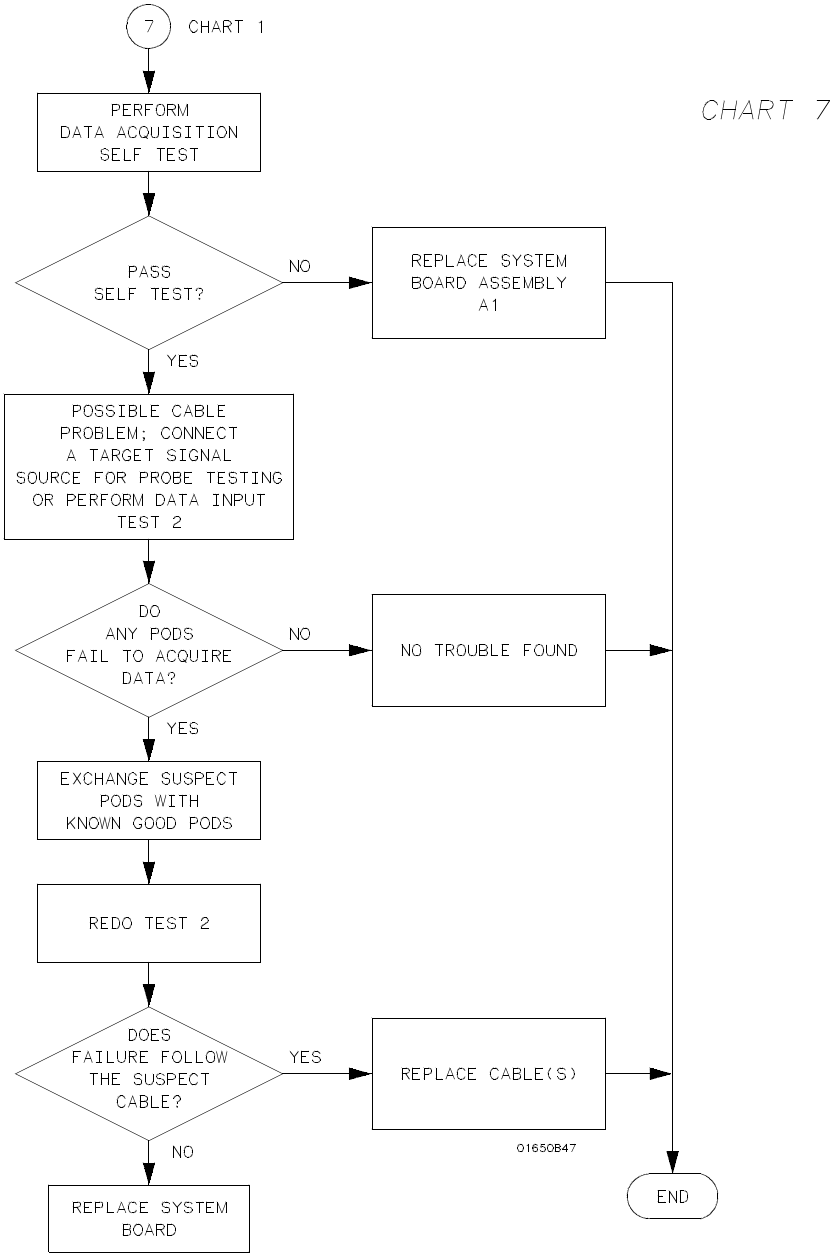


Figure 6-8. Trouble Isolation for Data Acquisition

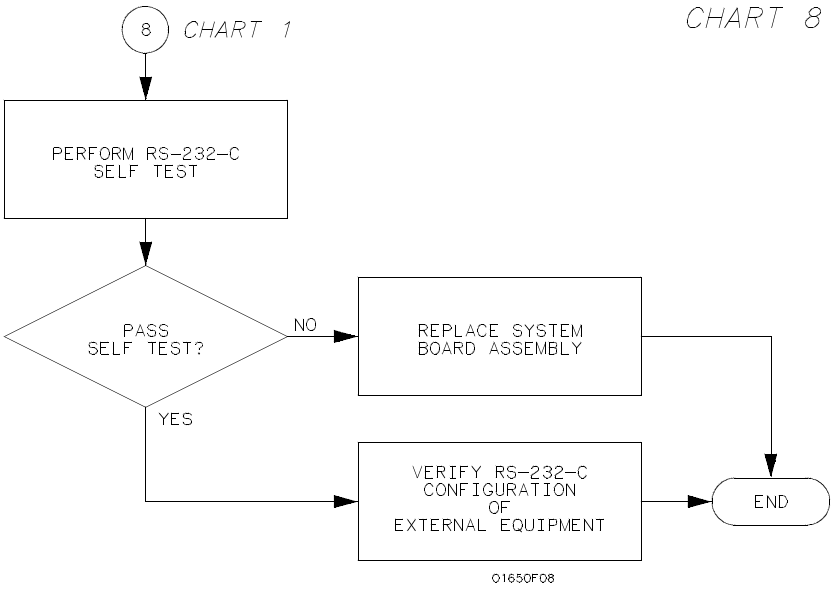


Figure 6-9. Trouble Isolation for RS-232-C

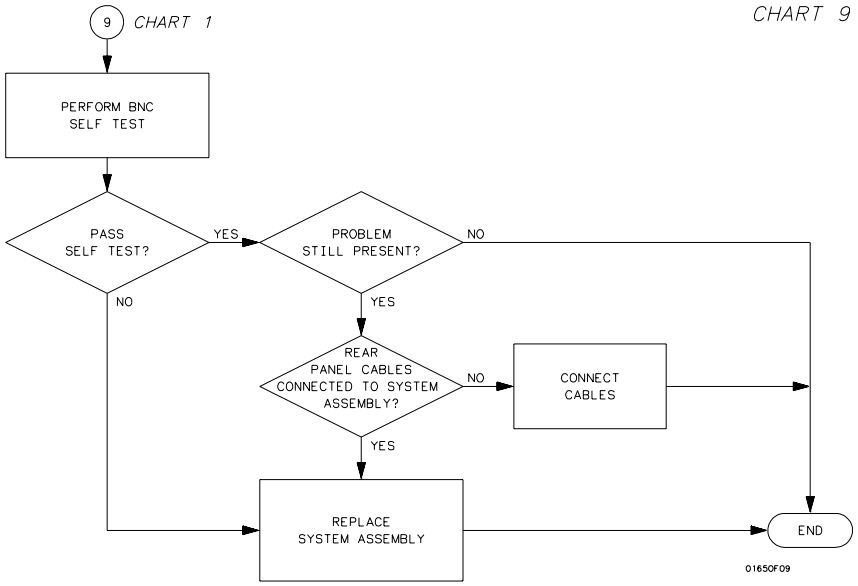


Figure 6-10. Trouble Isolation for BNC

Power Supply Voltages Check

The power supply must be loaded by either the System Assembly Board or with an added resistor to check the voltages.

Warning **This procedure is to be performed only by service-trained personnel aware of the hazards involved (such as fire and electrical shock).**

Power Supply Loaded by System Assembly

1. Remove instrument top cover.
2. Using the figure below, check for the voltages indicated at the testpoints.

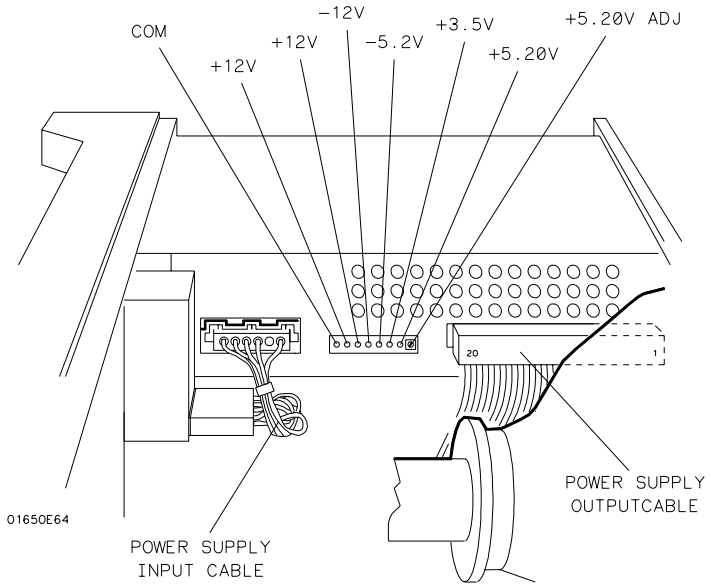


Figure 6-11. Power Supply Test Points

Power Supply Isolated

Isolate and check the supply with the following steps. Use the figure above for reference.

1. Remove instrument power cable.
2. Disconnect supply output cable at supply (see figure above).
3. Load + 5.20 V supply with a 2 ohm 25 watt resistor. Use jumper wires to connect one end of the resistor to any of pins 1-4, and the other end to any of pins 5-8.

4. Reconnect instrument power cable and check for voltages at the supply output using values in the following table.

Table 6-1. Power Supply/Main Assembly Voltages

PIN	SIGNAL	PIN	SIGNAL
1	+5.20 V	11	-5.2 V
2	+5.20 V	12	GROUND
3	+5.20 V	13	+12 V
4	+5.20 V	14	GROUND
5	GROUND (Display)	15	-12 V
6	GROUND (Digital)	16	GROUND
7	GROUND (Digital)	17	+12 V (Display)
8	GROUND	18	-5.2 V
9	+3.5 V	19	+15.5 V (Fan)
10	GROUND	20	GROUND (Fan)

Note

The ground planes (digital, fan, and display) are at the same potential on the power supply, but when measuring on the main assembly the supplies must be measured with reference to the respective ground.

CRT Monitor Signals Check

1. Remove instrument top cover.
2. Check the CRT Monitor input cable for the signals and supplies listed in the table below. The cable is the wide ribbon cable connecting the monitor to the System Assembly Board.
3. Dynamic video signals FB (Full-bright) and HB (Half-bright) are TTL inputs. Check for activity on these lines. The table includes a truth table for these signals.

Table 6-2. CRT Monitor Input Cable Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
1	+5 V (Digital)	2	+12 V (Display)
3	GROUND (Display)	4	GROUND (Display)
5	+12 V (Display)	6	GROUND (Display)
7	+12 V (Display)	8	GROUND (Display)
9	+12 V (Display)	10	HSYNC
11	VSYNC	12	+12 V (Display)
13	GROUND (Digital)	14	GROUND (Digital)
15	GROUND (Display)	16	FB (Full-bright)
17	GROUND (Display)	18	HB (Half-bright)
19	GROUND (Display)	20	+5 V (Digital)

FB	HB	VIDEO
0	0	OFF
0	1	HALF
1	0	FULL
1	1	FULL

Keyboard Signals Check

Isolate a faulty elastomeric keypad or keyboard when random key(s) not operating by performing the following steps.

1. Remove instrument power cable.
2. Without disconnecting the keyboard cable, follow keyboard removal procedure to loosen keyboard. Leave keyboard in place in front of instrument.
3. Apply power.
4. Run Keyboard Self Test and press all keys.
5. Allow keyboard assembly to fall forward from front panel. Separate the elastomeric keypad and keyboard panel from the PC board.
6. Short PC board trace (with a paper clip or screwdriver) of non-operating key and look for appropriate response on display.
7. If display responds as if key were pressed, replace elastomeric keypad.
8. If display does not respond as if key were pressed, replace keyboard.

The RPG connector has a TTL pulse on pins 1 and 3, when the knob is being turned. Pin 5 of the connector is + 5 V.

The ROW (scan) signal is approximately 60 Hz, a low duty-cycle pulse. It is continually present on pins 11 through 18 of the keyboard cable. Because of the resistance of the keypad contacts, the signal does not appear the same on the COLUMN (data) pins when keys are pressed. Refer to the following table for signals going to and from the keyboard.

Table 6-3. Keyboard Connector Voltages and Signals

PIN	SIGNAL	PIN	SIGNAL
1	RPGA	2	RPGB
3	COLUMN 1 (Data)	4	COLUMN 2 (Data)
5	COLUMN 3 (Data)	6	COLUMN 4 (Data)
7	COLUMN 5 (Data)	8	COLUMN 6 (Data)
9	COLUMN 7 (Data)	10	COLUMN 8 (Data)
11	ROW 8 (Scan)	12	ROW 7 (Scan)
13	ROW 6 (Scan)	14	ROW 5 (Scan)
15	ROW 4 (Scan)	16	ROW 3 (Scan)
17	ROW 2 (Scan)	18	ROW 1 (Scan)
19	+5 V (Digital)	20	GROUND (Digital)

Assembly Removal and Replacement

This section contains the procedures for removal and installation of major assemblies. Read the Safety Summary at the front of this manual before servicing the instrument.

Warning

Hazardous voltages exist on the power supply, CRT, and the display sweep board. To avoid electrical shock, adhere closely to the following procedures. Also, after disconnecting power cable, wait at least three minutes for capacitors on the power supply and sweep boards to discharge before servicing this instrument.

Caution

Never remove or install any assembly with the instrument power ON. Component damage can occur.

Caution

The effects of ELECTROSTATIC DISCHARGE may damage components. Use grounded wriststraps and mats when servicing the System Assembly Board.

Removal and Replacement of System Assembly Board

1. Disconnect pod cables from rear of instrument.
2. Disconnect power cable.
3. Remove ten screws securing top cover. Remove top cover.
4. Disconnect disk drive cable from disk drive.
5. Remove two screws securing disk drive to power supply. Remove disk drive by sliding assembly out front panel of instrument.
6. Remove two retaining pins securing power supply to chassis. Slide power supply out far enough to gain unobstructed access to power supply cables.
7. Disconnect power supply line input and DC output cables. Remove power supply.
8. Disconnect video sweep cable, BNC trigger cables, disk drive cable, keyboard cable, fan cable, power supply DC output cable, and HP-IB cable from system board.
9. Remove eight screws securing rear panel to chassis. Remove rear panel.
10. Remove RS-232 ESD ground spring from RS-232 connector.
11. Carefully place instrument in a front-panel-down position (or on its side) and remove eight screws securing system board to chassis (on underside of instrument).
12. Carefully slide system board out rear of instrument.
13. Carefully slide new system board through rear of instrument.

14. Secure system board to chassis with eight screws.

Note 

Hand-start the self-tapping screws securing the system board. Otherwise, if the holes are not aligned, damage to the board will result.

15. Set instrument upright. Install RS-232 ESD spring ground on RS-232 connector. Ensure angled wing tabs of spring ground points toward rear of instrument.

16. Place rear panel close enough to chassis to route cables through the rear of the instrument.

17. Install rear panel. Ensure cables slide completely through rear of chassis. Secure panel to instrument with eight screws.

18. Connect HP-IB cable, power supply DC output cable, fan cable, keyboard cable, disk drive cable, BNC trigger cable, and video sweep cable to system board.

Note 

Ensure BNC trigger cables are properly connected to system board. The EXTERNAL TRIGGER INPUT is connected to J9 of the system board, and the EXTERNAL TRIGGER OUTPUT is connected to J10 of the system board.

19. Slide power supply in far enough to connect line input cable and DC output cable. Connect cables and slide power supply in completely. Secure power supply using two retaining pins.

20. Slide disk drive through front panel of instrument. Secure disk drive to power supply using two screws.

21. Connect disk drive cable to disk drive.

22. Install top cover. Secure top cover to chassis using ten screws.

Note 

To ensure top cover is properly installed, secure side screws of top cover before securing top screws.

23. Verify instrument performance by executing Extended Performance Verification program on Operating System disk.

Removal and Replacement of CRT Monitor Assembly

1. Disconnect pod cables from rear of instrument.
2. Disconnect power cable.
3. Remove ten screws securing top cover. Remove top cover.
4. Connect a jumper lead between ground lug of CRT and shaft of a screwdriver. To discharge CRT, place screwdriver under protestive rubber cap of post accelerator lead and momentarily touch screwdriver to metal clip of post accelerator lead.

Caution

Discharge the post accelerator lead to a grounding lug only. Components will be damaged if the post accelerator is discharged to other areas.

Note

The CRT may charge by itself even while disconnected. Discharge the CRT before handling by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead.

5. Disconnect post accelerator lead from CRT by firmly squeezing rubber cap until metal clip disengages from CRT.
6. Detach intensity cable from sweep board.
7. Disconnect sweep cable assembly from sweep board and CRT cables from from CRT and Sweep board.
8. Slide sweep board up and out of cabinet slot.

Note

When installing sweep board, it may be necessary to press on center of outer shield of sweep board to allow the board to clear cabinet support rib.

9. Carefully place instrument in front-panel-down position.
10. To remove CRT, remove the four locknuts securing the CRT to front panel. Remove CRT and ground bracket from front panel of instrument.

Note

When installing CRT, make certain that CRT yoke is properly aligned. THE GROUND BRACKET MUST BE INSTALLED BEFORE THE CRT.

11. To install CRT Monitor Assembly, reverse this procedure.

Note

After replacement of CRT Monitor Assembly, perform the CRT adjustment procedures in section 4 of this manual.

Removal and Replacement of Power Supply

1. Disconnect pod cables from rear of instrument.
2. Disconnect power cable.
3. Remove ten screws securing top cover. Remove top cover.
4. Disconnect disk drive cable from disk drive.
5. Remove two screws securing disk drive to power supply. Remove disk drive by sliding assembly out front panel of instrument.
6. Remove two retaining pins securing power supply to chassis. Slide power supply out far enough to gain unobstructed access to power supply cables.
7. Disconnect power supply line input and DC output cables. Remove power supply.
8. Slide new power supply in far enough to connect line input cable and DC output cable. Connect cables and slide power supply in completely. Secure power supply using two retaining pins.
9. Slide disk drive through front panel of instrument. Secure disk drive to power supply using two screws.
10. Connect disk drive cable to disk drive.
11. Install top cover. Secure top cover to chassis using ten screws.

Note

To ensure top cover is properly installed, secure side screws of top cover before securing top screws.

Removal and Replacement of Fan

1. Disconnect pod cables from rear of instrument.
2. Disconnect power cable.
3. Remove ten screws securing top cover. Remove top cover.
4. Disconnect fan cable and BNC trigger cables from system board.
5. Disconnect AC power supply cable from power supply.
6. Remove two hex standoffs securing HP-IB cable to rear panel.
7. Remove eight screws securing rear panel. Remove rear panel.

Note

An ESD spring ground is inserted on the RS-232 connector. This spring ground is not secured and can easily fall off.

8. Detach fan from rear panel by removing four screws securing fan to rear panel.
9. Disconnect fan cable from old fan and connect to new fan.

10. Align new fan on back panel with fan cable adjacent to line filter assembly and label toward rear (fan rotor is facing forward).
11. Align fan guard on back of panel.
12. Attach fan to rear panel with four machine screws.
13. Re-assemble instrument in reverse order of above.
14. Install top cover. Secure top cover to chassis using ten screws.

Note To ensure top cover is properly installed, secure side screws of top cover before securing top screws.

Removal and Replacement of Keyboard Assembly

1. Disconnect pod cables from rear of instrument.
2. Disconnect power cable.
3. Remove ten screws securing top cover. Remove top cover.
4. Disconnect disk drive cable from disk drive.
5. Remove two screws securing disk drive to power supply. Remove disk drive by sliding assembly out front panel of instrument.
6. Remove two retaining pins securing power supply to chassis. Slide power supply out far enough to gain unobstructed access to power supply cables.
7. Disconnect power supply line input and DC output cables. Remove power supply.
8. Disconnect keyboard cable from system board.
9. Remove four screws securing keyboard assembly to chassis (located on inside of instrument).
10. Remove keyboard assembly.
11. Disconnect RPG cable from keyboard circuit board assembly. Keyboard assembly can now be disassembled.
12. Reinstall keyboard assembly by reversing this procedure.
13. Install top cover. Secure top cover to chassis using ten screws.

Note To ensure top cover is properly installed, secure side screws of top cover before securing top screws.

Self Tests

The extended self tests are used for isolating problems in the logic analyzer. The tests are loaded from the operating disk.

Caution

The process of running the self test DESTROYS the current configuration and data. Please use a master disk (or copy) in the disk drive to run the tests.

The self tests are invoked from any menu by pressing the front-panel I/O key The pop-up I/O menu appears on screen with the following choices:

- Done
- Print Screen
- Print All
- Disk Operations
- RS-232-C Configuration
- BNC
- Self Tests

1. Use the front-panel knob to move the cursor to Self Tests and SELECT.
2. Insert operating disk (or copy) into disk drive.
3. Move cursor to **Start Self Test** with front-panel knob and SELECT. A message appears on-screen indicating the logic analyzer is loading the test system file and then the menu is displayed.
4. To leave the self test menu, move cursor to **Done** and SELECT.

Note

Operating disk (or copy) must be in disk drive for reloading after self tests.

Data Acquisition Self Test

The data aquisition self test verifies the functionality of key elements of the internal acquisition system.

1. In **HP 1650B/51B Self Tests** menu, move cursor to **Data Acquisition** and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

RS-232-C Self Test

The RS-232-C self test verifies the functionality of the RS-232-C driver and continuity of the RS-232-C data paths. Connect the RS-232-C loopback connector to the rear-panel RS-232-C port before beginning this test.

1. In **HP 1650B/51B Self Tests** menu, move cursor to RS-232-C and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

BNC Self Test

The BNC self test verifies the functionality of the internal BNC trigger circuitry1. In HP 1650B/51B Self Tests menu, move cursor to RS-232-C and SELECT

1. In **HP 1650B/51B Self Tests** menu, move cursor to **BNC** and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

Keyboard Self Test

The keyboard self test verifies the key closures and and knob operation on the front panel system.

1. In **HP 1650B/51B Self Test**s menu, move cursor to **Keyboard** and SELECT.
2. Move cursor to **Execute** and SELECT.
3. Press all keys on front panel and rotate knob to verify proper operation.
4. Press STOP twice to return to **Keyboard Self Test**.
5. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

RAM Self Test

The RAM self test verifies the operation of system RAM and display RAM.

1. In **HP 1650B/51B Self Tests** menu, move cursor to **RAM** and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

ROM Self Test

The ROM self test verifies the operation of the system ROM.

1. In **HP 1650B/51B Self Tests** menu, move cursor to **ROM** and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Done** and SELECT.

Disk Drive Self Test

The disk drive self test verifies the functionality of key elements of the internal disk system.

1. In **HP 1650B/51B Self Tests** menu, move cursor to **Disk Drive** and SELECT.
2. Move cursor to **Single test** or **Repetitive test** and SELECT.
3. If running repetitive test press and hold STOP to end test. The number of runs and failures are displayed in the menu.
4. To return to **HP 1650B/51B Self Tests** menu, move cursor to **Don**e and SELECT.

Cycle Through Tests

The following tests are run consecutively and continually until STOP is pressed:

- Data Acquisition
- RAM
- ROM
- Disk Drive

To see reults of continuous tests, move cursor to one of the four tests listed on the menu and SELECT. The number of runs and failures are displayed for that test. To return to **HP 1650B/51B Self Tests**, press SELECT.

Auxiliary Power

The + 5 volts auxiliary power to the logic analyzer pods is protected by a current limiting circuit on the System Assembly Board. If current on pins 1 and 39 of the logic analyzer pods exceeds 2.3 amps, the current limiting circuit opens. After the path causing the excessive current is opened, the circuit resets in approximately 20 ms. If a problem is suspected with this circuit, remove all loads from the pods and measure for + 5 volts at either pin 1 or 39 of the pod.