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Operation, Maintenance and Service Manual

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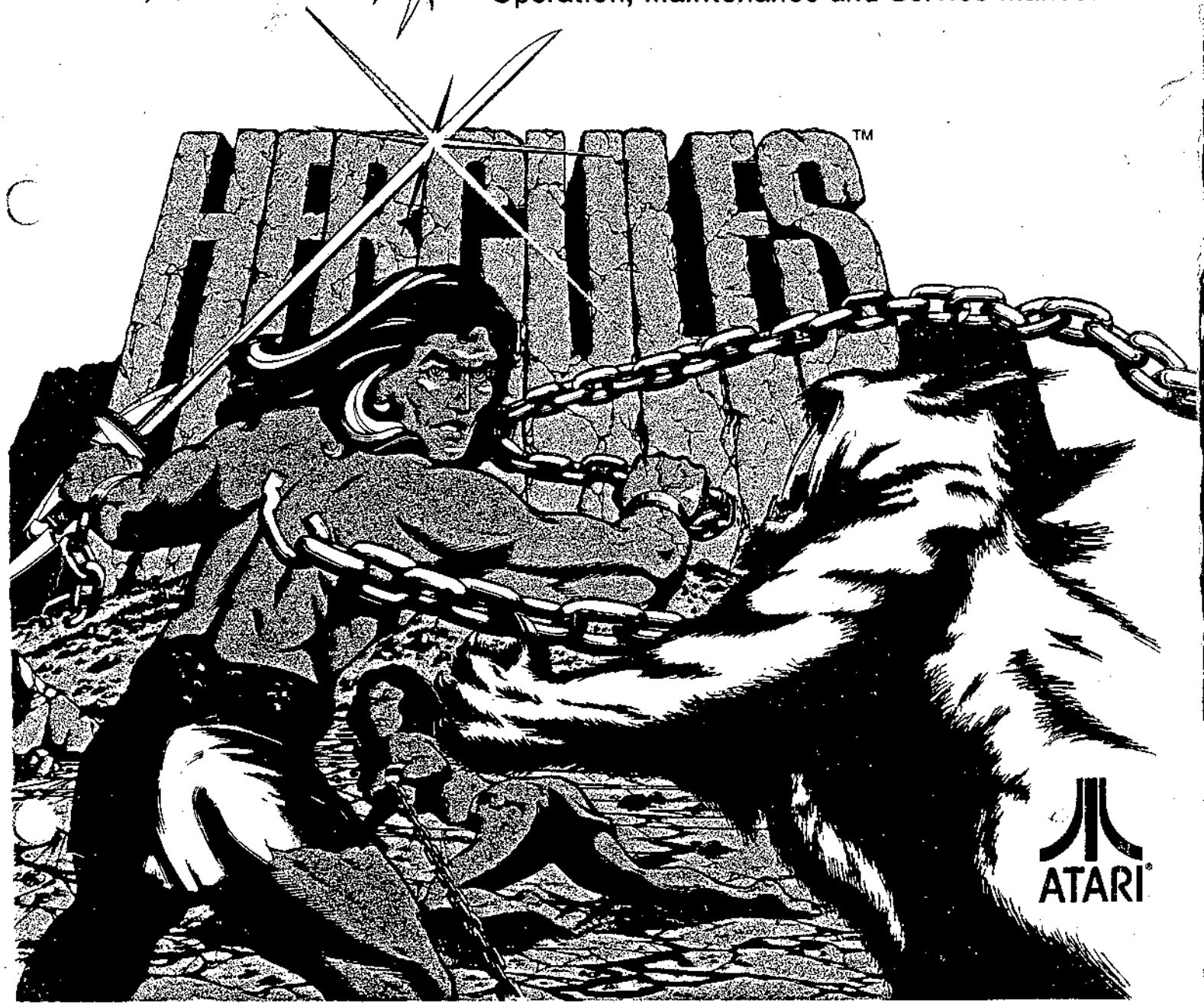

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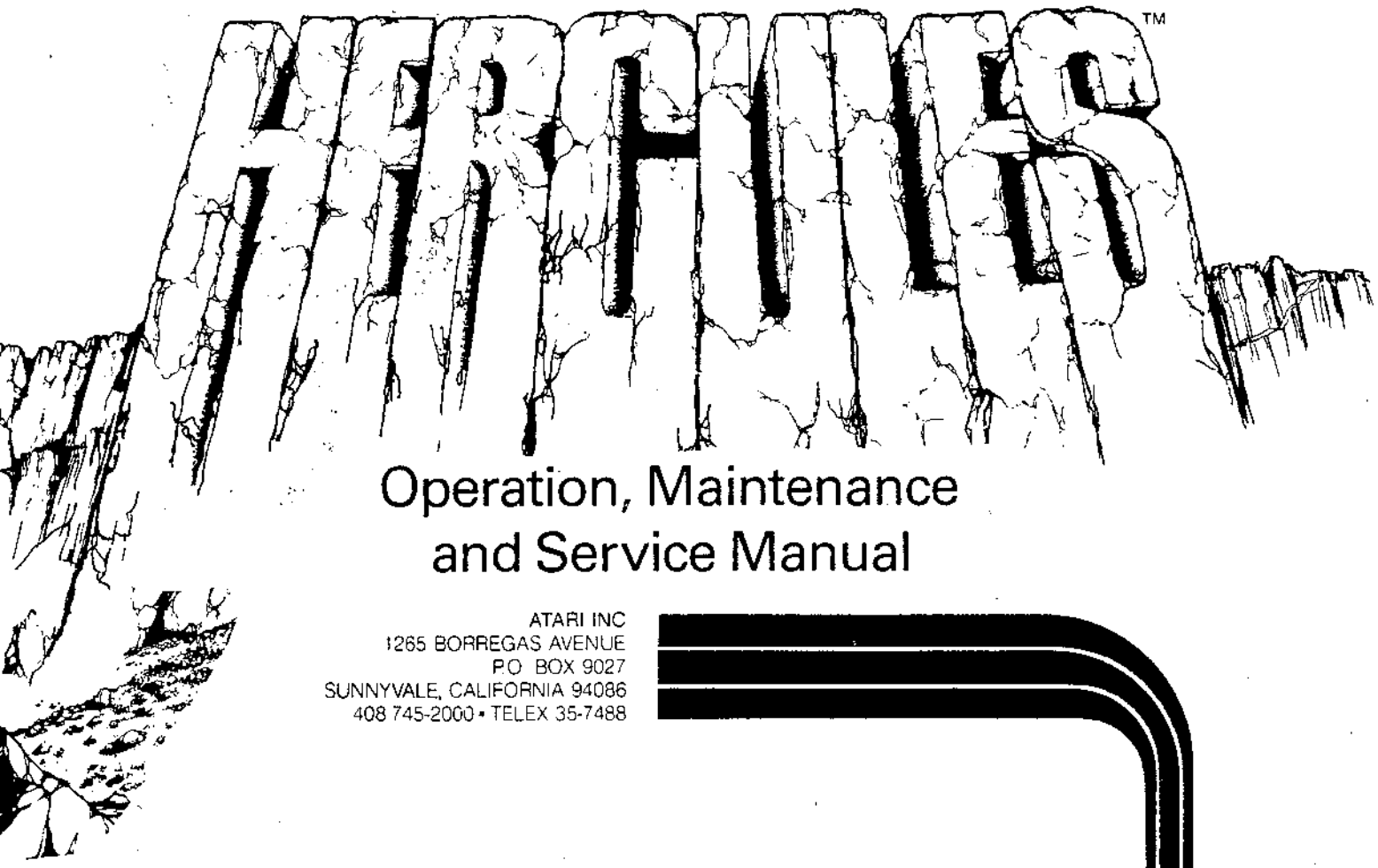

Operation, Maintenance and Service Manual

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NOTE

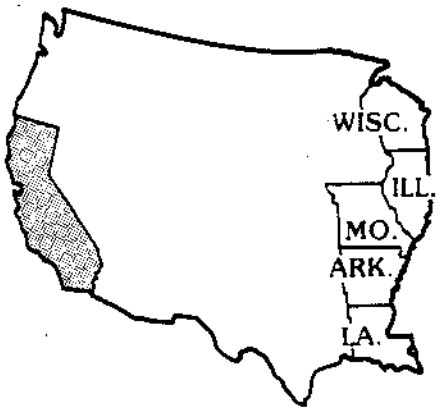
If reading through this manual does not lead to solving a specific maintenance problem, you can call Tele-Help™ at the following two Atari Customer Service offices.

WEST and CENTRAL U.S.A.

Atari Coin-Op Customer Service
1344 Bordeaux Drive, Sunnyvale, CA 94086
Telex 17-1103
(Monday - Friday, 7:30 - 4:00 pm Pacific Time)

From California, Alaska or Hawaii, dial (408) 745-2900

From anywhere else in this area, dial toll-free (800) 538-1611

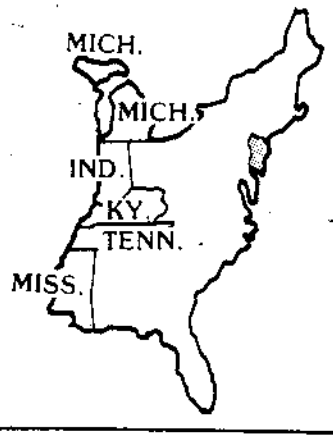


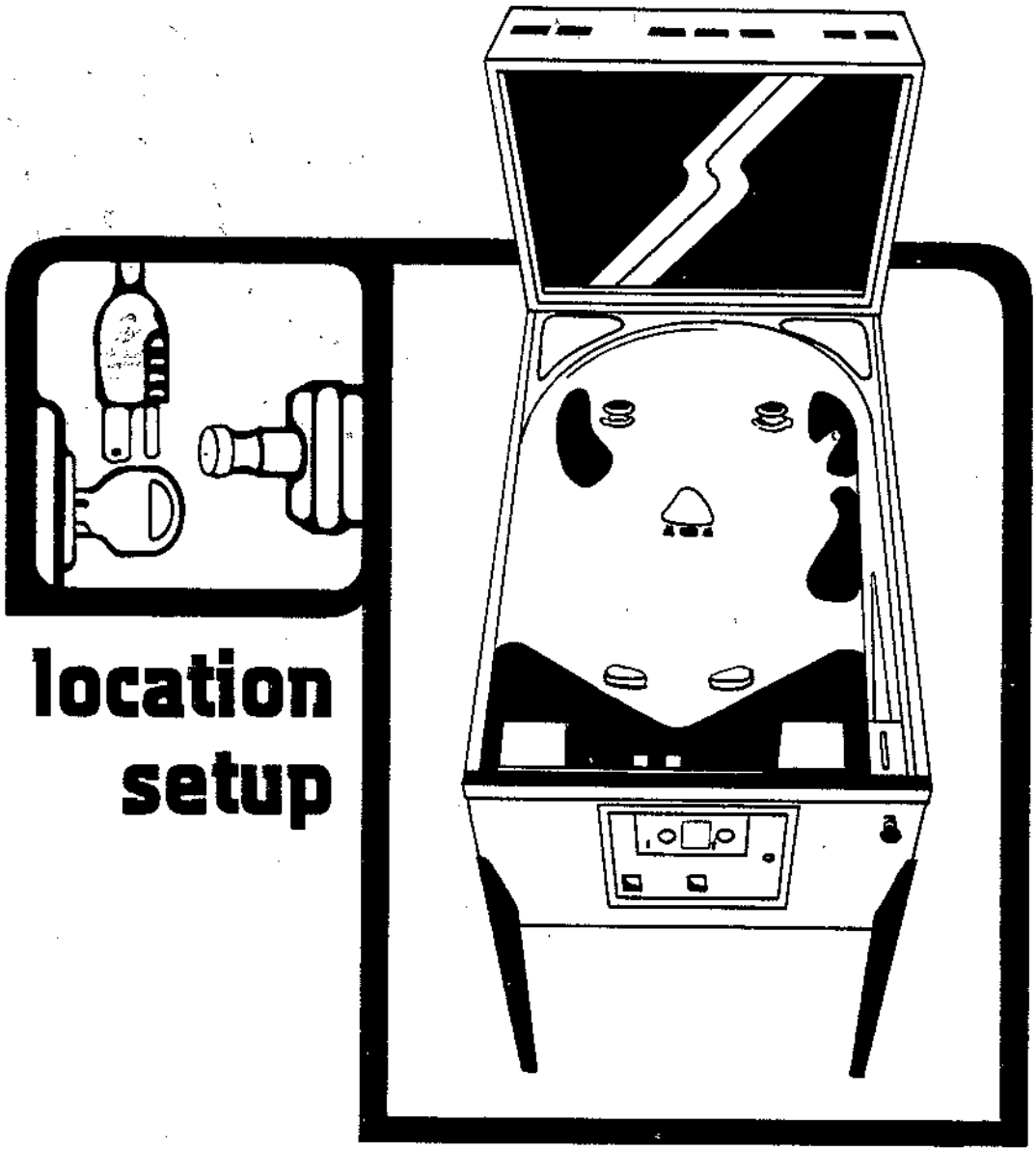
EAST U.S.A.

Atari Inc.
New Jersey Customer Service Office
44 Colonial Drive, Piscataway, NJ 08854
Telex 37-9347
(Monday - Friday, 8:30 - 5:00 pm Eastern time)

From New Jersey dial (201) 981-0490

From anywhere else in this area, dial toll-free (800) 631-5374





location setup

a. inventory of parts from shipping cartons

Due to its physical dimensions, this game is shipped in two separate cartons. Figure 1-1 illustrates and lists the game pieces as they are unpacked from the two cartons. Again, due to its sheer size, Atari recommends that the game be assembled at its installation site, rather than pre-assembling and then trucking to the final site as is done routinely with smaller games.

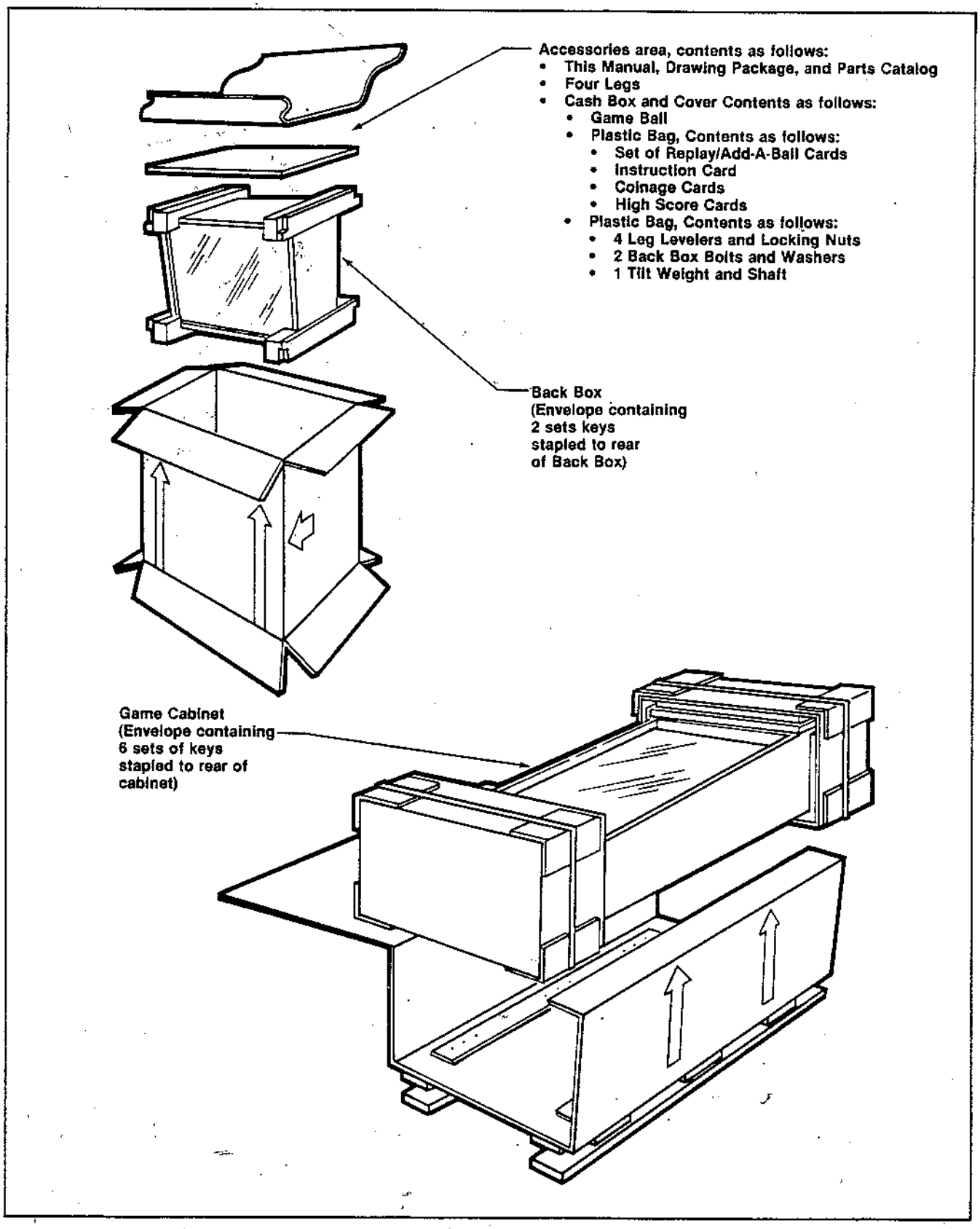


Figure 1-1 Inventory of Parts from Shipping Container

NOTE

Care should be taken while handling the cabinet to prevent twisting it.

b. assembly of game

1. Attach Legs

See Figure 1-2 below, and attach the four legs to the cabinet. Lift the cabinet carefully. Avoid applying any twisting force.

2. Secure Back Box

See Figure 1-2 below, and secure the back box to the cabinet.

3. Remainder of Assembly

Follow the instructions illustrated in Figure 1-2 to complete the assembly of the major game systems and parts.

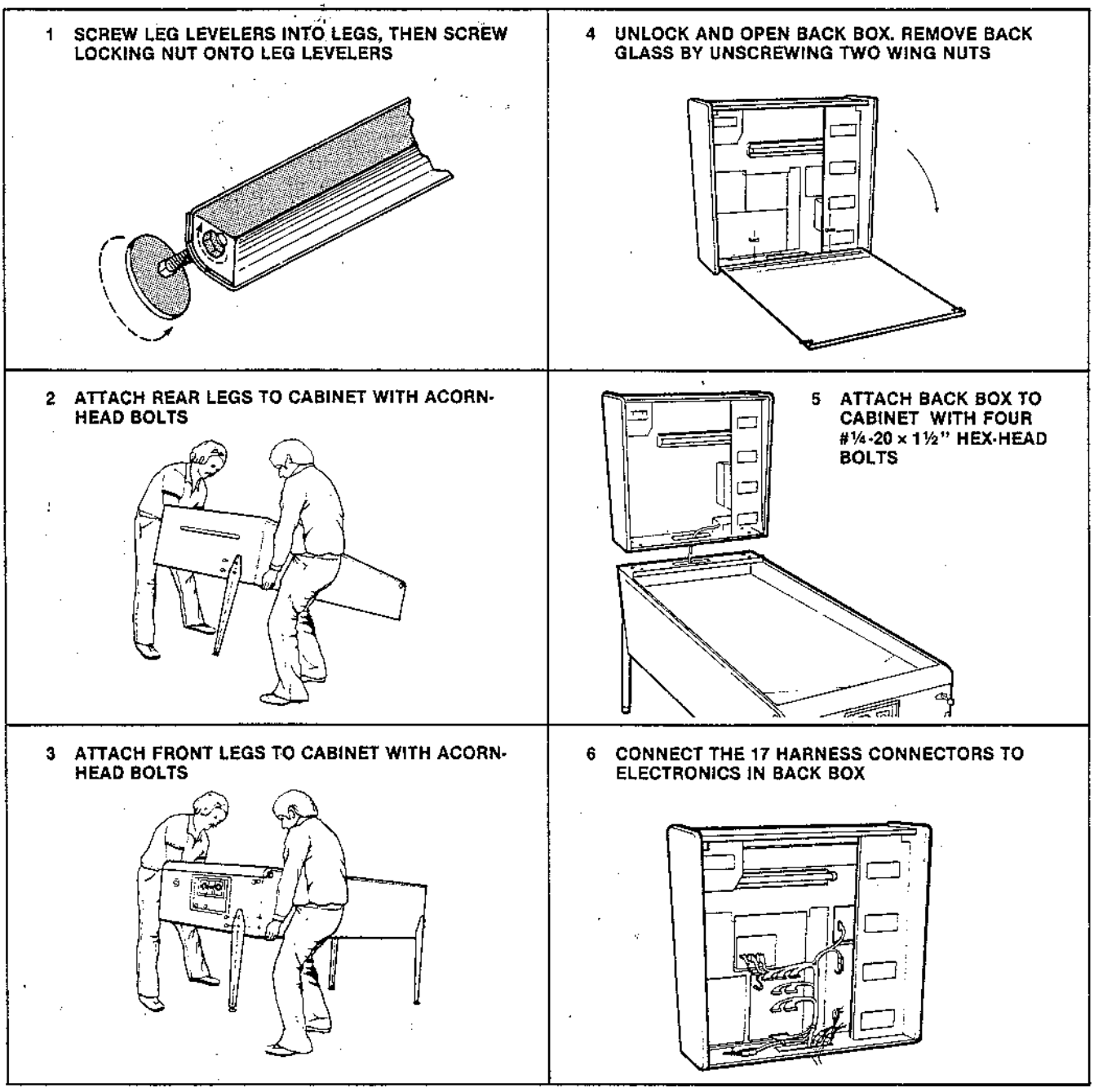


Figure 1-2 Game Assembly

4. Final Assembly of Game

See Figure 1-3, below, for the final assembly of the game.

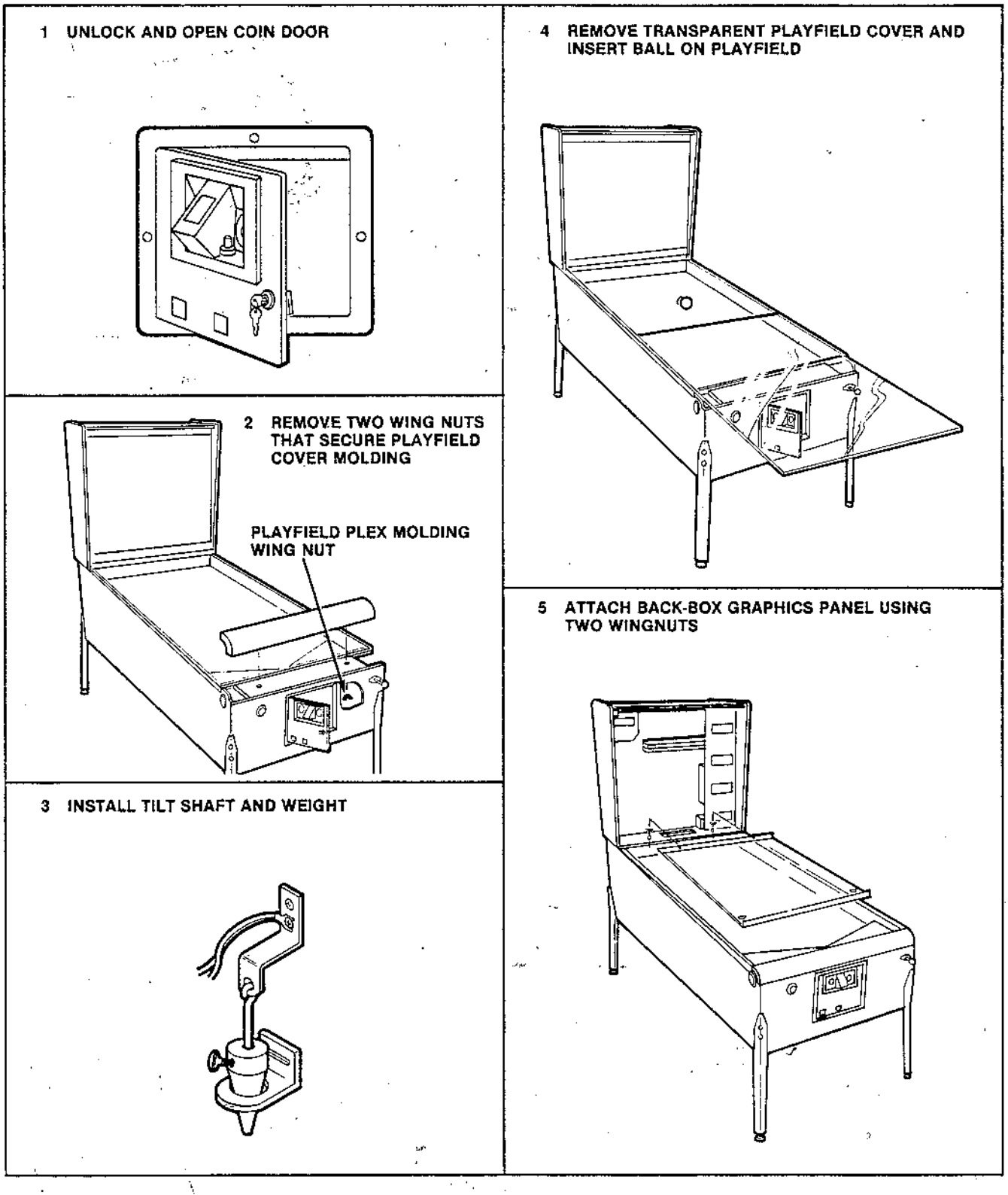


Figure 1-3 Final Assembly of Game

c. game checkout

We strongly advise you to thoroughly check the game *before applying power*. If you have never seen Atari's new generation pinball games, this is an excellent time to familiarize yourself with this new game.

1. Check Back Box

The Back Box contains all of the game's electronics; therefore this is a critical area for you to check. See Figure 1-4 below for a list of items you should check in the Back Box.

2. Check Cabinet

Since this game has all of its electronics in the Back Box, there isn't much left in the bottom of the cabinet. However, you should check that the parts installed on the bottom of the playfield and items such as the incandescent lamp, game lampsockets, and the various electro-mechanical parts have not been jarred loose in shipment. These are accessible through the "bomb bay" doors in the bottom of the cabinet. To open the bomb bay, unlock all four locks.

3. Check Playfield

Give the top surface of the playfield a careful visual check, too. Look for anything that may have come loose during the game's shipment to you.

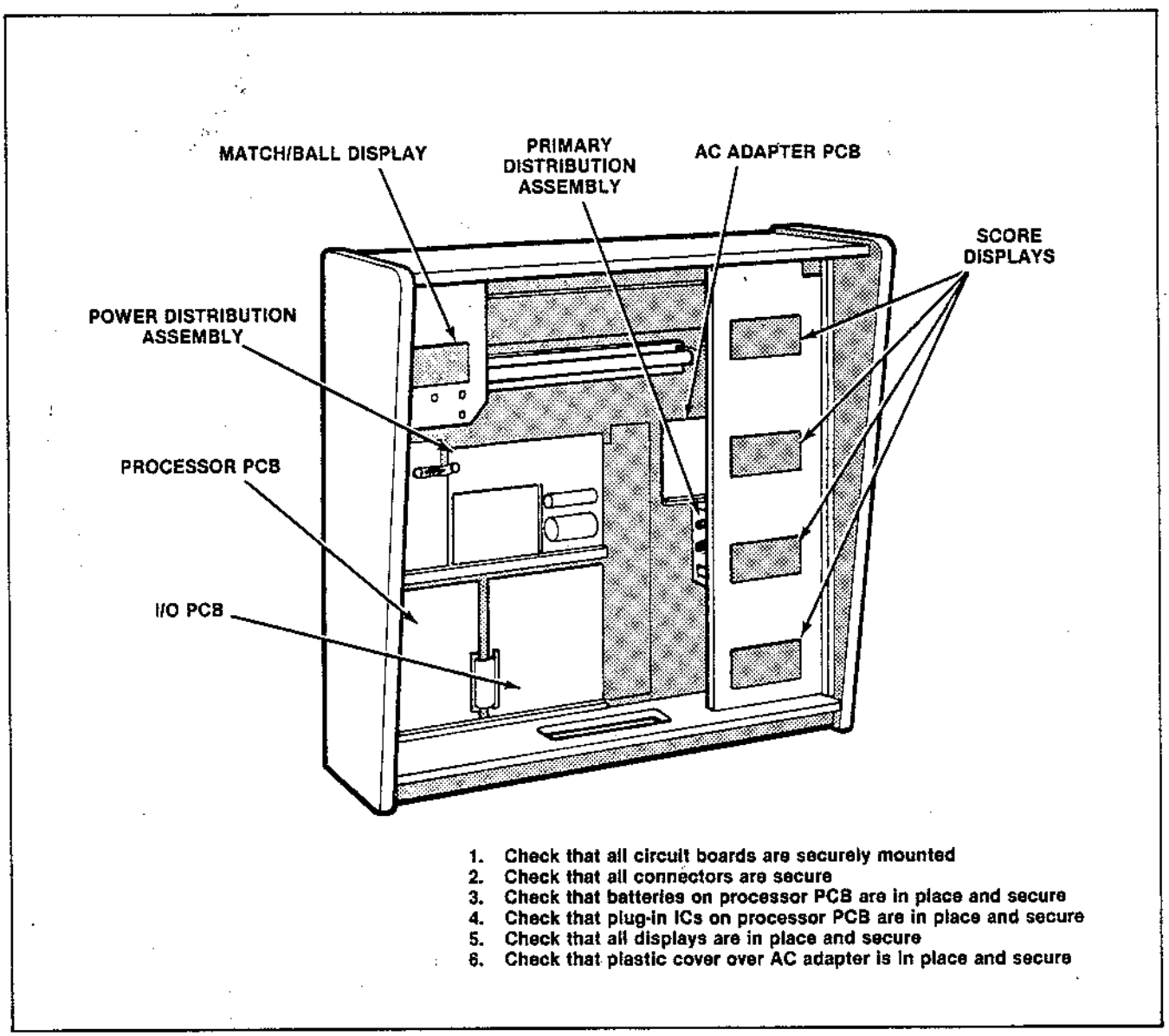


Figure 1-4 Checking the Back Box

d. perform self-test

Table 1-1 is an exact duplicate of the Self-Test Label located inside the coin door on the Coin Box Cover. See Table 1-2 for an explanation of each Test step.

Table 1-1 Self-Test Label

TEST NO.	TEST NAME	TEST DESCRIPTION
		Press Self-Test Switch on inside top of Coin Door.
	RAM/ROM Test	If test passes, Self-Test automatically advances to Test No. 1, Display Test. If test fails, Test does not advance to Test No. 1. If it fails, see instructions at top of Option Switch Settings label inside Back Box.
1	Display Test	All displays cycle through numerals 0 thru 9, blank for six beats, then cycle again. To stop cycling (and start again), press START.
2	Solenoid Test	Match/Ball display indicates Test No. 2. Solenoids activate one at a time while solenoid identification number is displayed in Credit display. To change to next solenoid, press START. See Solenoid Identification label on inside left front of cabinet.
3	Lamp and Switch Test	Match/Ball display indicates Test No. 3. All Playfield and Back Box Lamps are lighted. All microcomputer controlled lamps may be turned off (and on again) by pressing START. Any stuck or activated switches are identified by a switch identification number in the CREDIT display and a tone emitted from the game speaker. See Switch Identification label on inside left front of cabinet.
4	Sequential Lamp Test	One Lamp at a time is sequentially lighted for about 1 second each.
		ACCOUNTING
5	Credits	Present number of credits is displayed in player 1 Score display.
6	Left Coin Count	Left coin switch total count is displayed in player 1 Score display.
7	Right Coin Count	Right coin switch total count is displayed in player 1 Score display.
8	Total Coin Count	Total of Tests 6 and 7 is displayed in player 1 Score display.
9	Total Plays	Total number of plays is displayed in player 1 Score display.
10	Total Replays	Total number of Replays is displayed in player 1 Score display.
11	Game Timer	Total time (minutes) of game play is displayed in player 1 Score display.
12	Specials Awarded	Total number of awarded Specials is displayed in player 1 Score display.
13	Extra Balls Awarded	Total number of awarded Extra Balls is displayed in player 1 Score display.
14	Tilts	Total number of Tilts is displayed in player 1 Score display.
15	Battery Backup Errors	Total number of Battery Backup Errors is displayed in player 1 Score display.
16	Replay Level	*Replay Level is displayed in player 1 Score display. } Replay Levels may be set in any order. To eliminate Replay Level(s), set level(s) to zero.
17	Replay Level	*Replay Level is displayed in player 1 Score display.
18	Replay Level	*Replay Level is displayed in player 1 Score display.
19	High Score to Date	*High Score to Date is displayed in player 1 Score display.

*To change, zero score number by activating right coin switch. Press START to increment Score by steps of 5000 as indicated in player 1 Score display.

Table 1-2 Defining Self-Test

TEST	TEST NAME	DEFINITION
	RAM/ROM Test	If this test fails, the test will not advance to the Display Test. To determine the failing device, check the lighting of LEDs L1 thru L4 on the Processor PCB. If L1 is ON and L2 is ON—indicates failure of RAM H6 or L3 is ON—indicates failure of RAM K6 or L4 is ON—indicates failure of RAM J6 If L1 is OFF and L2 is ON—indicates failure of ROM K/L7 or PROMs E5 and J5 or L3 is ON—indicates failure of ROM M7 or PROMs D5 and K5 or L4 is ON—indicates failure of ROM J7 or PROMs F5 and H5

WARNING

A RAM/ROM test failure indicates a defective game. Continuing the test procedure may result in damaging the game. However, if you would like to continue to the next tests in such a situation, press TEST and START switches simultaneously and hold for at least a second.

Table 1-2 Defining Self-Test (continued)

TEST	TEST NAME	DEFINITION
1	Display Test	All displays cycle through numerals 0 thru 9, blank for six beats, then cycle again. While cycling, make sure the segments are lighting and blanking properly.
2	Solenoid Test	All solenoids and relays are actuated in this test. The test begins by energizing the Outhole Kicker about once a second until you press START or press the SELF-TEST pushbutton. Each time you press START, the test advances to energize the next solenoid. Each solenoid and relay is identified by a number in the Credit display. To identify displayed solenoid number, open the coin door and refer to the Switch and Solenoid Identification label on the left front wall of the cabinet.
3	Lamp and Switch Test	All microcomputer-controlled lamps are lighted for you to accurately check for burned-out bulbs. To turn the lights off and on, press START. Any stuck or activated switches are identified by a flashing number in the Credit display and an "oink" tone is emitted from the game speaker. To identify the displayed switch number, open the coin door and refer to the Switch and Solenoid Identification label on the left front wall of the cabinet.
4	Sequential Lamp Test	This test is specifically designed for Atari's Pinball Tester. See your distributor for availability of this tester.
The following is an explanation of each Accounting step:		
5	Credits	Present number of credits accepted.
6	Left Coin Count	Total number of coins accepted by left coin chute.
7	Right Coin Count	Total number of coins accepted by right coin chute.
8	Total Coin Count	Total number of coins accepted.
9	Total Plays	Total number of games played.
10	Total Replays	Total number of replays awarded by game (to include replays earned by matching, add 10% of Total Plays to this figure. Match replays are not recorded by the microcomputer.)
11	Game Timer	Total number of minutes game has been in play mode.
12	Specials Awarded	Total number of Specials awarded by game.
13	Extra Balls Awarded	Total number of Extra Balls awarded by game.
14	Tilts	Total number of tilts experienced by game.
15	Battery Backup Errors	This is a random number. Record it for future reference. If the number changes from previous reading, a battery backup error was experienced.
16 17 18	Replay Level Replay Level Replay Level	You may set three, two, one or no replay levels. To zero, activate right coin switch. Replay levels are set in increments of 5000 with the start button. Each zero setting eliminates that replay level.
19	High Score to Date	This represents either the highest score achieved on this game or a score you set to challenge the players. To zero, activate right coin switch. Score is set in increments of 5000 by pressing the START button. Score can be completely eliminated by setting option switch SWC, toggle 8, to OFF. Suggested setting of High Score is about double the first replay level.

e. setting the option switches

1. Definition of Game Option Switch Settings

Atari pinball games now have thirty-two option switches that can be set by the operator. Our field testing has shown that the factory-preset option settings will maximize the profits possible with the game. If you wish to change some of these settings, see Table 1-3 for a definition of each option.

2. Set the Options

Figure 1-5 below duplicates the Option Switch Settings Label located in the game's Back Box. Please note that the switch settings marked with the $ symbol and the switch toggles shaded on the drawing indicate how the game was set before shipment from Atari.

The factory-set options are as follows:

a. Number of Balls: Three
b. FREE PLAY feature: Off
c. MATCH: On
d. SPECIAL awards player: One replay (credit)
e. EXTRA BALL gives player: One extra ball
f. 2 Coins/1 Credit
g. High-Score-to-Date MILLION LIMIT: *ALWAYS LEAVE THIS SWITCH ON*
h. HI-SCORE-TO-DATE FEATURE: On
i. Exceeding HIGH-SCORE-TO-DATE awards player: Two free games (credits)
j. Maximum Credits: 10
k. Memory Feature: On

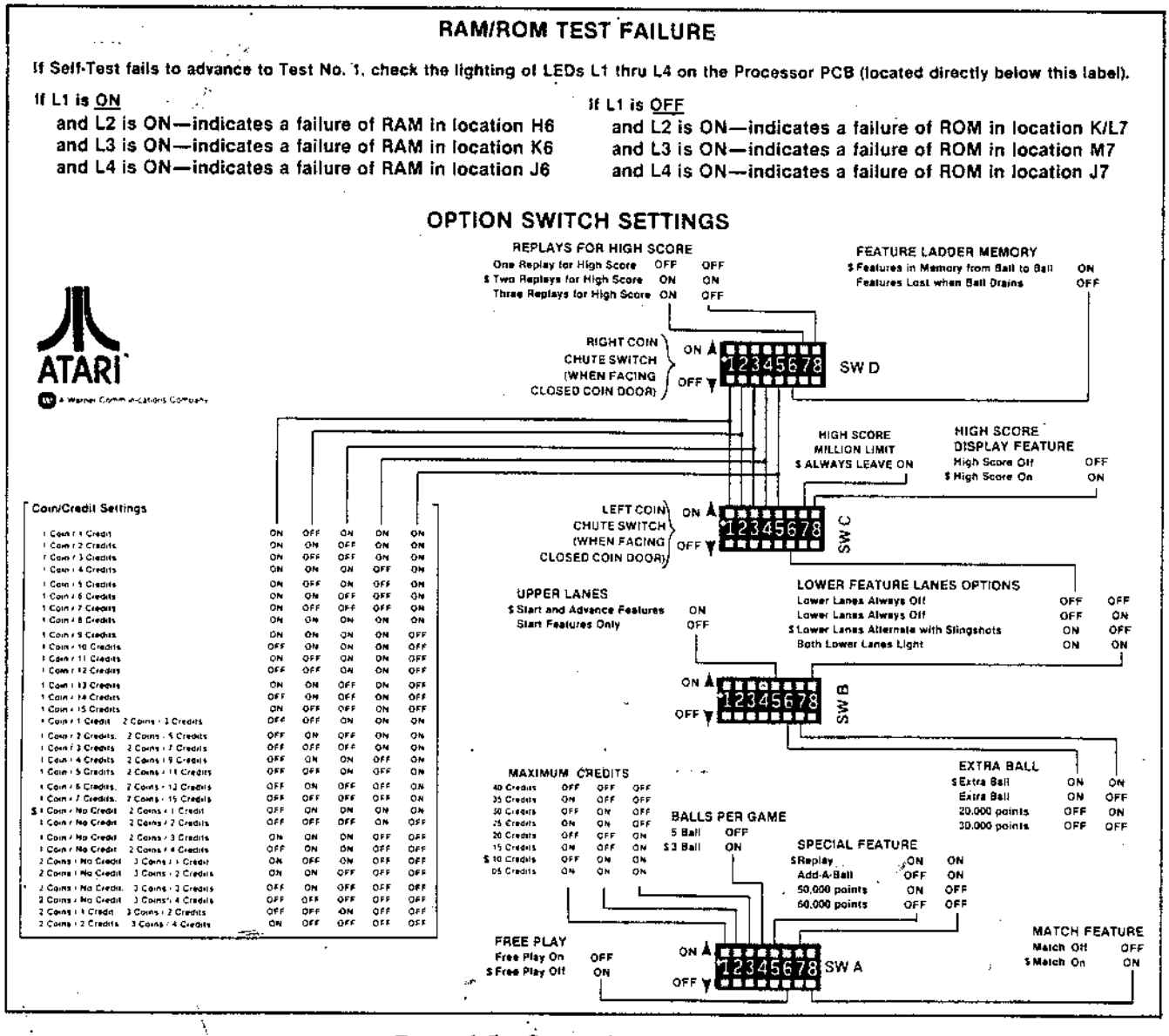


Figure 1-5 Option Switch Settings

Table 1-3 Definition of Game Options

OPTION	AS SHIPPED	DEFINITION
Coin/Credit Settings	2 coins/credit.	There are 32 settings for the number of coins required to play the game. The setting of the right and left coin mechanisms are completely independent.
Maximum Credits	10 Credits	Controls maximum credits that the credit accumulator will hold. Adjustable from 5 to 40 credits. Once the accumulator reaches the maximum credit setting, coins are rejected from the coin mechanism.
Free Play	Free Play Off	With the free play feature ON, the game will always indicate 1 credit in the credit accumulator, and no coins are necessary to play the game. With free play OFF, game can only be played if the proper number of coins are inserted.
Special Features	Awards Replay	The two special feature switches may be set to award a replay, additional points, or an extra ball.
Match Feature	Feature ON	With the match feature ON, when the last ball of the last player drops into the outhole, a random number is displayed on the Match/Ball display. If the number matches the last two digits of any player's score, one replay is awarded for each score that is matched.
High Score Feature	Feature ON	The operator may set High Score in increments of 5000 points. If a player's score reaches the high score, 1, 2, or 3 credits or Add-A-Ball will be awarded (depending on the high score award setting or the SPECIAL FEATURE setting). If this feature is turned off, there will be no high score displayed.
High Score Replays	2 Replays	This is the award setting for the High Score feature. May be set for 1, 2, or 3 credits.
Feature Ladder Memory	Memory ON	If ON, keeps memory of features advanced from ball to ball. If OFF, means all feature advances are lost as each ball drains.
Lower Lane Features	Lanes Alternate (with Slingshots)	When features have been advanced to fill ladder, the lower lanes may be lit alternately, always, or never, depending on the setting of this option.
High Score Million Limit	Limit ON	Prevents High Score from exceeding 999,999. ALWAYS LEAVE THIS OPTION ON.
Upper Lanes	Start and Advance	This option allows setting of the upper lanes so that the passage of the ball will either start or start and ADVANCE the features.
Extra Ball	Extra Ball ON	An extra ball is awarded if the ball activates the extra ball drain rollover when that lane's extra ball light is ON. The extra ball award may be set for 20,000 or 30,000 points instead of an extra ball. The extra ball feature is also awarded by passage of the ball completely through the Path of Victory.
Balls/Game	3 Balls/Game	Game may be set for either 3 or 5 balls.

3. Electronic Percentaging

Percentaging of the game (by adjusting the option switches as shown in Table 1-4) should only be done after the game has been introduced at a location. Percentaging of the game as shipped from Atari is best for initial player appeal. Settings of the percentaging options are shown below for the 3-ball (as shipped) and 5-ball settings recommended by Atari. These are followed by settings you can use at your location to make the game more conservative or liberal if desired.

Table 1-4 Option Switch Percentaging

3-Ball Game (As Shipped)

- Feature ladder memory maintained from ball to ball.
- Upper lane rollover starts and also advances each feature.
- Lower lane lights set to alternate from side to side whenever a lower slingshot is activated by the ball.

5-Ball Game (Recommended Settings)

- Feature ladder memory forgets features advanced (but not collected) when ball drains.
- Upper lane rollover starts and also advances each feature.
- Lower lane lights are turned off at all times.

5-Ball Game (Liberal Settings)

- Feature ladder memory maintained from ball to ball.
- Upper lane rollover starts and also advances each feature.
- Lower lane lights are lit any time feature ladder is fully advanced.

5-Ball Game (Conservative Settings)

- Feature ladder memory forgets features advanced (but not collected) when ball drains.
- Upper lane rollover starts, but does not advance each feature.
- Lower lane lights are off at all times.

3-Ball Game (Liberal Settings)

- Feature ladder memory maintained from ball to ball.
- Upper lane rollover starts and also advances each feature.
- Lower lane lights are on any time feature ladder is fully advanced.

3-Ball Game (Conservative Settings)

- Feature ladder memory forgets features advanced (but not collected) when ball drains.
- Upper lane rollover starts, but does not advance each feature.
- Lower lane lights are off or alternate from side to side whenever a lower slingshot is activated by the ball.

f. final checkout of game

1. Check Power-Down Coin Rejection

With the power to the game turned off, insert coins into the game. These should be rejected into the coin return in the coin door.

2. Check Coin Acceptance

With the power switch on and the coin door closed, insert coins into the game. The coins should be accepted and should enter the cash box.

3. Check Operation of Mechanical Coin Counters

Open the Coin Door and insert coins into game. The mechanical coin counters should trip for each coin that is accepted.

g. insert player instruction cards

A plastic bag of instruction, coinage, and replay level cards was shipped with your game. The instruction card should be inserted in the right-hand side of the lower arch. The only difference between the front and back of this card is the advancement or non-advancement of the Double Bonus, Extra Ball, and Special features. Select the appropriate side of the card according to the setting of option switch SWB toggle 5.

Place the coinage card over the bottom of the instruction card. Then slip the pair of cards into the right card holder on the lower arch.

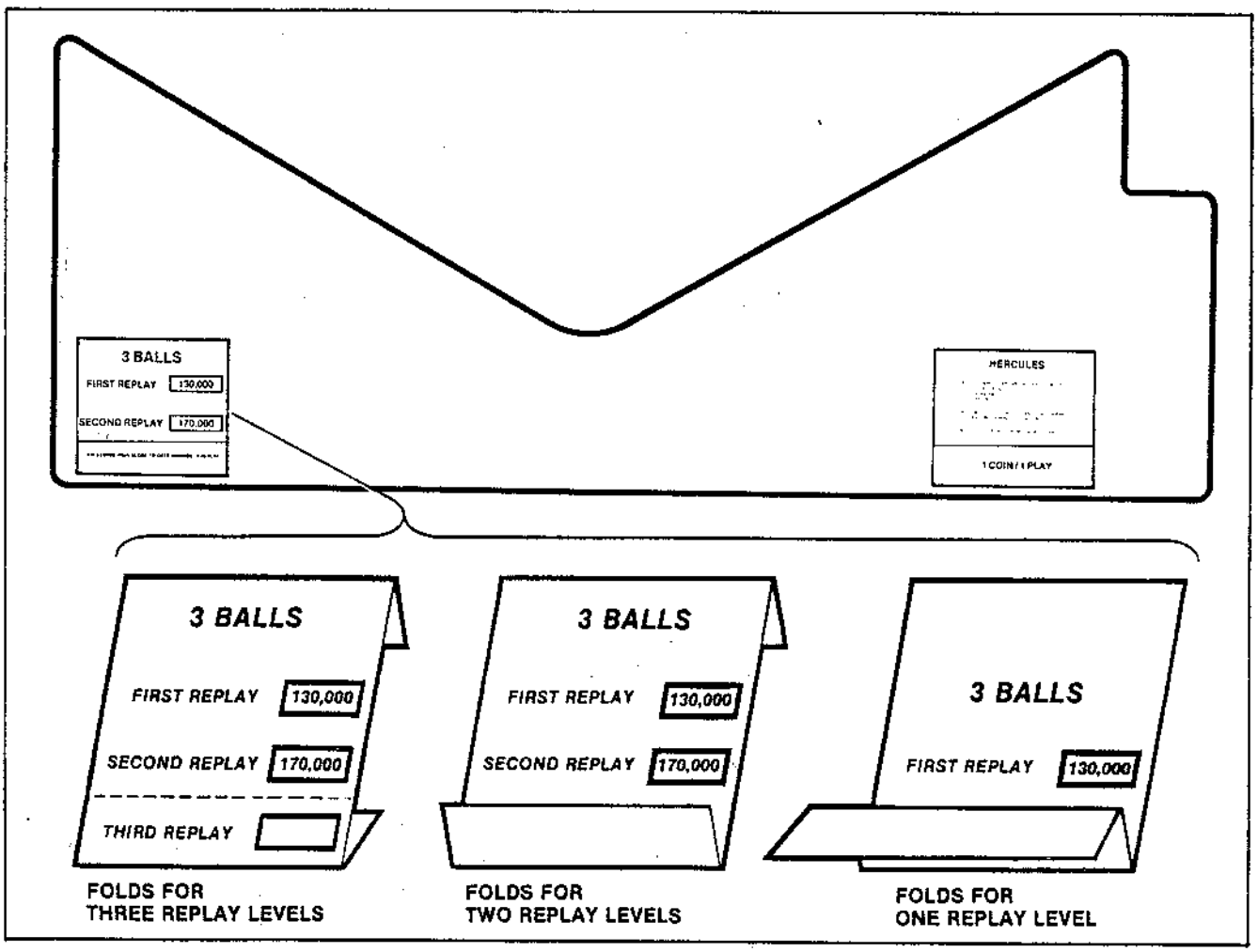


Figure 1-6 Folding and Displaying Player Instruction Cards

There are twelve replay level cards shipped with the game. The suggested card for the 3-ball game is part number 021227-03, and for 5-ball game is part number 021227-09. These cards must be folded and slipped into the left card holder on the lower arch. On one side of the replay level cards is the message "3 BALLS", and the various replay scores. See Figure 1-5 and fold the card to display the proper replay levels; insert it as shown.

Place the High-Score-To-Date card over the bottom of the replay level card. Then slip the pair of cards into the left card holder on the lower arch.

h. final location assembly and inspection

WARNING

Hazard of unisolated line voltage electric shock. Do not contact the flipper switches, thumper bumpers, or AC Adapter PCB with power applied to the game.

Before applying power to the game, thoroughly inspect it to make sure that nothing came loose while setting it up. If it was transported by you from a remote set-up point to the installation site, re-perform the self-test, activating each playfield switch during test step #3 to make sure that the switches are properly adjusted.

1. Adjust the tilt weight.
2. Install the playfield's transparent plastic shield.

—THE GAME IS NOW READY TO BEGIN EARNING YOU MONEY—

i. about the battery-powered memory

This game includes a battery-powered computer memory (battery-backed RAM) that remembers the game's accounting information, operator selectable Replay Levels, and the High Score to Date. Even when the AC power to the game is removed, this information is retained in this memory.

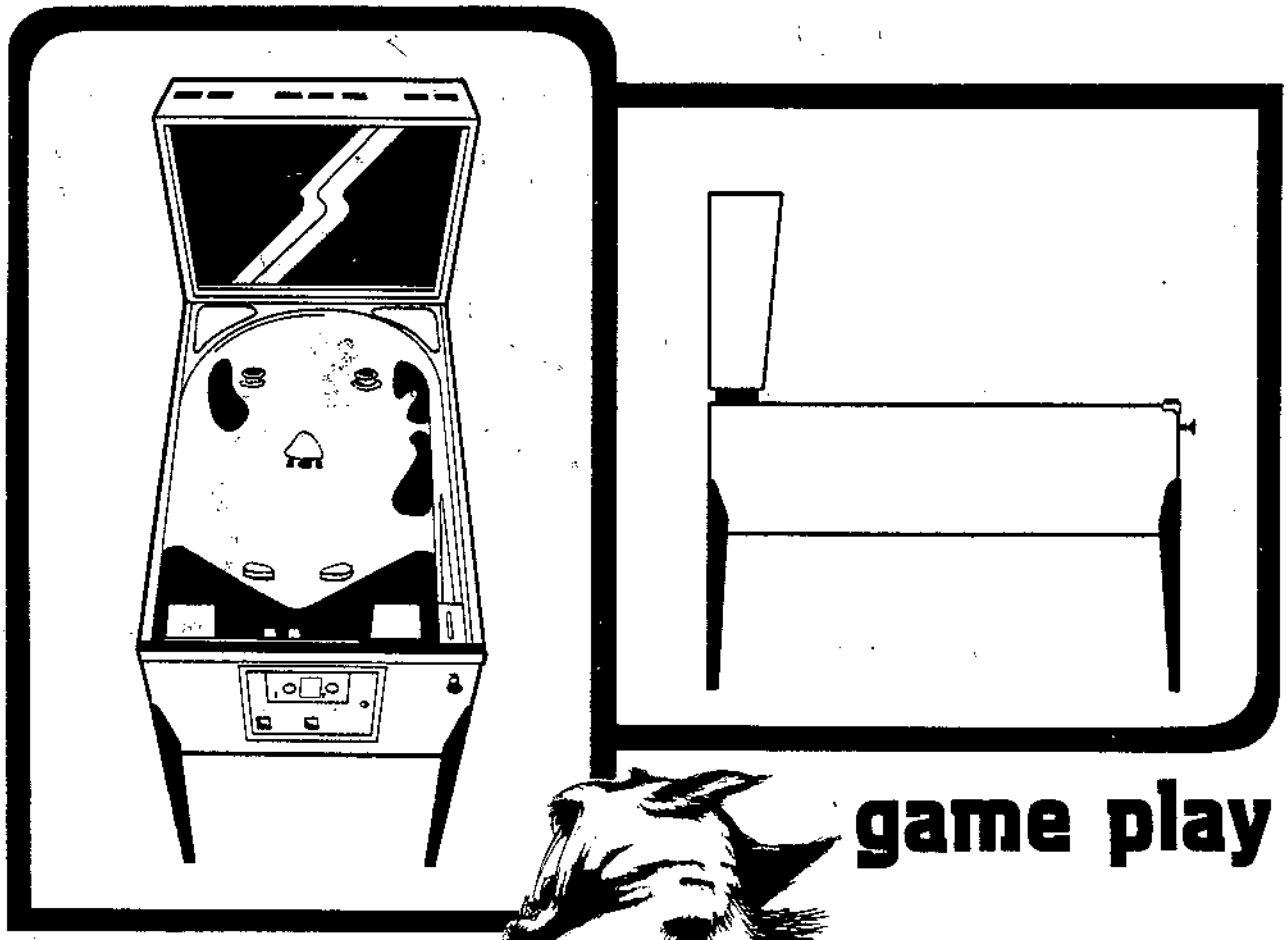
The game's microcomputer continually checks the Replay Levels and High Score to Date. If, by some error of the microcomputer, one of these scores is "blitzed", the microcomputer will reset the erroneous score to zero. Therefore, the Replay Level (or High Score to Date) in error is totally eliminated. This feature protects the operator from players getting unwarranted free games due to a failure of the microcomputer.

Test number 15 of the Self-Test Procedure is named Battery Backup Error. In this test, a totally random number is displayed in the Player 1 Score Display. This number does not represent the number of failures that have occurred. It merely represents a number which should remain constant on your particular game. In other words, your game could have any number from 1 to 999,999 displayed during this test. That same number should always be displayed each time you run this test. If you discover this number has changed from the last time you ran this test, it means a battery-backed RAM failure has been experienced. Therefore, you should check the Replay Levels and the High Score to Date to see which one failed and thus had been set to zero.

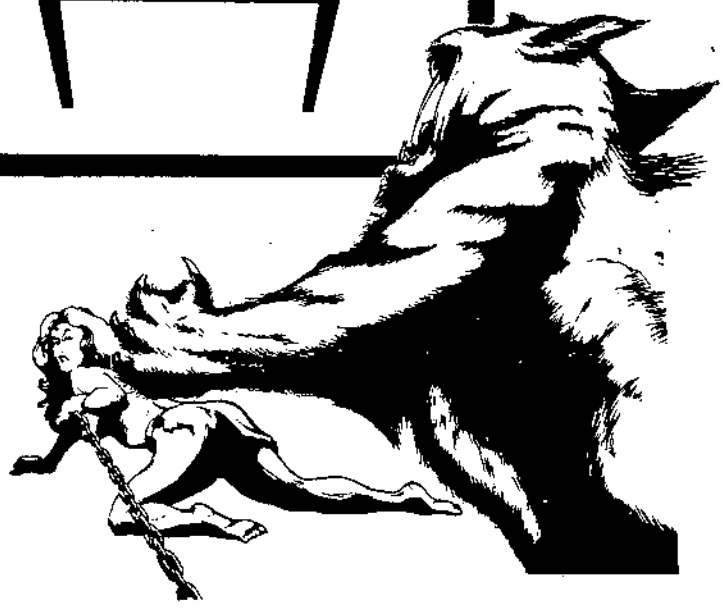
j. checklist of operations covered by this chapter

The following is a checklist of things you should have done to the game as a result of reading this chapter.

1. Screwed leg levelers into legs.
2. Attached front and rear legs to cabinet.
3. Installed tilt weight and wire.
4. Checked Back Box for shipping damage.
5. Checked cabinet for shipping damage.
6. Checked playfield for shipping damage.
7. Performed self-test procedure.
8. Set option switches.
9. Checked for coin rejection and acceptance.
10. Checked for operation of mechanical coin counters.
11. Folded and displayed instruction, coinage, replay level cards, and High-Score-To-Date cards.
12. Permanently secured (with 4 bolts) the Back Box to the cabinet.



game play



2

The game has three modes of operation: *Attract*, *Play*, and *Self-Test*. The attract mode is specifically programmed to attract potential players. The play mode begins when the START button is pressed. Self-Test serves to "freeze" several functions of the game so the operator can determine if everything is operating properly.

a. attract mode

The attract mode begins after game power-up, exiting from self-test mode, or after the end of a game.

1. Attract Mode After Power-Up or Play Mode

In this mode, the score display indicates the score(s) of the previous game, the match/ball display indicates the last ball (3rd or 5th) of the previous game, and the credit display indicates the number of credits in the credit accumulator.

High Score to Date Option: If this option is selected, the score display alternates between the score(s) of the previous game and the high score to date.

Match Option: If this option is selected, the match number of the previous game is displayed in the match/ball display.

2. Attract Mode After Self-Test Mode

In this mode, the score display is blank, the match/ball display is blank, and the credit display indicates the number of credits in the credit accumulator.

High Score to Date Option: If this option is selected, the score display alternates between the score(s) of the previous game and the high score to date.

In the attract mode, the playfield lamps blink on and off in an exciting light show that attracts potential players. The game remains in this mode until a player presses the START button (if there are sufficient accumulated credits or the game is set for the free play option) or by the operator entering into the self-test mode by pressing the TEST button.

b. play mode

After the START button is pushed, the game responds as follows:

1. The player 1 score display indicates two zeros.
2. The number in the credit display decreases by one.
3. The match/ball display shows the number 1, representing the first ball in play.
4. The ball is ejected from the outhole and rolls over to the ball shooter.
5. All playfield lamps stop blinking. The 1,000-point bonus lamp is lighted. All other playfield lamps are unlighted.
6. The flipper controls are enabled.

Additional players may join the game any time before the last player's first ball drops into the outhole. This is done by depositing the required number of coins (if necessary), then pressing the START button. Each time the game responds by adding another set of two zeros in the score displays and decreasing the accumulated credit in the Credit display by one.

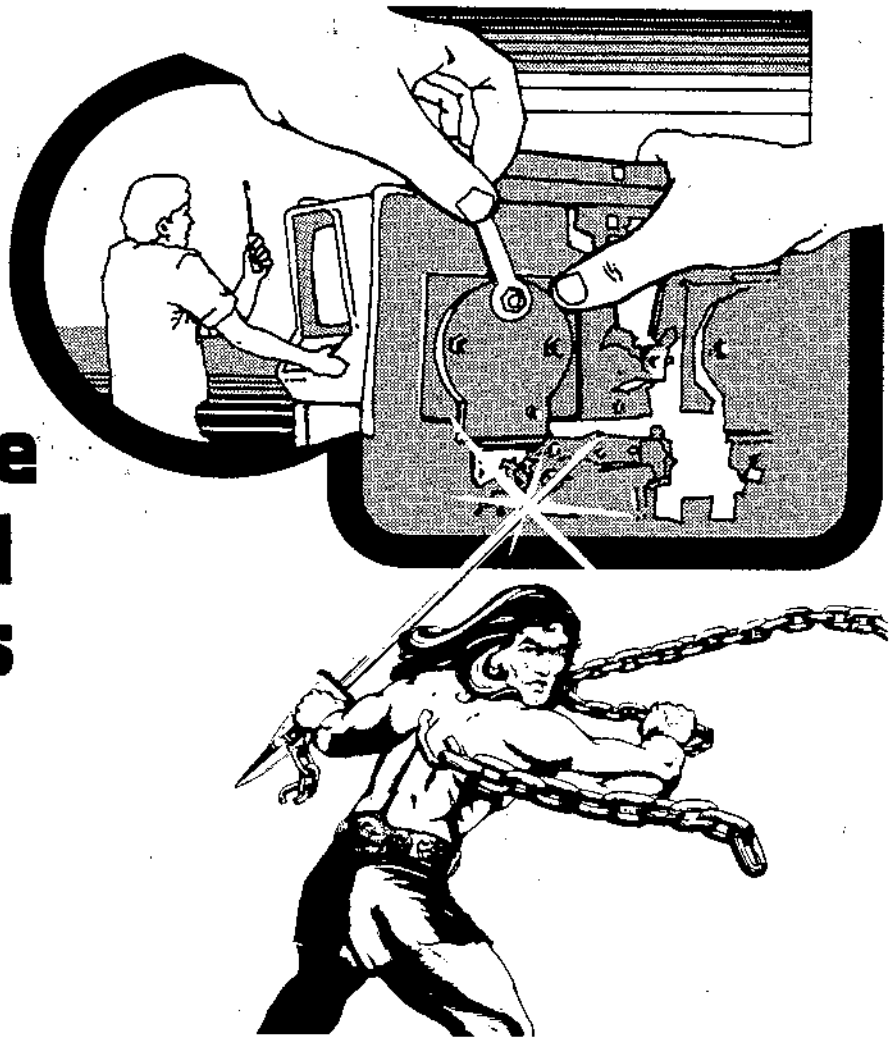
c. game play

1. All scoring is as shown on the playfield.

2. The top three lanes each initiate and/or advance a particular feature. The top left lane initiates and/or advances DOUBLE BONUS, the middle lane EXTRA BALL, and the right lane SPECIAL. None of these lanes will *award* any feature, but only activate the feature for advancement. If switch SWB, toggle 5, is OFF, the feature is only advanced and awarded when the ball passes through the "Path of Victory". If the toggle is ON, both the top lanes and the Path of Victory advance the feature. However, the ball must pass through the Path of Victory to award the feature.

3. Whenever EXTRA BALL or SPECIAL is lit in the Path of Victory, the lower lanes light up the corresponding feature. If the ball passes through these lanes when they are lit, the features are awarded.

4. Bonus System: Basically, the bonus system works like that of most pinball games, but it is possible to collect your bonus while in actual play: Once the bonus has reached its first level (10,000 points), the corresponding 10,000 target will flash. Hitting this target awards the 10,000 points. From this point, the bonus is continued to 20,000 points and so on up to 40,000. Once a target has been lit, but has not been hit, the bonus will not advance to a higher level until the target *is* hit. All of the bonus is collected when the ball drains. For example, a player could collect 20,000 bonus points during play. Upon drain, he will collect an additional 20,000.



maintenance and adjustments

a. cleaning

3

1. Cabinet and Back Box

Any *non-abrasive* household cleaner may be used to clean the cabinet, back box, and other metal or wood parts. The playfield shield is not of the conventional glass material, but is an acrylic plastic (to limit the weight that must span the oversize playfield), and should NEVER be dry wiped. The dust may cause scratches in the material that will seriously detract from the player appeal of the game. Use a soft, damp cloth, and a plastic cleaner or plain water when cleaning the playfield cover.

2. Playfield

Atari has improved the playfield surface for longer wearing qualities. Much of the player appeal in a pinball game depends on smooth ball travel over the entire surface. To keep the playfield and ball from prematurely wearing, use a non-abrasive cleaner only. For even better care, wax the playfield surface with a good playfield wax, obtainable from your Atari distributor. Do not use products such as "Formula 409" or "Windex", kitchen cleansers, soapy cleaning pads or steel wool, waxes or polishes not specifically intended for playfields, or great amounts of water. These products may remove the dirt, but they also remove the top surface of the playfield graphics, and may cause the playfield to collect even more buildup of residue.

While cleaning the playfield, avoid getting foreign material into the bodies of star rollovers.

b. fuse replacement

There are twelve fuses in Hercules. Fuses F1 and F2 are located on the Primary Distribution Assembly, while fuses F3 through F6 are in a fuse strip on the Power Distribution Assembly. Fuse F7 is not used. Table 3-1 gives the function and value of fuses F1 to F6. Fuses F8 through F12 (on AC Adapter PCB) are all 10 amp @ 250V, Fast-Blow.

c. lamp replacement

All playfield and back box lamps are 6.3 volt, 150 milliampere, bayonet-type, general purpose miniature lamps, type #47. In order to get optimum playfield lighting, many of the lamps are mounted deep in or below the playfield. Due to the nature of this design, it may be difficult to change some of the lamps. In some cases it may prove easier for you to remove the lamp socket itself to get good access to its lamp. In doing this, be very careful not to damage the harness wire connected to the lamp socket. Many lamps are best accessed through the bomb bay doors in the bottom of the cabinet.

d. switch replacement

Most of the game switches operate at only 5 volts and carry a very low current. Pitting of these switches is extremely unlikely.

For part numbers for "exact replacement" of a switch, refer to the game Illustrated Parts Catalog.

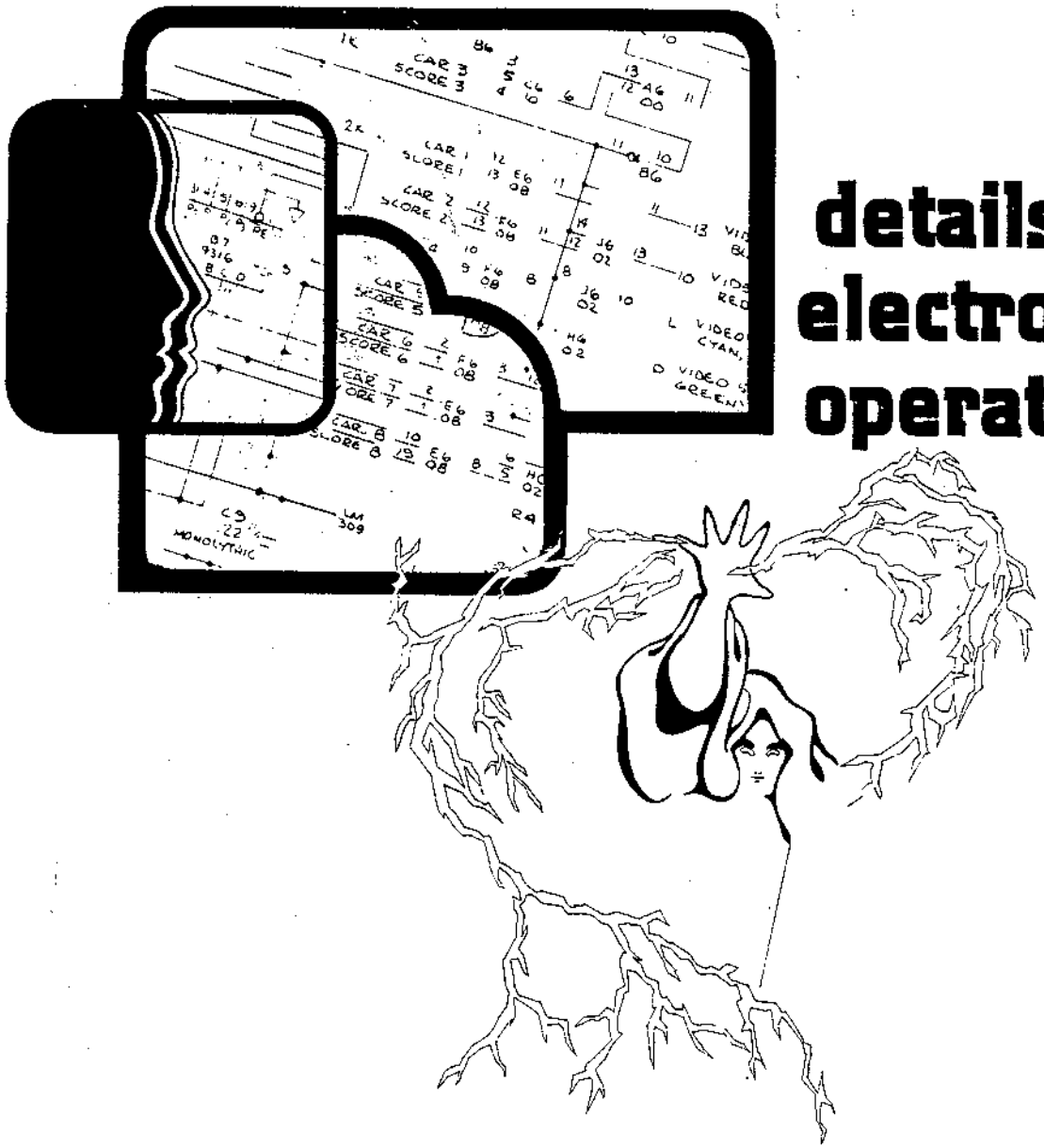
e. lubrication of playfield parts

A tube of lubricant is shipped with each game. This is for you to use on the moving playfield parts such as thumper bumpers, standing targets, ball ejectors, and the ball shooter. When lubricating a part, apply only a thin coat of lubricant with a cotton swab. When applying the lubricant to the ball shooter, make sure you don't get any on either ball shooter spring, as the lubricant may come off on a player.

One cost advantage of lubricating solenoid plungers is that if a solenoid should burn out, the plunger won't freeze to the plastic tube, and the solenoid and tube only need be replaced.

Table 3-1 Fuse Functions and Values

FUSE	VALUE	FUNCTION
F1	5 amp @ 250 V, Slow-Blow	Main Power
F2	2 amp @ 250 V, Slow-Blow	Service Outlet
F3	15 amp @ 250 V, Slow-Blow	Fluorescent Display high voltage and Solenoid power
F4	15 amp @ 250 V, Slow-Blow	LED Display power, Back Box controlled lamps power, and Playfield controlled lamps power
F5	7 amp @ 250 V, Slow-Blow	I/O PCB Audio Amplifier, Coin Door Lockout Coil, Coin Counter power, and unregulated logic supply
F6	10 amp @ 250 V, Slow-Blow	Uncontrolled Back Box lamps, uncontrolled Playfield lamps, and Coin Door lamp power



details of electronic operation

a. circuitry features

1. RAM Batteries

Battery-backed RAM (location H6 on Processor PCB) contains the accounting information of Self-Test. When the game is set to *off* or unplugged, battery-backed RAM is powered by three AA batteries. Since battery-backed RAM is a CMOS device, it takes little current to hold the information written into it.

Therefore, the lifespan of the batteries (located in the battery clip on the lower left corner of the Processor PCB) in the game is nearly equivalent to the shelf life of the bat-

teries—about one year. It is therefore advisable to change the batteries every nine months, to ensure no loss of data. Batteries should be changed with the power on.

Replace only with size AA alkaline batteries. The following note applies:

> **NOTE**
>
> The RAM batteries should be replaced **(with game power on)** about once **every 9 months** to ensure no loss of data. Replace batteries **only with size AA alkaline batteries.** Insert batteries with **polarities as marked** on the Processor PCB immediately above the battery clip.

2. LEDs on the Printed Circuit Boards

a. Processor PCB

There are five LEDs on the Processor PCB; they are identified as LED1 thru LED5.

When lit, LED1 is an indicator of the presence of the +5 VDC logic power. LED2 thru LED5 are used during the Self-Test procedure as an aid for troubleshooting a memory failure. Information at the top of the Option Switch label (located immediately above the Processor PCB in the Back Box) helps you determine if the memory failure is in the RAM or ROM and isolates the failure to the chip level.

b. I/O (Input/Output) PCB

There are two LEDs on the I/O PCB. When lit, LED1 is an indicator of the presence of +5 VDC logic power. When lit, LED2 is an indicator of a failure in either one or more of the playfield driver transistors or in a solenoid coil.

3. LED Displays

Atari's new-generation pinball games have LED displays located in the back box. These displays along with their attached driver PCB assemblies are completely interchangeable. Therefore, if one fails, you may swap it with another.

4. Microprocessor

Atari pinball games are designed around the Motorola M6800 microprocessor. The microprocessor is at location N6 on the Processor PCB.

5. ROM/PROM Memory

ROM is the abbreviation for read-only memory. PROM is the abbreviation of programmable read-only memory.

When we begin the production of a pinball game, we generally program our own memory (PROMs). After the first few weeks of production, we begin installing ROM memory in our games (it takes over two and one half months from the time of our order to have ROMs manufactured). Therefore, when you received this game, you may have either six PROMs or three ROMs for memory. In fact, it is even possible to have a combination of both ROMs and PROMs in your game. One ROM is equivalent to two PROMs. The following is a list of ROMs and their equivalent PROMs:

ROM1 in K/L7 = PROMs in E5 and J5
ROM2 in M7 = PROMs in D5 and K5
ROM3 in J7 = PROMs in F5 and H5

6. Processor PCB Low-Power Schottky TTL Circuitry

The Processor PCB in the game uses mostly low-power Schottky TTL integrated circuitry. The advantages of this circuitry are high circuit density, high speed, and low power consumption; thus a smaller power supply is required and less heat is generated by the PCB. However, there is one disadvantage in troubleshooting the PCB: grounding outputs or connecting them to +5 VDC may cause circuit damage. Therefore, the following caution applies to the Processor PCB.

> **CAUTION**
>
> The Processor PCB contains Lower-Power Schottky (LS) integrated circuitry. Grounding the outputs of this circuitry or connecting them to +5 VDC may result in damaging the circuitry.

7. Solenoid Overcurrent Protection Circuit

All playfield solenoid drivers and coils are protected from potential fire hazard, in the event of a shorted driver or coil, by the overcurrent protection circuit of the solenoid circuitry. See Section E of this chapter for a description of this circuit.

8. Test Points on Printed Circuit Boards

Test points have been provided on the Processor, I/O, and AC Adapter PCB to aid you in troubleshooting the boards. Test points +5V and +12V are of the power inputs to the boards from the Power Supply Distribution. The Processor PCB has three conveniently located ground (GRD) points. The I/O PCB has two ground points.

On the Processor PCB, test points +9V, Φ2, $\overline{\text{TEST}}$, and AUDIO are of signals generated on the Processor PCB. The $\overline{\text{WDOGKILL}}$ test point was added for use by Atari in developing future pinball games.

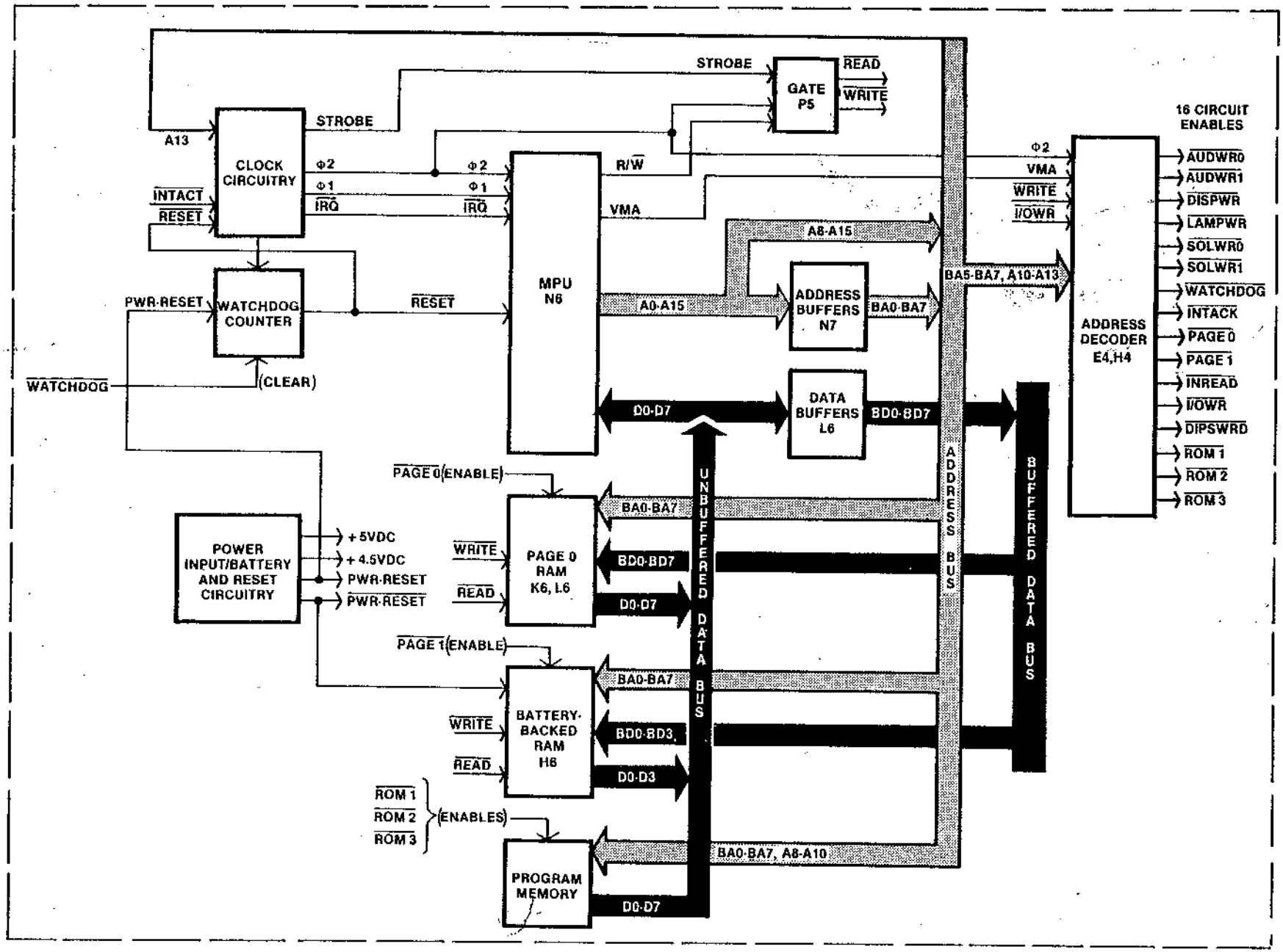


Figure 4-1 MPU Circuitry

b. game power distribution

The game receives its power from the AC line via a line filter. The AC voltage from the filter goes to the master ON/OFF switch located under the right front corner of the cabinet, then to the primary power assembly and to the playfield solenoids. The primary power assembly contains the primary power fuses (see Chapter 3, Section C, for fuse replacement information), the voltage selection plug for Transformer T1 primary winding, and the connectors for the line and interlock switch. The interlock switch, located on the hinge side of the coin door, turns the game power OFF when the coin door is opened. However, the coin door interlock switch plunger may be pulled to the alternate ON position for servicing the game with the coin door opened. The service outlet inside the cabinet is powered even when the coin door is opened and the interlock switch is OFF, but not when the master ON/OFF switch is OFF.

Transformer T1's secondary connects to the power distribution assembly located in the upper right corner of the back box. This assembly contains the rectifier bridges, fuses, filter capacitors, and power distribution PCB (see Chapter 3, Section b, for fuse replacement information). The power distribution PCB contains the +5 VDC regulator, and the various connectors for distributing power to the game.

With this game, you received this manual and three large drawings, marked Sheet 1 thru Sheet 3. Each sheet is marked Side A on one side and Side B on the reverse side. The wiring diagrams on Sheet 2, Side A provide all the information for the distribution of power throughout the game. These diagrams contain cross references for you to locate the termination of connectors. As an aid in finding the right sheet for these terminations, see the Table of Contents of the three large sheets on the lower right of Sheet 1, Side A.

c. processor pcb's microprocessor circuitry

The following paragraphs provide information about the circuitry of the printed circuit boards of the game. With this information we provide block diagrams of the circuits. In the block diagrams we have tried to use the same blocks in which we have divided the schematic diagrams of the Processor, I/O and AC Adapter PCB. We hope that this will aid you in directly identifying the actual functions of the circuitry.

The block diagram of Figure 4-1 illustrates how the circuitry is linked together on the Processor PCB for the MPU (microprocessor) circuitry. The following is a discussion of the function of each block of Figure 4-1.

1. MPU (Microprocessor)

The MPU, at location N6, controls the entire game circuitry. This device outputs addresses, reads data instructions, stores data in the RAM (random-access memory), reads previously stored data from the RAM, reads switches, and activates solenoids and lamps.

The MPU receives two clock signals, Φ 1 and Φ 2 (Phase 1 and Phase 2) from the Clock circuitry. These clock signals provide the basic synchronization that is critical to the operation of the MPU.

The $\overline{\text{RESET}}$ input to the MPU forces the MPU to perform specific instructions when power is initially applied to the game or if a program error is detected by the watchdog circuitry.

The pulses of the $\overline{\text{IRQ}}$ (interrupt request) are counted by the MPU. These pulses are used as the basic timing of the game. For example, the information that you find in the accounting procedure of the Self-Test that gives the total play time of the game (in minutes) is a result of the MPU counting these pulses. The MPU also uses this timing to output lamp data, output data to the multiplexed displays, and to synchronously debounce switch inputs.

The R/$\overline{\text{W}}$ (read/$\overline{\text{write}}$) output designates whether the MPU is in the read or write mode for a given clock cycle. R/$\overline{\text{W}}$ is gated by additional circuitry to provide $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ signals to the RAM and Address Decoder.

The VMA (valid memory address) output of the MPU indicates to the address decoder that the MPU is performing a valid read or write operation, and that the address currently on the MPU address bus is stable, during the high duration of Φ 2.

2. Clock and Watchdog Circuitry

The Clock circuitry provides opposite phase, non-overlapping, Φ 1 and Φ 2 (Phase 1 and Phase 2) clock signals for the basic synchronization of the MPU. The circuitry also provides an $\overline{\text{IRQ}}$ (interrupt request) signal to the MPU every 2.048 milliseconds. The watchdog counter resets the MPU in the event of a program malfunction.

To allow for more access time for reading or writing the RAM, or reading or writing the I/O PCB, it was necessary to reduce the speed of the MPU clock from the normal 1 MHz rate to a rate of 0.667 MHz. However, since most of the MPU's time is spent reading Program Memory which does not require the lower frequency clock, it would be very inefficient to clock the MPU at a constant rate of 0.667 MHz. Therefore, it was necessary to have a two-speed clock. The signal CLOCKSWITCH controls the frequency of the MPU clock. Whenever the MPU is reading Program Memory, address line A13 goes high, causing the CLOCKSWITCH signal to pulse high. When the MPU is writing to or reading from RAM or the I/O PCB, A13 remains low, causing CLOCKSWITCH to be low. The CLOCKSWITCH signal is applied to the Decade Counter R2. When low, counter R2 counts from four to nine—six counts. When high, the counter counts from six to nine—only four counts. This dynamically allocates the Φ2 high pulse duration as a function of the address range.

The Φ1 and Φ2 clock signals are derived from the 4 MHz crystal oscillator, Y1. The signal is divided down by counter R2 for a QB output of 1 MHz when CLOCKSWITCH input to R2 is high, and 0.677 MHz when CLOCKSWITCH is low. Therefore, Φ1 and Φ2 have two frequencies (frequency of Φ1 and Φ2 are always equal). The 1 MHz Φ1 and Φ2 waveform is two signals with a period of 1 microsecond (positive pulse and negative pulse each equal to 500 nanoseconds). The 0.667 MHz Φ1 and Φ2 waveform is two signals of opposite polarity with a period of 1.5 microseconds (Φ1 positive pulse equals 500 nanoseconds, negative pulse equals 1 microsecond—Φ2 positive pulse equals 1 microsecond, negative pulse equals 500 nanoseconds).

During normal operation, Φ1 and Φ2 clock signals are constantly changing from fast to slow. Therefore, if you look at the clock with an oscilloscope, the signals look unstable. However, to check the clock at the 1 MHz rate, check while depressing the RESET button on the Processor PCB. To check the clock at a continuous 0.667 MHz rate, clip pin 2 of Inverter N5. (When finished observing this speed of clock frequency, remember to resolder N5, pin 2.

$\overline{IRQ}$ (Interrupt Request) countdown begins at the QA output of counter R2. The division of the QA frequency continues through eight stages of counter L2 and four stages of counter M2 and is then fed to flip-flop M1. Since the QA output of counter R2 is a constant 2 MHz, the $\overline{IRQ}$ output of flip-flop M1 is a constant pulse period of 2.048 milliseconds. When the MPU receives a low $\overline{IRQ}$, it outputs the address 18E0 (hex) that results in an $\overline{INTACK}$ (Interrupt Acknowledge) signal from the address decoder and then performs the function of the interrupt routine in the MPU. $\overline{INTACK}$ results in resetting flip-flop M1 for a high $\overline{IRQ}$ output. The flip-flop is also reset by a $\overline{RESET}$ signal that results from either a PWR-RESET (power reset) or an output from the watchdog counter.

The watchdog counter is a hardware circuit that guards against a software failure. The second half of counter M2 receives an input clock from the Q_D output of the first half of counter M2. The second portion of counter M2 should never reach its maximum count. This is due to a PWR-RESET signal during power-up and the MPU outputting the address 18C0 (hex) that results in a low $\overline{WATCHDOG}$ signal from the address decoder after power-up. This signal clears the second half of counter M2, thus preventing the output at Q_D of counter M2 from going high. If the MPU should fail to output the necessary address, the counter will count to its maximum, resulting a low $\overline{RESET}$ signal to the MPU input.

3. Power Reset Circuit

The power reset circuit's function is to reset, and hold in the reset condition, the MPU and other game circuitry, until the power input voltages are stabilized. A delay is established by RC network C7 and R13. Because of this network, it takes a little less than half a second for a voltage to develop at the base of transistor Q1 that is sufficient for Q1 to conduct. When Q1 conducts, transistor Q2 turns off, resulting in a high $\overline{PWR\text{-}RESET}$ and a low PWR-RESET signal. Resistor R8 provides hysteretic feedback to the base of transistor Q1 to clamp Q1 into conduction. When power is removed from the game and as the +12.5 VDC supply drops below +10 VDC, the reverse of the preceding occurs and the MPU and other game circuitry are reset. The RC network of capacitor C29 and resistor R123 delays the reset input ($\overline{PWR\text{-}RESET}$) to the battery-backed RAM. As the +5 VDC supply drops, diode CR7 becomes reverse-biased, isolating the RC network from the bleeding +5 VDC supply. Therefore, the battery-backed RAM is permitted to complete its cycle during power down.

4. Address Decoder

The address decoder performs the critical function of "turning on" or enabling the appropriate game circuitry (i.e., RAM, program memory, I/O PCB solenoid latches, etc.) at the appropriate time. Once these circuits are enabled, information can be transferred back and forth between the MPU and the game circuitry.

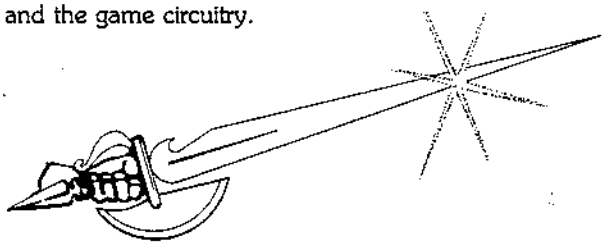


Table 4-1 Universal Processor PCB Memory Map

ADDRESS																	R/W	DATA								FUNCTION	ADDRESS DECODER SIGNAL
HEXADECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0		
0000-00FF	X	X	0	0	0	X	X	X	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	Working RAM	PAGE 0
0800-08FF	X	X	0	0	1	X	X	X	A	A	A	A	A	A	A	A	R/W					D	D	D	D	Battery-Backed RAM (Half-Byte)	PAGE 1
1000	X	X	0	1	0	X	X	X	X	X	X	X	X	X	X	X	R	D								Self-Test Input	INREAD
1000	X	X	0	1	0	X	X	X	X	X	X	X	X	X	X	X	R		D							Disabled Solenoid Input	INREAD
1000-1007	X	X	0	1	0	X	X	X	X	X	X	X	X	A	A	A	R			D	D	D	D	D	D	External Switch Inputs	INREAD
1800	X	X	0	1	1	X	X	X	0	0	0	X	X	X	X	X	W	D								Audio Noise Enable	AUDWR0
1800	X	X	0	1	1	X	X	X	0	0	0	X	X	X	X	X	W		D							Audio Waveform Enable	AUDWR0
1800	X	X	0	1	1	X	X	X	0	0	0	X	X	X	X	X	W			D	D					Audio Octave Select	AUDWR0
1800	X	X	0	1	1	X	X	X	0	0	0	X	X	X	X	X	W					D	D	D	D	Audio Waveform Select	AUDWR0
1820	X	X	0	1	1	X	X	X	0	0	1	X	X	X	X	X	W	D	D	D	D					Audio Frequency Divisor	AUDWR1
1820	X	X	0	1	1	X	X	X	0	0	1	X	X	X	X	X	W					D	D	D	D	Audio Amplitude Control	AUDWR1
1840-1846	X	X	0	1	1	X	X	X	0	1	0	X	X	A	A	A	W					D	D	D	D	Display Data Output	DISPWR
1847	X	X	0	1	1	X	X	X	0	1	0	X	X	1	1	1	W						D	D	D	Display Digit Enable	DISPWR
1860-1867	X	X	0	1	1	X	X	X	0	1	1	X	X	A	A	A	W	D	D	D	D	D	D	D	D	Lamp Output	LAMPWR
1880	X	X	0	1	1	X	X	X	1	0	0	X	X	X	X	X	W					D	D	D	D	Solenoid Output	SOLWR0
18A0-18A5	X	X	0	1	1	X	X	X	1	0	1	X	X	A	A	A	W								D	Independent Control Output	SOLWR1
18A7	X	X	0	1	1	X	X	X	1	0	1	X	X	1	1	1	W								D	Solenoid Enable	SOLWR1
18C0	X	X	0	1	1	X	X	X	1	1	0	X	X	X	X	X	W									Watchdog Reset	WATCHDOG
18E0	X	X	0	1	1	X	X	X	1	1	1	X	X	X	X	X	W									Interrupt Acknowledge	INTACK
2000-2003	X	X	1	0	0	X	X	X	X	X	X	X	X	X	A	A	R	D	D	D	D	D	D	D	D	DIP Switch Input	DIPSWRD
A800-AFFF	X	X	1	0	1	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM 1 Select	ROM 1
3000-37FF	X	X	1	1	0	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM 2 Select	ROM 2
3800-3FFF	X	X	1	1	1	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM 3 Select	ROM 3

Table 4-1 is the memory map for the MPU circuitry address decoder. Note that the address is given in both hexadecimal and binary. In the binary column, an X indicates that it makes no difference whether that address line is high or low. The address necessary to select a given output of the address decoder is indicated with ones and zeros. The actual address lines that are used to address the selected game circuitry are indicated by A's. The R/W column shows that when WRITE (designated by W) is low, the MPU is writing to the selected circuitry. When READ is low, the MPU is reading the selected circuitry. The data column shows the data lines used in the read or write operation. The function column defines the purpose of the read or write operation. The address decoder signal column defines the selected output of the address decoder for the operation.

The address decoder consists of two decoders at locations E4 and H4. Decoder E4 is driven by buffered address lines BA5 thru BA7 and I/OWR (I/O Write) gated with WRITE. Notice that only when I/OWR and WRITE are low, can the outputs of this decoder be active. Therefore, the control of this decoder is not only in address lines A5 thru A7, but also the decoder is enabled by the I/OWR output from decoder H4. Additional control of decoder E4 from the WRITE signal ensures that the selected game circuitry from this decoder is not enabled except for a write condition.

Decoder H4 is driven by address lines A11 thru A13 and $\Phi 2$ gated with VMA. (Disregard address A15, as this is used only during game development.) Address lines A11 thru A13 determine the output of decoder H4.

5. Program Memory

Program memory consists of three ROMs (read-only memory) or six PROMs (programmable read-only memory) with a total memory size of 6K × 8. See Section A of this chapter for information concerning the ROM/PROM equivalents. See the game Illustrated Parts Catalog for ROM or PROM part numbers.

The program memory has the function of instructing the MPU in the operation and rules of this specific pinball game.

When addressed by the MPU, it supplies the data required for the game play. Each ROM or equivalent pair of PROMs are enabled by the address decoder.

6. RAM (including Battery-Backed RAM Memory)

The function of the RAM is to act as a scratch pad for the information that the MPU decides it wants to store. The RAM of locations K6 and L6 stores temporary information while the battery-backed RAM of H6 stores more permanent information, such as the accounting information of the Self-Test Procedure. The battery-backed RAM is automatically powered by a +4.5 VDC battery supply when the line power is turned off. At this time the CE2 input, pin 17, goes low so the RAM consumes less power in this standby mode.

In order to write information into a RAM, the $\overline{\text{WRITE}}$ input must be low, the $\overline{\text{READ}}$ input must be high, and the proper address decode must be active. To read information from the RAM, the $\overline{\text{WRITE}}$ input must be high, $\overline{\text{READ}}$ must be low, and it must be properly selected by the address decoder.

Note that the battery-backed RAM will lose data if the batteries are removed and the line power is off. Batteries should be changed with the power set to ON to retain data during the battery change. Batteries should be changed every nine months. Only size AA alkaline batteries should be used.

7. Power Input and Battery Circuit

The power input circuit receives +5 VDC, +7 VDC, and +12.5 VDC from the Power Distribution Board. The +5 VDC input is the logic supply voltage for all circuits on the Processor and I/O PCBs. To complement the +5 VDC input, resistor R9 supplies additional current to the logic supply from the +12.5 VDC input from the Power Distribution Board. The +12.5 VDC input is also used as the supply voltage for the audio circuit on both the Processor PCB and I/O PCB. The +7 VDC input is used as the supply voltage for the anode drivers of the display interface circuit.

With no power input, the battery supply BAT1 thru BAT3 provides +4.5 VDC to maintain data in the battery-backed RAM. When power is applied, +12.5 VDC (which is clamped to the +5 VDC supply by diode CR1) forward biases diode CR2, resulting in raising the battery-backed RAM voltage to +5 VDC. Therefore, the drain is removed from the batteries, as diode CR4 is reverse biased. The battery-backed RAM will retain data with a battery supply voltage greater than 3.0 VDC.

d. switch circuitry

The following circuit description relates to the schematic diagram of the Processor PCB and I/O PCB. These schematics are located on Sheet 2, Sides A and B, of the large sheet included with this manual. See Figure 4-2 for a block diagram representation of this circuit.

The MPU addresses option switches SWA thru SWD with buffered address lines BA0 and BA1 and reads the switches thru data lines D0 thru D7. The coin door, start, and playfield switches are addressed by buffered address lines BA0 thru BA2 and read through data lines D0 thru D5.

1. Coin Door, Start and Playfield Switches

The wipers (or "common" terminals) of all coin door, start, and playfield switches are connected to the inputs of six data selectors E2 thru E7. The N.O. (normally open) contacts of each switch are connected directly to ground. Each switch input is connected to a pullup (470-ohm resistor tied to +5 VDC) on the I/O PCB. Therefore, when a switch is closed, the data selector input for that switch is pulled from +5 VDC to 0 VDC (ground) through a 100K ohm resistor (used to protect the data selector against static electricity).

Each data selector has the capability of handling eight switch inputs. Since there are six data selectors, this circuitry can handle up to 48 switches (although this game does not use all the possible switch inputs). The address inputs (IOBA0 thru IOBA2) to the data selectors select the switches to be read by the MPU. Therefore, six switches at a time may be read by the MPU via data outputs SD0 thru SD5. Signals SD0 thru SD5 are buffered onto the MPU data bus by tristate buffer H7, which is enabled by the MPU address decoder signal $\overline{\text{INREAD}}$.

2. Game Option Switches

One side of all the option DIP (dual inline package) switches on the Processor PCB is connected to ground. The opposite contact of all these switches is connected to the inputs of multiplexers A4, B4, C4, D4. Each input of these multiplexers is connected to a pullup (10K ohm resistor tied to +5 VDC). Therefore, a closed switch pulls the input from +5 VDC to 0 VDC (ground).

Each multiplexer handles eight inputs from the DIP switches. The address inputs (BA0 and BA1) to the multiplexers select two toggles from each switch to be read by the MPU. Therefore, eight switch toggles at a time are read by the MPU via data outputs D0 thru D7. $\overline{\text{DIPSWRD}}$ (from the

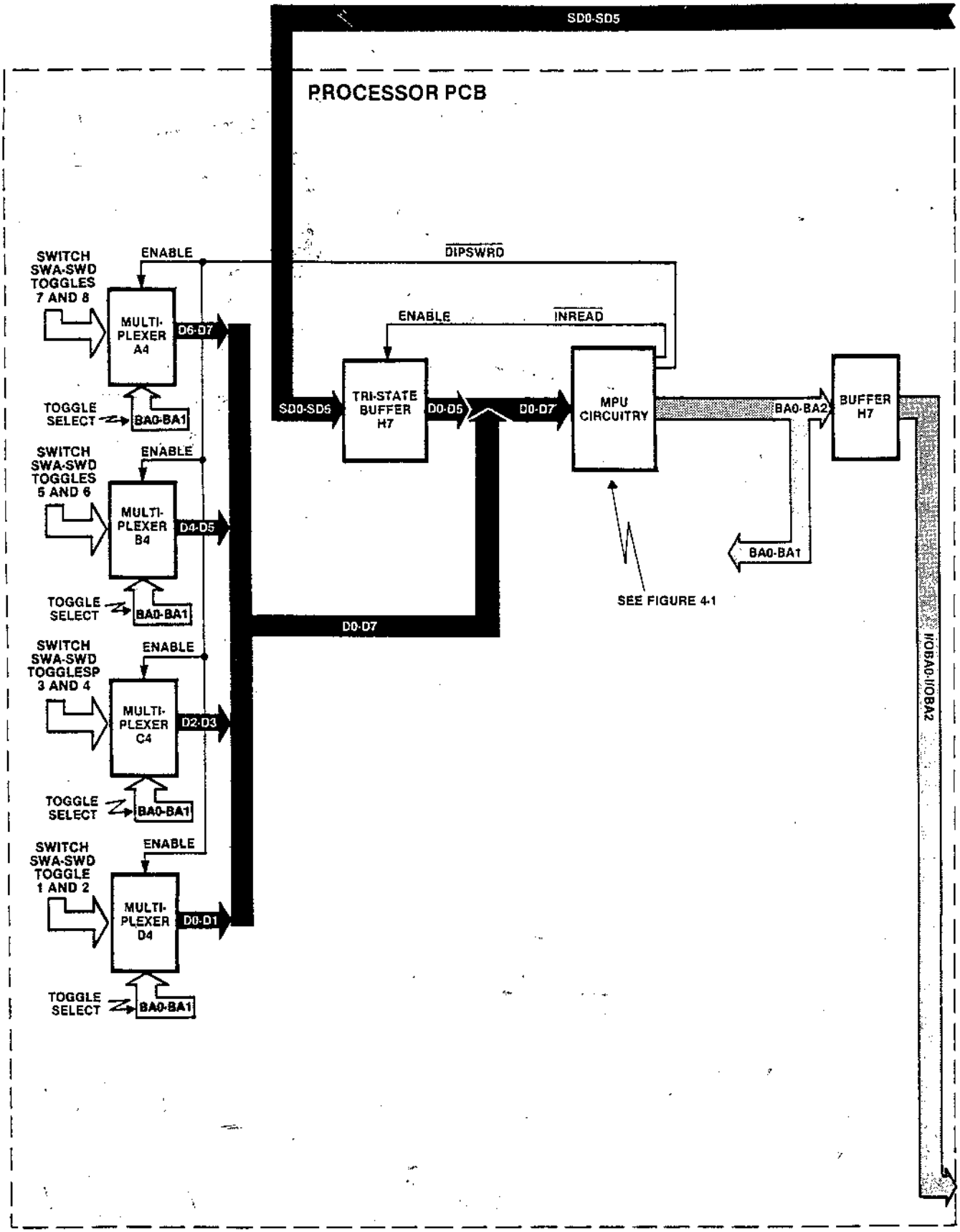
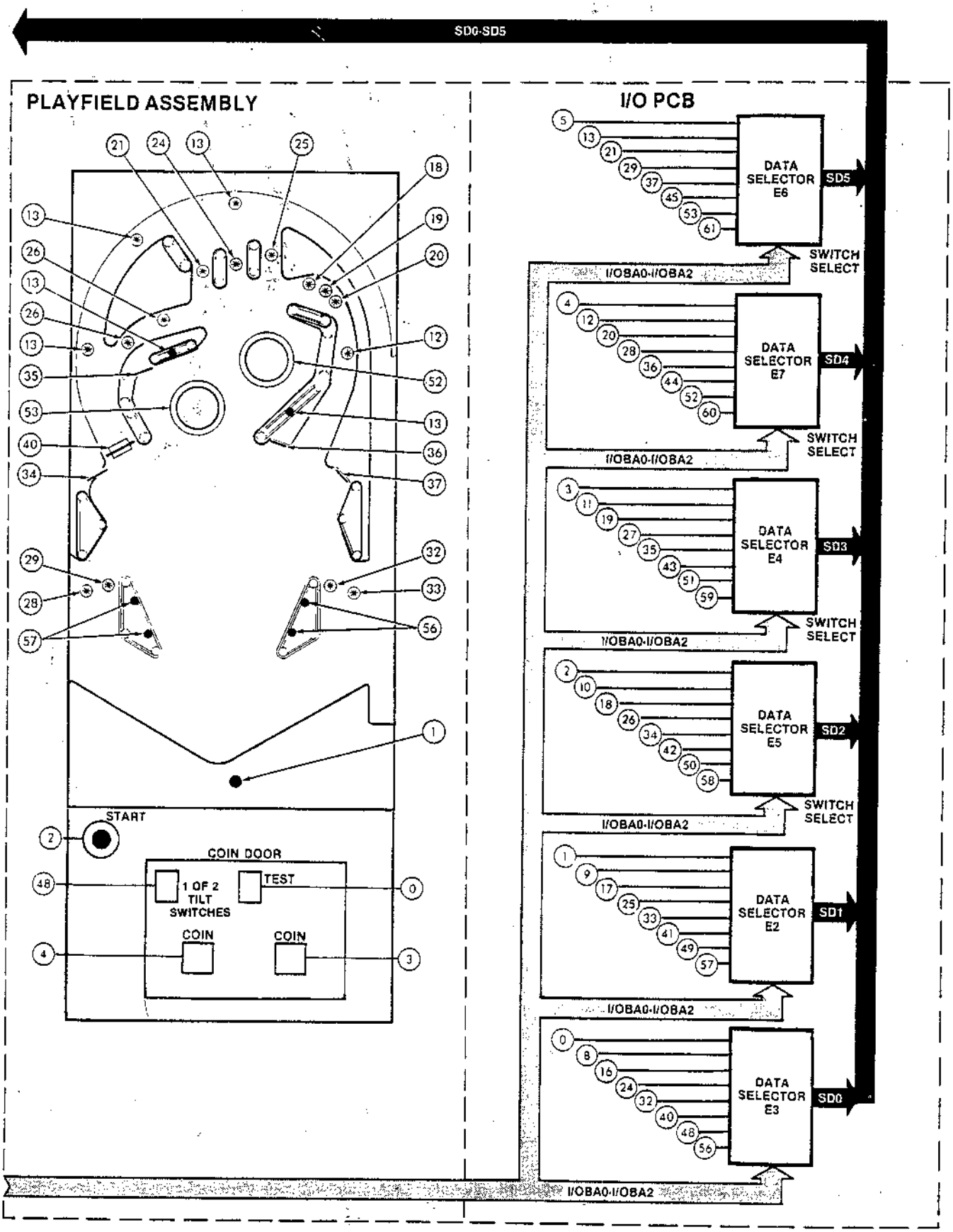


Figure 4-2 Switch Circuitry


SD0-SD5
PLAYFIELD ASSEMBLY
I/O PCB
START
COIN DOOR
1 OF 2 TILT SWITCHES
TEST
COIN
COIN
DATA SELECTOR E6
DATA SELECTOR E7
DATA SELECTOR E4
DATA SELECTOR E5
DATA SELECTOR E2
DATA SELECTOR E3
SD5
SD4
SD3
SD2
SD1
SD0
SWITCH SELECT
I/OBA0-I/OBA2

MPU address decoder) enables the multiplexers (A4, B4, C4, D4), which have tri-state outputs, and gates option switch information onto the MPU data bus.

3. $\overline{\text{TEST}}$ Test Point on Processor PCB

Not only can the game's self-test be activated by the coin door self-test switch, but also by grounding the $\overline{\text{TEST}}$ test point on the Processor PCB. The MPU reads the test point through tri-state buffer H7 on data line D7. Therefore, self-test may be easily activated while the Processor PCB is on the test bench.

e. solenoid circuitry

The following circuit description relates to the schematic diagram of the Processor PCB, I/O PCB and AC Adapter PCB. These schematics are located on Sheet 2, Sides A and B, of the large sheets included with this manual. See Figure 4-3 for a block diagram representation of this circuit.

All solenoids are energized by commands from the MPU circuitry. There are two solenoid circuits on the I/O PCB. One is for long-term or low-current relays, such as the coin door lockout coil. The other is for short-term high-current solenoids, which are the playfield solenoids.

The AC Adapter PCB supplies a return path to AC energized relays and flipper switches. It also isolates the AC voltage from the I/O PCB.

1. Coin Door Lockout Coil

The key to this circuitry is addressable latch A6/7, on the I/O PCB. From the MPU circuitry, the latch receives buffered address signals I/OBA0 thru I/OBA2, buffered data signal I/OBD0, and solenoid write command I/OSOLWR1. The address signals select the output of the latch to which the data is to be written. The solenoid write command signal $\overline{\text{I/OSOLWR1}}$ (from the address decoder of the MPU circuitry), when present, **allows** the data to be latched.

When power is initially applied to the game, the I/O RESET, generated by the MPU circuitry, sets all the outputs of latch A6/7 to a low. The MPU eventually sends out the address and data for enabling the coin door lockout coil; when appropriate. When the latch receives the proper solenoid write command, a high is written to the coin door lockout coil output of the latch. The high biases driver transistor Q82 into conduction, thus applying a ground to the lockout coil. Since the other side of the lockout is attached to +12.5 VDC, the coil energizes.

2. AC Adapter PCB

When the MPU circuitry recognizes that there is credit for a game, the start button is pressed, and the game is not tilted, the flipper switches are enabled via the AC Adapter PCB. When driver transistor Q85 (on the I/O PCB) conducts, the transistors Q1 and Q2 (on the AC Adapter PCB) are turned on. This results in high 1D and 6D inputs to latch U1. On the next rising edge of U1's clock, the high inputs are transferred to the 1Q and 6Q outputs of latch U1.

Opto-isolators U12 thru U15 totally isolate the low-voltage DC driving signal from the AC energizing signal. When the outputs of buffers U2 go low, resistors R50 thru R52 and R53 thru R55 bias bi-directional thyristors Q13 and Q14 into conduction. Thyristors Q13 and Q14 provide a full-wave conduction path to the flipper solenoids through the flipper switches. Therefore, as long as the flipper enable output of addressable latch A6/7 (on the I/O PCB) remains high, the flippers are enabled for operation.

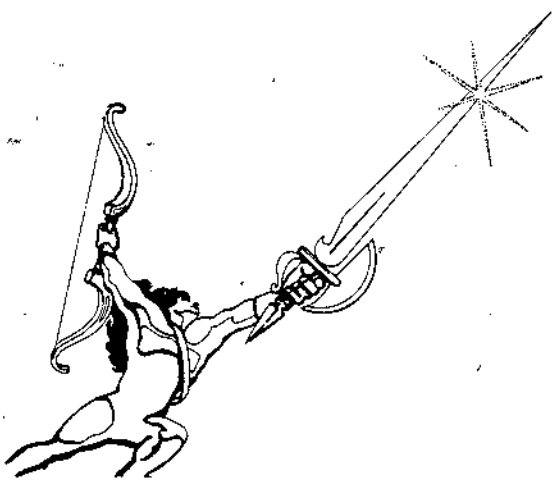
3. AC Adapter PCB Clock and Clear

When power is applied to the game, the low clear input of latch U1 remains until capacitor C1 charges (through resistor R26) enough to bias transistor Q7 into conduction. When transistor Q7 conducts, a high CLEAR signal results, enabling latch U1 to transfer data.

When power is applied to the game, capacitor C2 charges (through diode CR1 and resistor R68) to the +5.1 voltage of zener CR3.

The base of the transistor is driven from a positive half-wave pulse of voltage from resistor R69. This causes clock pulses when the AC sine wave input is close to its zero voltage crossing point.

Opto-isolator U3 completely isolates the AC voltage input to the clock circuit from the +5 VDC supply voltage.



4. Playfield Solenoids

The playfield solenoids, coin counters, and total plays counter are enabled by the SOLENABLE signal from latch A6/7 (see Part 1 of this Section for the operation of latch A6/7). SOLENABLE resets the pin 13 output of one half of flip-flop B4/5 for a high $\overline{\text{DISABLE}}$ and a low DISABLE output, and sets the pin 1 output of the other half of flip-flop B4/5 for a low output to the base of transistor Q106. The high $\overline{\text{DISABLE}}$ output provides the proper bias for the conduction of transistor Q81 and solenoid driver transistor Q103. The low DISABLE output of the flip-flop removes the inhibit from decoder/latch B2. The MPU writes to decoder/latch B2 with buffered data signals I/OBD0 thru I/OBD3 for the selected solenoid. When B2 receives the solenoid write command I/OSOLWR0, the selected output of B2 is latched high.

Let's say that the MPU writes to latch B2 with data to turn on output latch fifteen, the outhole kicker. The outhole kicker now has a ground path through resistor R109, solenoid enable transistor Q103, solenoid driver transistor Q90, and the outhole kicker coil to +50 VDC. Therefore, the outhole kicker energizes.

The slingshots' and thumper bumpers' outputs of the I/O PCB are received by the AC Adapter PCB. They are energized in the same manner as the flipper solenoids (as described in Part 2, AC Adapter PCB).

Under normal operation each playfield solenoid will conduct about 5 amps when energized. However, if a solenoid coil is shorted, the solenoid driver will initially attempt to supply the short circuit current. If one solenoid driver transistor is shorted and another solenoid is energized, the two energized solenoids will conduct about 10 amps of current. Transistors Q65, Q66, Q81, and Q103, together with current sense resistor R109, flip-flop B4/5 and associated resistors, capacitors and diodes, form an overcurrent protection circuit. Current in excess of approximately 7 amps will cause a voltage of 0.7 volts across resistor R109 (the current sense resistor). The capacitor of RC network C12 and R108 charges to about 0.7 volts in approximately 5 microseconds (1 TC = 1 microsecond). The 0.7 volt charge on C12 biases transistor Q65 into conduction. This turns off transistor Q66. The pin 10 reset and pin 6 set inputs of flip-flop B4/5 become high, through diode CR2. This resets one flip-flop for a high DISABLE and a low DISABLE output and sets the other flip-flop with a high output to the base of transistor Q106, thus turning Q106 on and lighting LED 2. Transistor Q81 loses its bias, turning off transistor Q103, resulting in the loss of the ground path for the selected coil. Therefore, the coil deenergizes, or will not burn up if it was a shorted coil. The overcurrent protection circuit protects shorted coils or driver transistors from creating a fire hazard.

When power is initially applied to the game, decoder/latch B2 is reset for all low outputs by I/ORESET, generated by the MPU circuitry. This prevents the floating address and data lines from energizing solenoids during power-up.

In the event of a shorted coil or driver transistor, SENSE FAILURE LED flashes on for the duration of the time that the coil is on.

f. lamp circuitry

The following circuit description relates to the schematic diagram of the Processor PCB and I/O PCB. These schematics are located on Sheet 2, Sides A and B, of the large sheets included with this manual. See Figure 4-4 for a block diagram representation of this circuit.

This game has two different lamp circuits. The constantly lit general illumination lamps are powered by 6.3 VAC from the power supply. The second type of lamp is controlled by the microprocessor. The microprocessor-controlled lamps turn on and off during the attract mode and during game play. Due to the simplicity of the general illumination lamps, the following information only relates to the microprocessor-controlled lamps.

The MPU addresses the 64 possible lamps (all 64 are not used in this game) through I/O PCB latches C2/3, C4, C5/6, C6/7, D2/3, D4, D5/6, and D6/7 with buffered address lines BA0 thru BA2, then writes to the latches through buffered data lines D0 thru D7. When the latches receive the lamp write command I/OLAMPWR, the data is transferred to the selected output and latched. When the selected output goes high, the lamp driver transistor is biased into conduction. Since all of the MPU-controlled lamps are connected to a common +7 VDC source, the lamp is lit through the ground path provided by the driver transistor and either diode CR7 or CR8.

When power is initially applied to the game, the latches are reset for all low outputs by I/OLAMPBLANK, generated by the MPU circuitry. This prevents the floating address and data lines from lighting during game power-up.

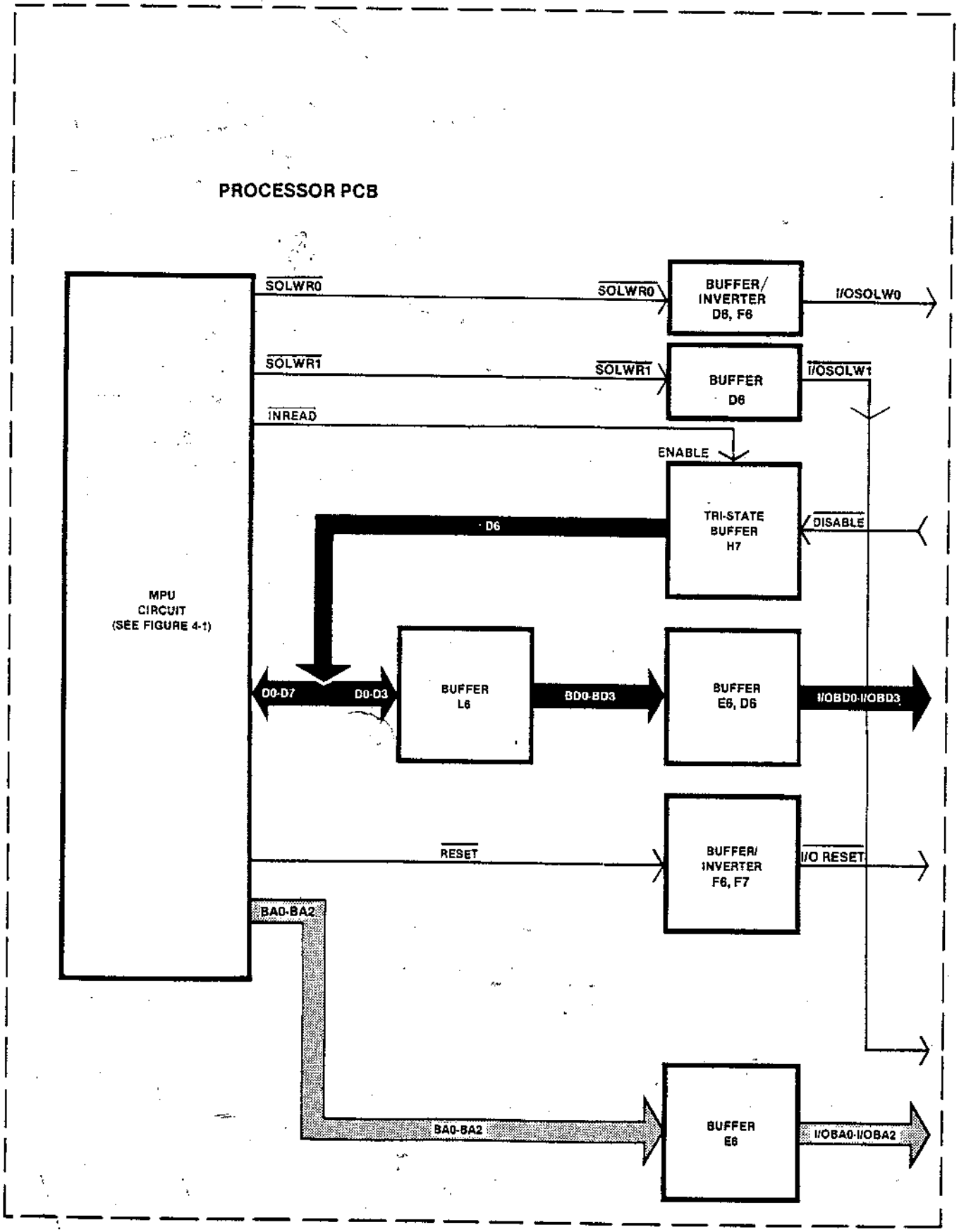
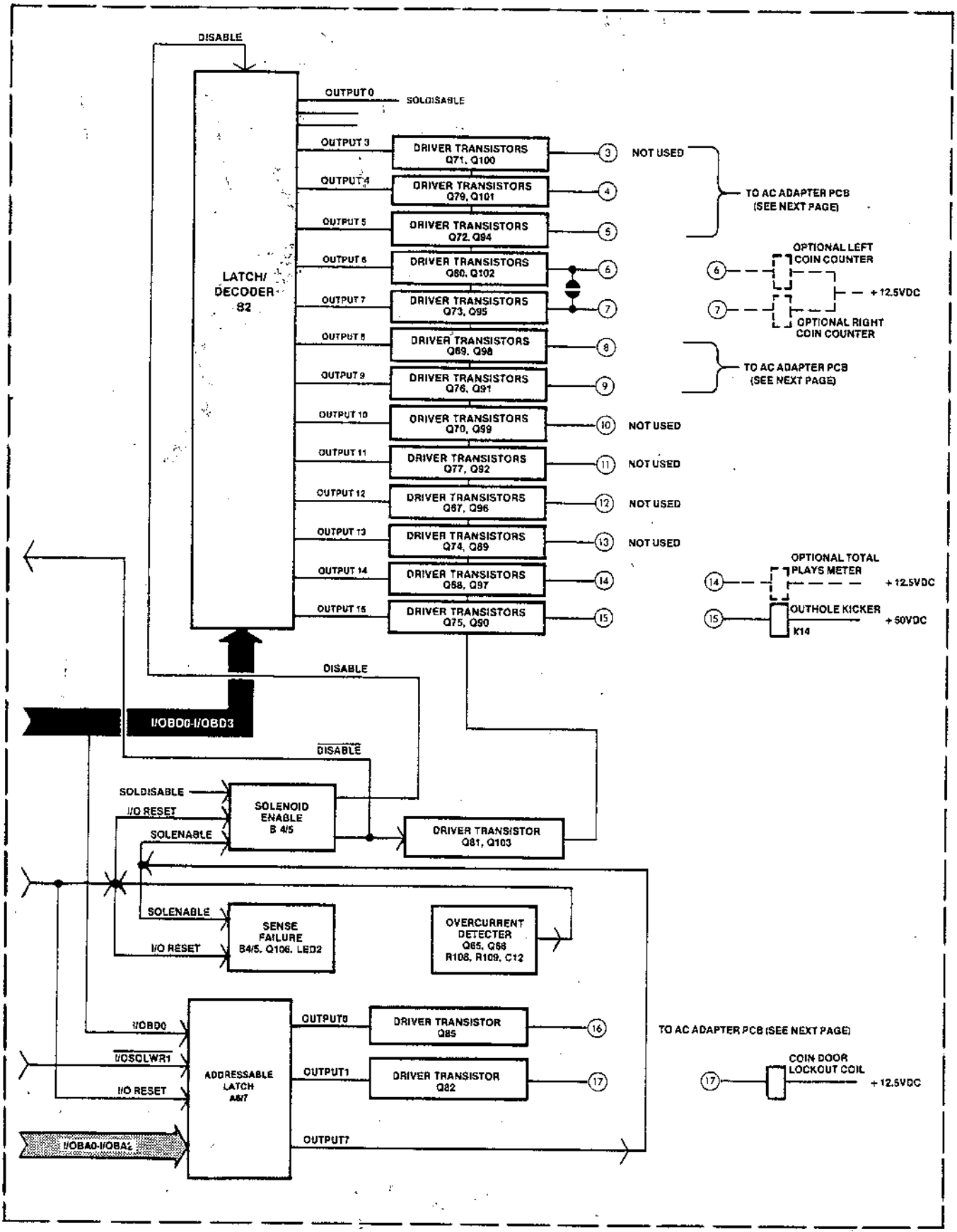


Figure 4-3 Solenoid Circuitry


DISABLE
LATCH/
DECODER
82
OUTPUT 0
SOLDISABLE
OUTPUT 3
DRIVER TRANSISTORS
Q71, Q100
3
NOT USED
OUTPUT 4
DRIVER TRANSISTORS
Q79, Q101
4
TO AC ADAPTER PCB
(SEE NEXT PAGE)
OUTPUT 5
DRIVER TRANSISTORS
Q72, Q94
5
OUTPUT 6
DRIVER TRANSISTORS
Q80, Q102
6
OPTIONAL LEFT
COIN COUNTER
OUTPUT 7
DRIVER TRANSISTORS
Q73, Q95
7
+12.5VDC
OPTIONAL RIGHT
COIN COUNTER
OUTPUT 8
DRIVER TRANSISTORS
Q69, Q98
8
TO AC ADAPTER PCB
(SEE NEXT PAGE)
OUTPUT 9
DRIVER TRANSISTORS
Q76, Q91
9
OUTPUT 10
DRIVER TRANSISTORS
Q70, Q99
10
NOT USED
OUTPUT 11
DRIVER TRANSISTORS
Q77, Q92
11
NOT USED
OUTPUT 12
DRIVER TRANSISTORS
Q67, Q96
12
NOT USED
OUTPUT 13
DRIVER TRANSISTORS
Q74, Q89
13
NOT USED
OUTPUT 14
DRIVER TRANSISTORS
Q68, Q97
14
OPTIONAL TOTAL
PLAYS METER
+12.5VDC
OUTPUT 15
DRIVER TRANSISTORS
Q75, Q90
15
OUTHOLE KICKER
+50VDC
K14
DISABLE
I/OBD0-I/OBD3
DISABLE
SOLDISABLE
I/O RESET
SOLENABLE
SOLENOID
ENABLE
B 4/5
DRIVER TRANSISTOR
Q81, Q103
SOLENABLE
I/O RESET
SENSE
FAILURE
B4/5, Q106, LED2
OVERCURRENT
DETECTER
Q65, Q66
R108, R109, C12
I/OBD0
I/OSOLWR1
I/O RESET
ADDRESSABLE
LATCH
A5/7
I/OBA0-I/OBA2
OUTPUT0
DRIVER TRANSISTOR
Q85
16
TO AC ADAPTER PCB (SEE NEXT PAGE)
OUTPUT1
DRIVER TRANSISTOR
Q82
17
COIN DOOR
LOCKOUT COIL
+12.5VDC
OUTPUT7

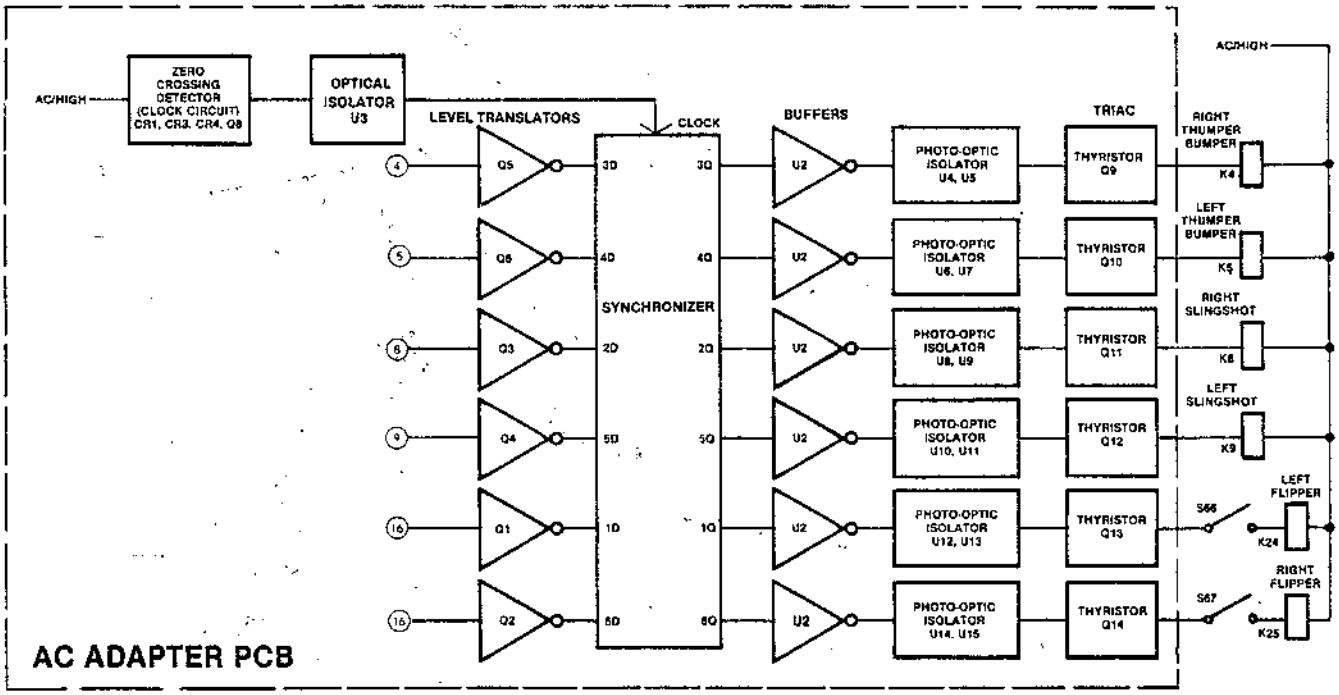


Figure 4-3 Solenoids Circuitry (Continued)

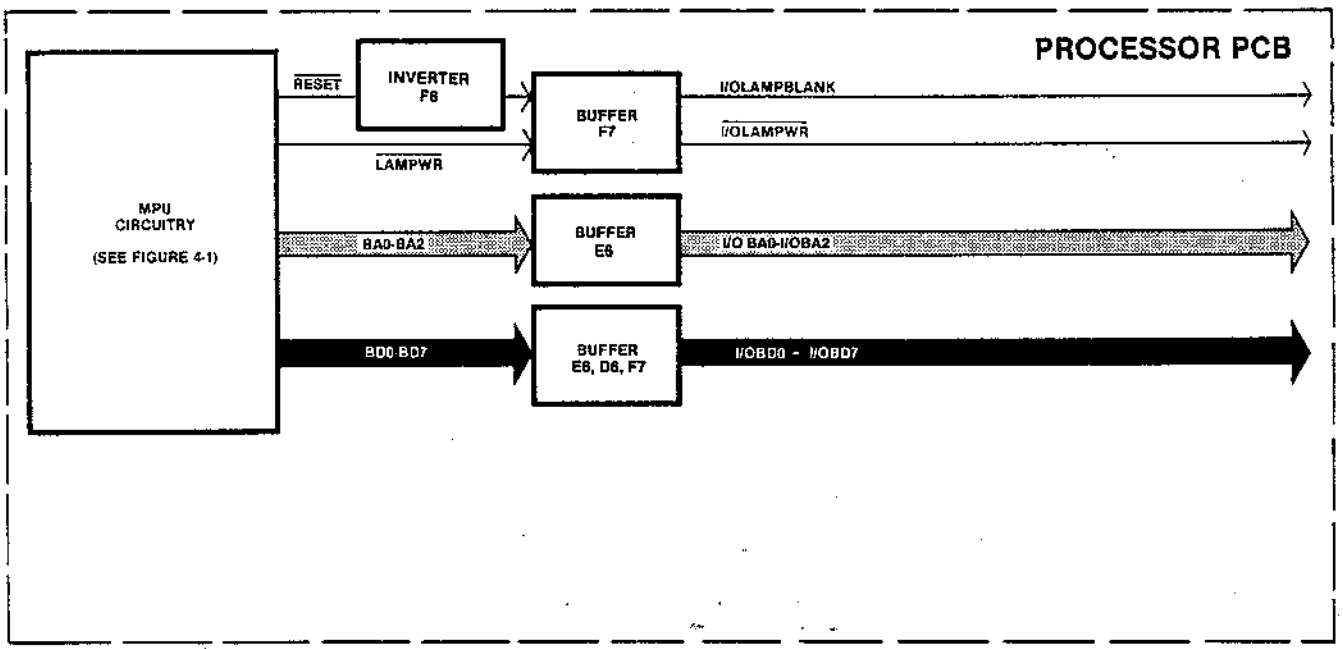


Figure 4-4 Processor PCB

g. display circuitry

The following circuit description relates to the schematic diagram of the Processor PCB and Display Driver PCBs. These schematics are located on Sheet 2, Side A and B, of the large sheets included with this manual. See Figure 4-5 for a block diagram representation of this circuit.

In the game, there are six possible displays: 1) Player 1, 2) Player 2, 3) Player 3, 4) Player 4, 5) BALL/CREDIT/MATCH, and 6) to be assigned on a future game. The MPU first writes display data to the individual Display Driver PCBs. Next it writes data that turns on a particular digit in all displays. This process is repeated for each of the six digits in each of the five separate displays.

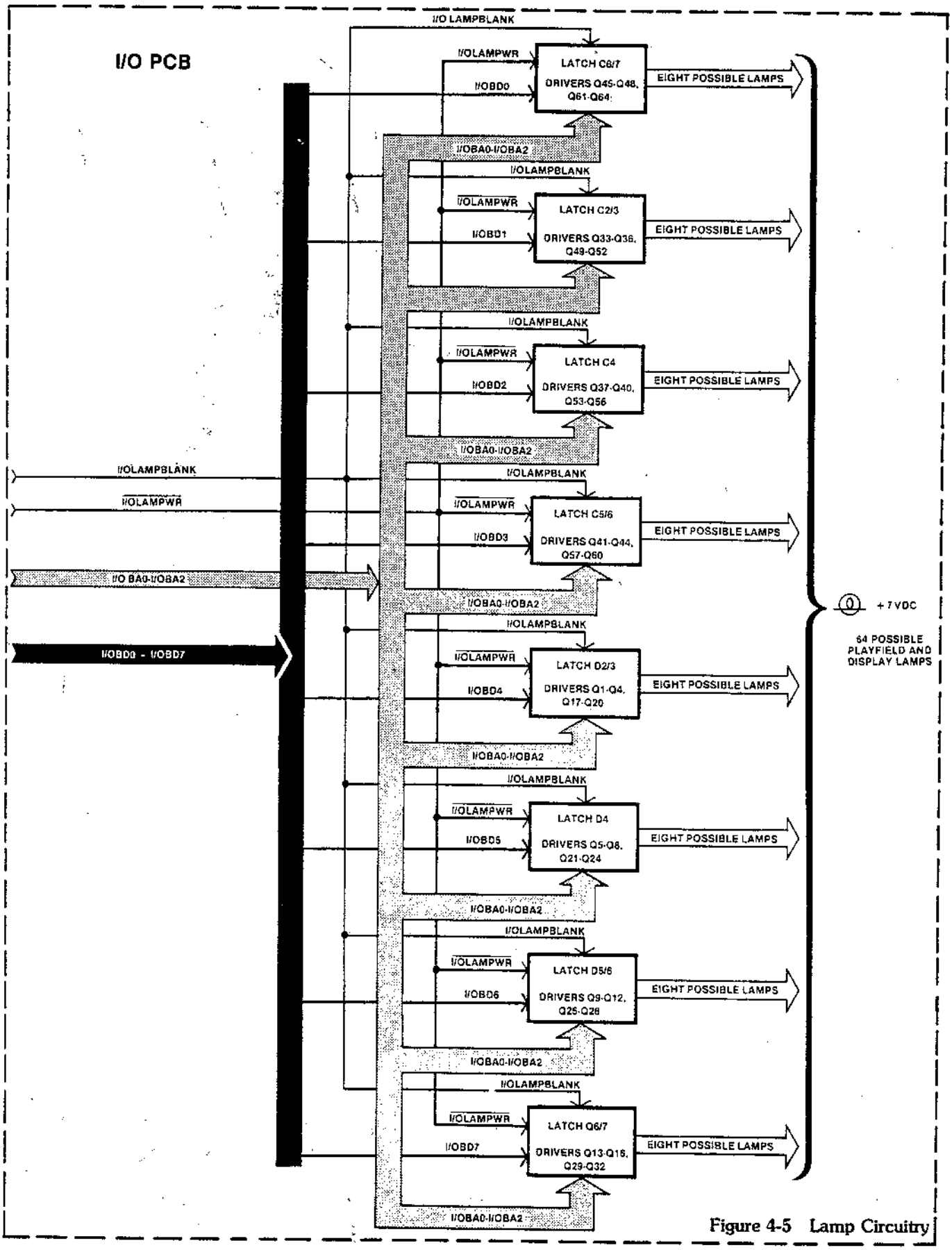


Figure 4-5 Lamp Circuitry

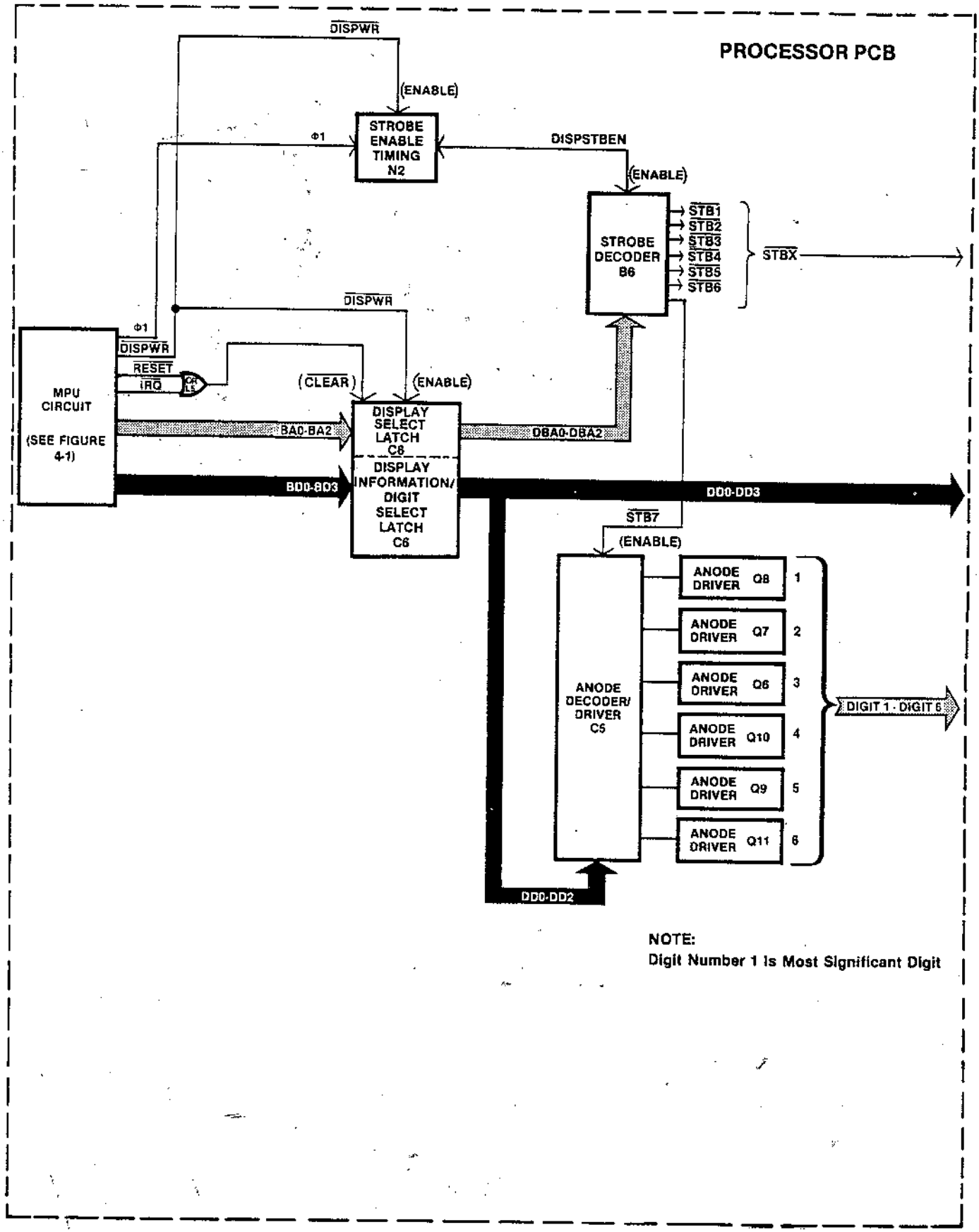


Figure 4-6 Display Circuitry

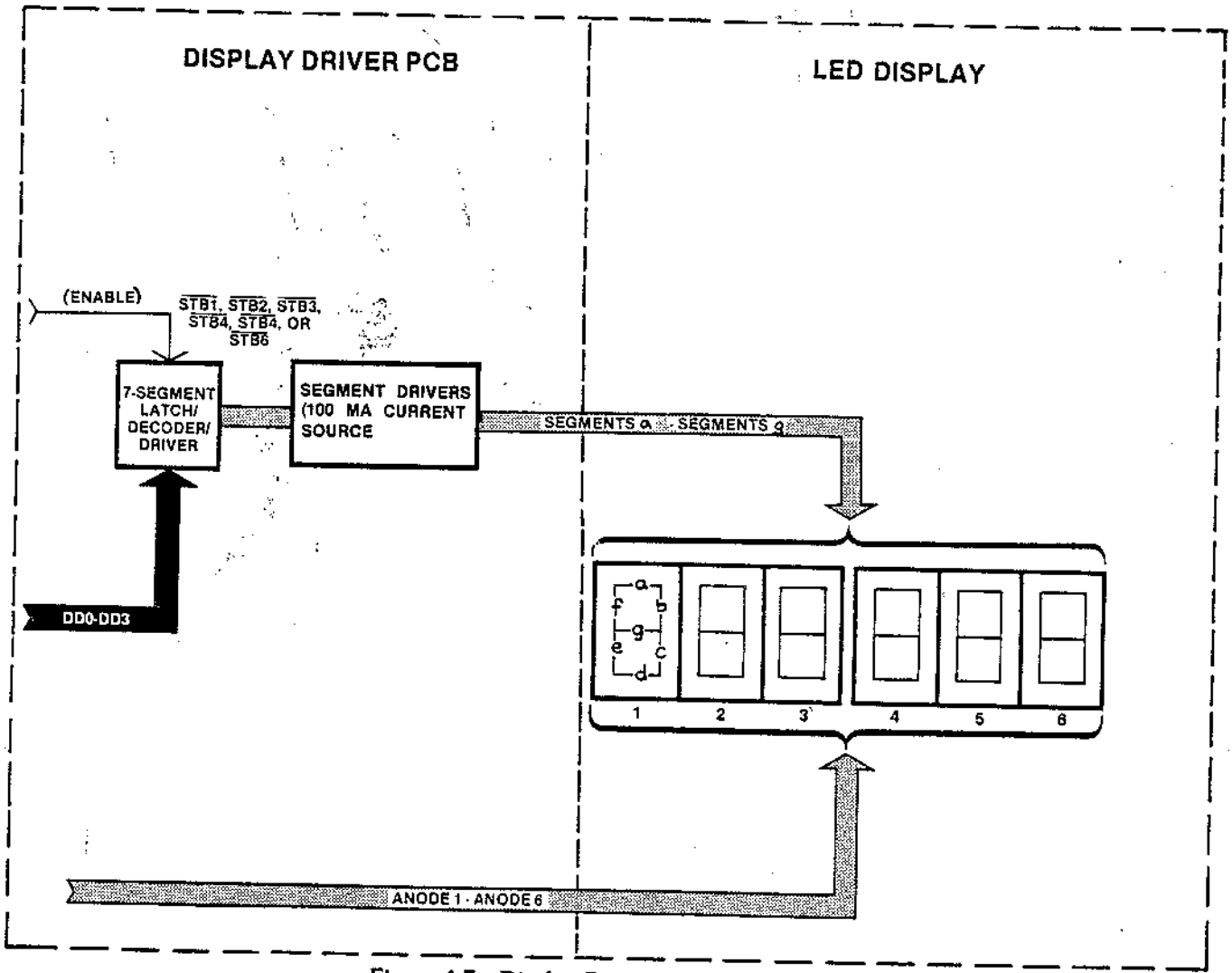
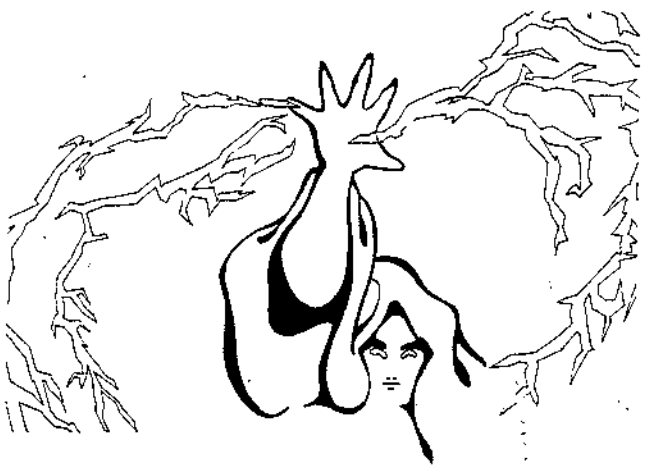


Figure 4-7 Display Drivers and LED Display

When the address decoder of the MPU circuitry outputs the display write command ($\overline{DISPWR}$), the MPU address information at the input of latch C6 is latched at its output and transferred to the address input of strobe decoder B6.



MPU data is also latched at the output of latch C6. Both data and strobe information then go to the Display Driver PCBs. The strobe decoder decodes which Display Driver PCB is to be written to (via $\overline{STB1}$-$\overline{STB6}$). The Display data (DD0-DD3) determines what segment data is being written to that display.

The preceding process is done until all five (six) displays have been addressed and data is latched into each of the 7-segment latch/decoder/drivers. The seventh address received by the strobe decoder causes input D of the anode decoder/driver C5 to go low. This enables the anode decoder/driver for an output as defined by the data input. The selected output of the anode decoder turns on the anode of the selected digit of all the displays. This entire process is done until all six digits of the displays are completed. This six digit cycle is continuously repeated, so that the displays appear to be continuously on.

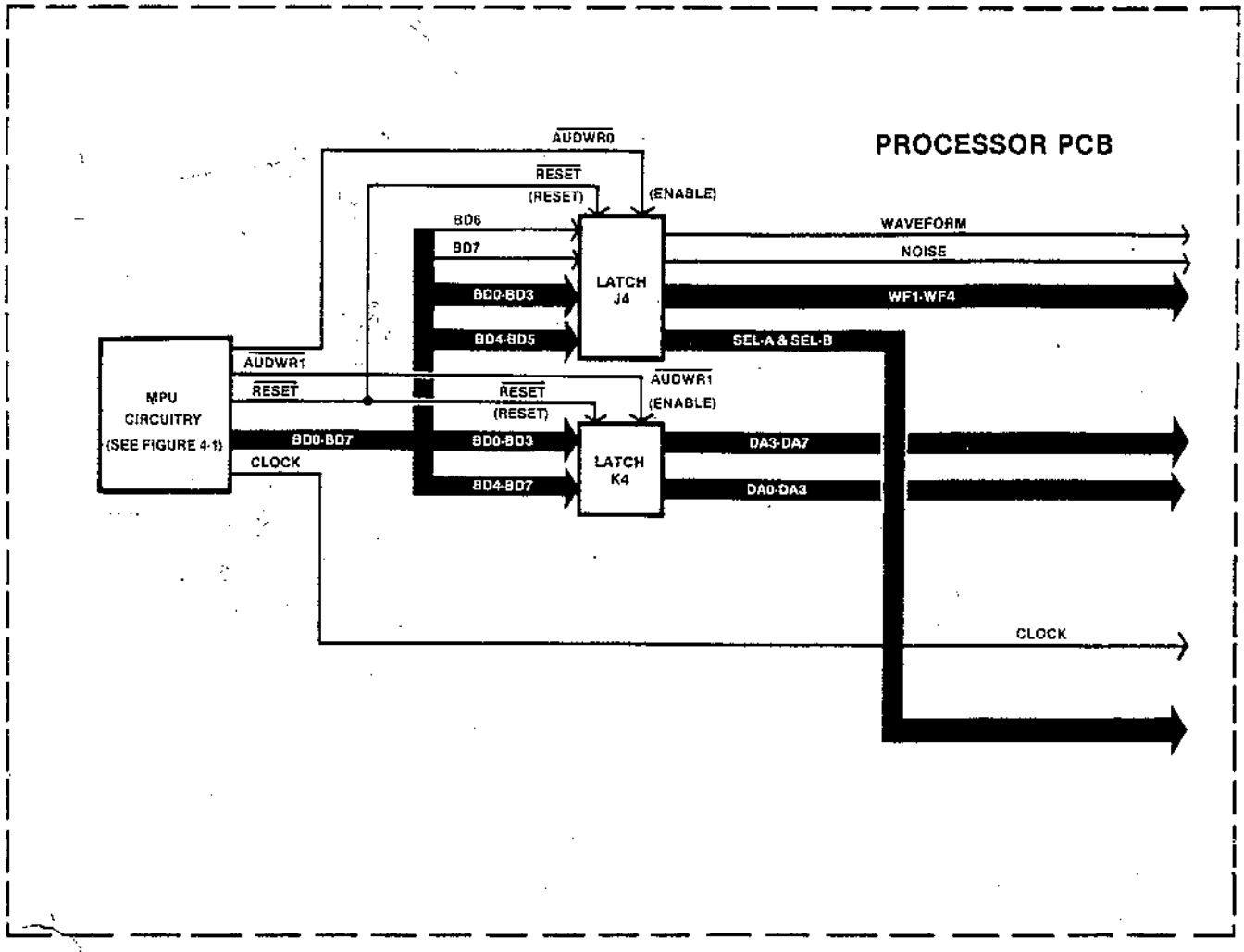


Figure 4-8 Audio Circuitry

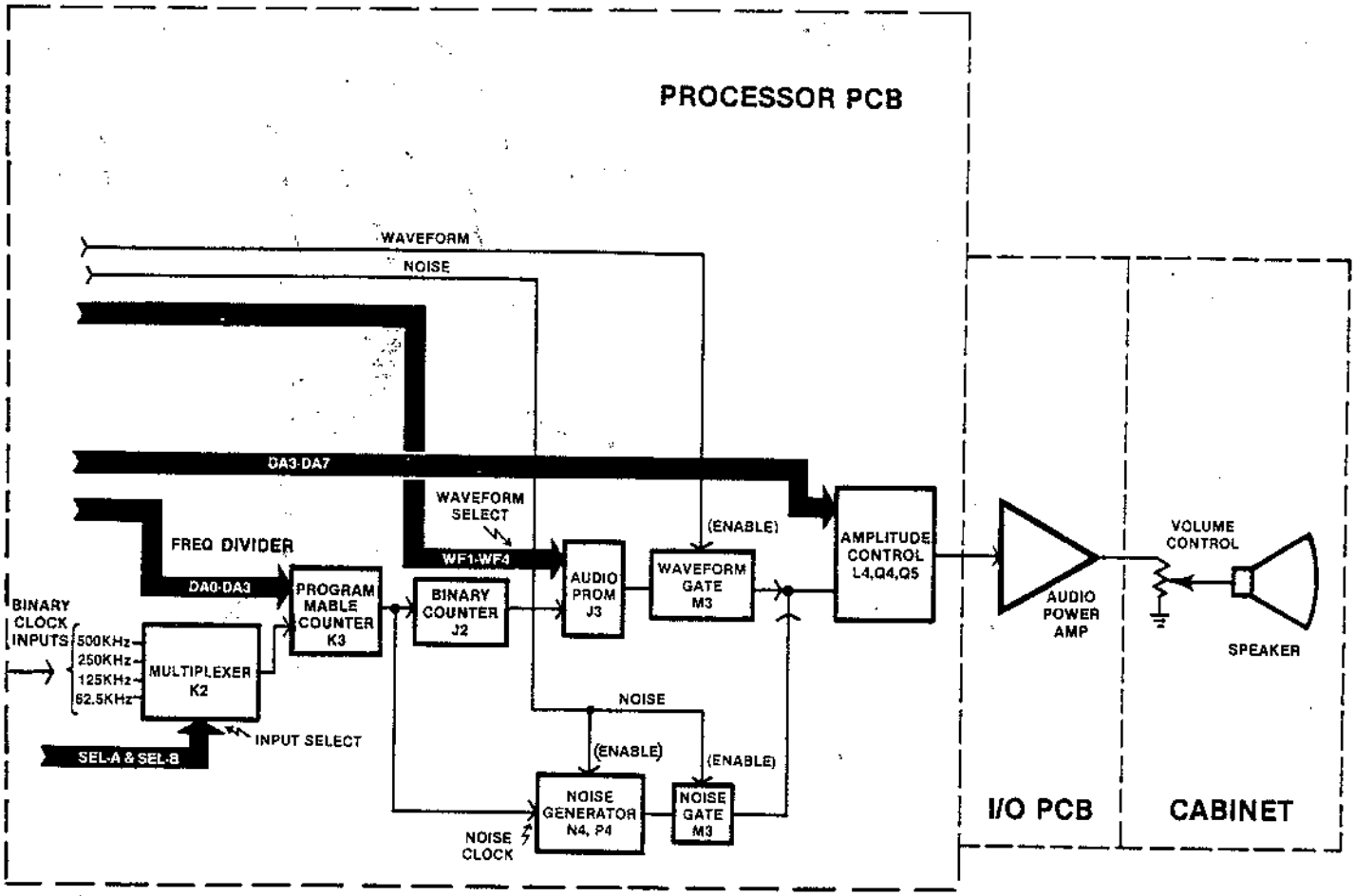
h. audio circuitry

The following circuit description relates to the schematic diagram of the Processor PCB and I/O PCB. These schematics are located on Sheet 2, Sides A and B, of the large sheets included with this manual. See Figure 4-6 for a block diagram representation of this circuit.

There are two audio generators in the audio circuitry: the noise generator, consisting of shift registers N4 and P4, and the waveform generator, consisting of multiplexer K2, programmable counter K3, binary counter J2, and PROM J3. The two audio channels are summed at the input of transistor Q5, then fed into the inputs of four analog gates L4. The outputs of the four gates are applied to a binary attenuator from which the outputs are summed and fed to the I/O PCB for amplification.

When power is initially applied to the game $\overline{\text{RESET}}$, generated by the MPU circuitry, sets latches J4 and K4 for all low outputs, disabling both audio channels. When the address decoder of the MPU circuitry outputs its audio write command ($\overline{\text{AUDWR0}}$), data is latched into latch J4 which defines what generator is to be turned on. A high data bit BD6 turns on the waveform generator, and a high data bit BD7 turns on the noise generator. At the same time, the octave of the waveform is defined by data bits BD4 and BD5; the shape of the waveform is defined by data bits BD0 thru BD3. The second audio write command ($\overline{\text{AUDWR1}}$) latches data into latch K4, which defines the frequency of the waveform and the amplitude of the summed audio signals.

The noise generator is a simple 15-bit pseudo-random sequence generator, clocked by the terminal count from the



waveform generator to make the two frequencies harmoniously compatible. The summed output of the noise generator is AC-coupled by capacitor C10 and fed to voltage dividers R16 and R17, which provide a DC voltage reference. The output of analog gate M3 applies the noise frequency to the summing point of transistor Q5.

The basic frequency of the waveform generator is selected from the input (AUD1-AUD4) of multiplexer K2 (via SEL-A and SEL-B). Programmable counter K3 receives the basic frequency and divides it by the two's complement of the digital number applied at the preset input of K3. In other words, if the selected frequency is 62.5 KHz and the preset input is 12 (DA3 thru DA0 are 1100), the output of counter K3 is 15.625 (65.2 divided by four).

The divided frequency output of K3 is applied to the input of binary counter J2 and the clock inputs of the noise generator. The binary count output of J2 is used for the five least significant bits of the address input of audio PROM J3. The most significant bits of the address input of audio PROM J3. The most significant bit inputs address the PROM for a given waveform (i.e. sine wave, triangle wave, square wave, etc.), while the least significant bits address the time-multiplexed amplitude components of the selected waveform. The data output bits from the PROM are fed to a digital weighted resistive network. PROM J3, together with resistors R23 thru R27, form a digital-to-analog waveform generator.

The analog output, filtered by capacitor C11, is AC-coupled by capacitor C12 and fed to voltage divider R21 and R22, which provide a DC voltage reference. The output of analog gate M3 applies the waveform to the summing point of transistor Q5. Transistor Q5, configured as an emitter-follower, buffers the summed signals. The signal is applied to the inputs of analog gates L4. The analog gates L4 are turned on or off by the control bits from latch K4. Together with resistors R65 thru R69, this circuit is a digitally controlled amplitude attenuator. When all gates of L4 are on, the maximum signal is delivered to the base of transistor Q4. Transistor Q4 forms an emitter-follower, which buffers the signal to audio amplifier D1 on the I/O PCB.

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