manual

VERSION-1.O

Exidy

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FAX™

Operation and Service Manual
1st Edition

(c) 1983 Exidy, Inc.
390 Java Drive, Sunnyvale,
California 94089-1271
Telephone: (408) 734-9410
Toll-free: (800) 538-8402
Telex: 357-499 (EXIDY MNTV)

Exidy Ireland
Gortlandroe Industrial Estate
Nenagh, County Tipperary
Ireland
Telephone (067) 32555
Telex: 70009 (EXDY EI)

FOREWORD

Part One of this manual contains Preliminary Procedures, describing game inspection, installation, and checkout. Also, Adjustment Procedures are given for Power Supply, Audio Volume, and Operator Selectable Options.

Part Two, Modes of Operation, describes the four FAX™ modes: Automatic Self-Diagnostic Test Mode, Attract Mode, Game Play Mode, and Vanity Mode.

Appendix A contains game schematics, with a circuit description on each page opposite.

Appendix B is the Illustrated Parts List. Parts are pointed out in the drawings and listed opposite each drawing.

EXIDY FAX™
OPERATION AND SERVICE MANUAL

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TRADEMARKS

FAX™ is a trademark of Exidy Inc.

WARNING

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measure may be required to correct the interference.

QUESTIONS

Exidy encourages technicians to use the toll-free customer service hotline for any questions they may have regarding FAX™. That number is **(800) 538-8402.**

I. PRELIMINARY PROCEDURES

A. GAME INSPECTION

All Exidy equipment is carefully packaged in well-padded cardboard containers to prevent damage during shipment. **Before** signing the delivery receipt, you should follow this procedure:

1. Check for obvious damage and make certain that the physical piece count of the shipment matches the piece count on the bill of lading. These two procedures should always be done **before** signing the delivery receipt.

2. Shortages and/or obvious damage to the packaging on any given shipment should be noted **in writing** on the delivery receipt **before** signing for the delivery.

3. If concealed damage is suspected on any shipment, those packages believed to contain the damaged goods **should be opened in the presence of the delivery driver.** If the goods have sustained concealed damage, a description of said damage should be noted **in writing** on the delivery receipt **before** signing for the delivery.

4. **Never** apply power to any game with noticeable damage.

1. Filing a Claim

To file a claim, follow this procedure:

1. Any and all damaged freight, including packaging, **should be retained by the consignee** until a physical inspection of said freight can be made by a representative of the carrier involved.

2. The Claims Manager for the carrier involved should be notified as soon as possible, after the damaged goods are received. Preferably, the carrier's Claims Manager should be notified within forty-eight (48) hours of receipt of the goods by the consignee.

3. If warranted, a written claim should be filed with the carrier involved. A detailed description of the damage(s) should be provided and copies of all supporting documents, **including bill of lading and/or delivery receipt, inspection report, and invoice,** should be attached.

4. The sooner a claim is filed, the better for all parties concerned. The carrier against which a claim is filed is required, by law, to respond to (acknowledge) that claim within thirty (30) days of receiving same and must reach a final disposition in the matter within one hundred twenty (120) days.

2. Visual Inspection

1. Remove the rear and front access doors with the appropriate packaged key.

2. Examine each major and electrical component thoroughly for scrapes, dents, broken or missing parts and loose or missing screws.

3. Check for loose cable connectors.

4. Visually verify that all the integrated circuit devices (IC's) plugged into sockets are properly seated and that no IC pins are bent or misaligned.

If you find any damage during this inspection, file a claim with the carrier. Send a complete report of the damage to Exidy Inc.

B. INSTALLATION

Planning the location of the game should involve both physical and electrical considerations. Such physical considerations concern the placement of the equipment with respect to these clearances:

Height: 55.5Ø inches, 14Ø.2 cm.
Width: 37.25 inches, 94.5 cm.
Depth: 24.ØØ inches, 61.Ø cm.

An indoor, relatively dust-free environment is necessary, with proper conditions required of any electrical device. Electrical considerations include availability of an AC outlet with the correct voltage and frequency. You should consider the working space required for technicians and operators including access to the rear of the game.

NOTE:

The cabinet must be within seven feet of an AC outlet. Be certain that a ground jack or terminal is available at the outlet.

CAUTION:

DO NOT remove the AC ground prong from the plug. Doing so **voids your warranty!**

C. PRELIMINARY CHECKOUT PROCEDURE

After properly installing FAX™, we suggest following this procedure to check its operation:

1. Connect the AC power plug into the AC outlet.

2. Once powered up, after five seconds of silence, a quick beep sounding like an organ chord, is heard. This is part of the Exidy Audio Diagnostic Test. A single beep indicates all is well with the audio board. If more than one beep is heard, refer to Part II, Automatic Diagnostic Test Mode.

3. Allow 8-1Ø seconds to pass for the CRT to warm up.

4. Observe the TV monitor display. After Exidy Diagnostic Test are completed assure the correct attract mode is present on the screen, as described in Part II B, Attract Mode. If the FAX™ display is incorrect, contact Exidy's Customer Service Department.

5. Insert the appropriate coin or token into each of the coin slots. The message in the attract mode will flash the following lines:

FAX™

CREDITS

Press Start

One or Two Players

A ONE PLAYER CHALLENGE

A TWO PLAYER RACE

depending on the number of coins dropped into the coin slot, or the number of credits awarded for each coin..

6. Press one or two player start and play the game to verify that all screen images are displayed as described in Part II C, Game Play Mode.

If assistance or repairs are necessary, contact the Exidy's Customer Service Department, (800) 538-8402.

D. ADJUSTMENTS

1. Power Supply Information and Adjustments

All DC Power required to operate FAX™ is supplied in the Exidy Power Supply Module. These supply outputs are as follows:

+5v DC	@	6 amps
-5v DC (Not used)	@	1 amp
+12v DC (HI)*	@	3 amps
+12v DC (LO)*	@	1 amp
-12v DC (HI)*	@	3 amps
-12v DC (LO)*	@	1 amp

* (HI) refers to "high current"
* (LO) refers to "low current"

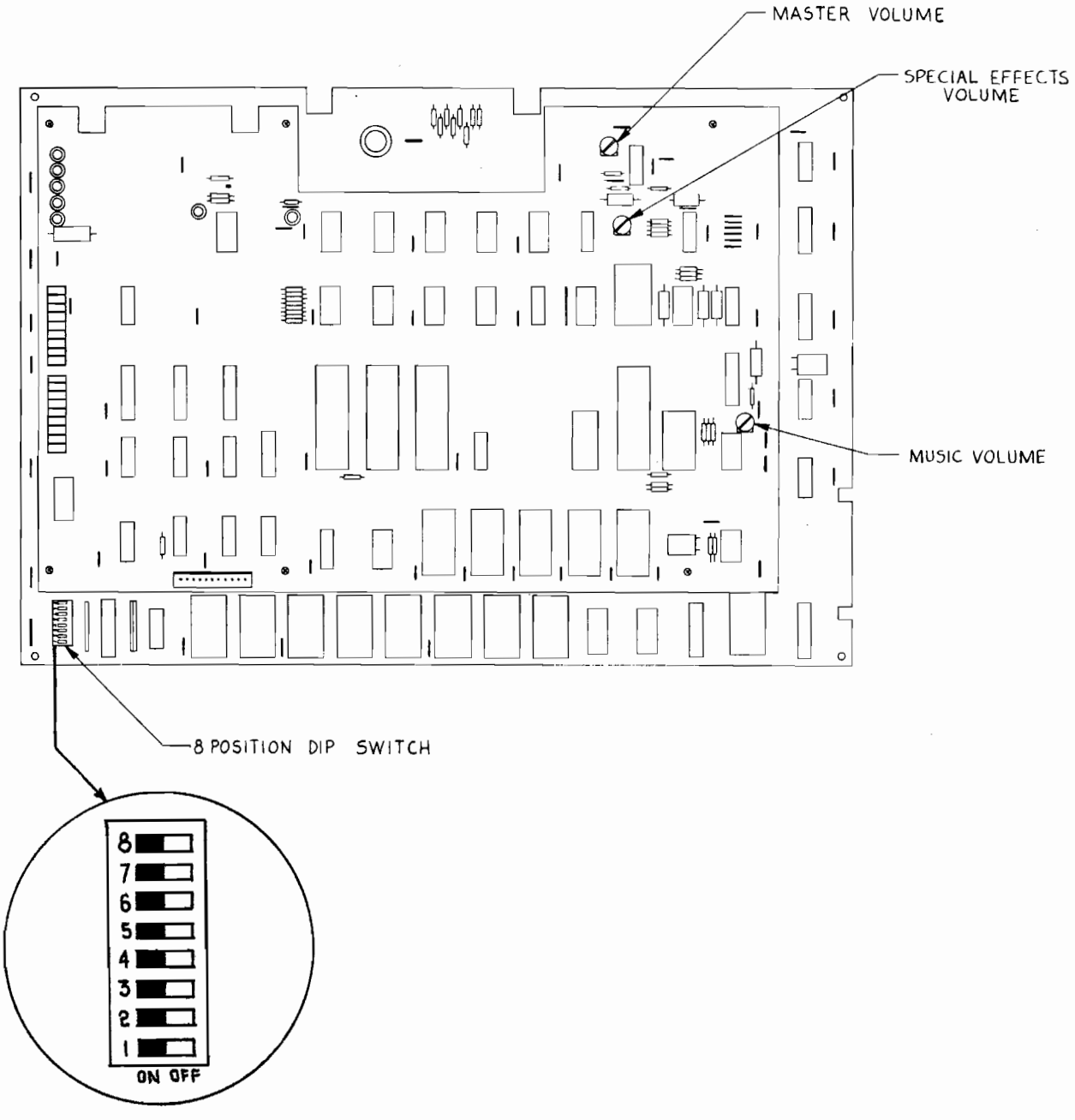
CAUTION: Only certified technicians should make adjustments on all components of FAX™. Only the +5v DC is adjustable. This must be adjusted to:

+5.00v DC +/- .1v

as measured on the Main Logic PCB near the 6502 Microprocessor (location 2A).

2. Audio Board Adjustments

The following drawing points out the three individual audio adjustments and the location of the DIP switch. The audio board rides piggyback on the logic board, mounted on the back wall of the game.



3. Operator Selectable Options

FAX™ has several switch selectable options controlled by an 8-position DIP switch located on the main logic board at position 16A. This switch is accessible through the left front door of the game.

FAX™ is shipped with the DIP switch already set for optimum dollar return, that is 48 seconds game clock 3:12 play time with 36 seconds bonus clock time at 13,000 point level. Actual game time play for the average player will be aproximately 2 to 4 times the game clock time as the game clock (bottom of screen) starts and stops at various times throughout the play of a game. The game clock starts when the answer to the first question appears on the screen, and stops when a player (both players in a two player game) selects an answer, right or wrong. This sequence is repeated for all questions. Should you decide to change the settings, you may select any of the following options by setting the proper switches accordingly:

	a. COINAGE	Switch 4	Switch 5	Switch 8
F/S	**1 Coin - 1 Credit**	**OFF**	**OFF**	**OFF**
	2 Coins - 1 Credit	OFF	ON	OFF
	1 Coin - 2 Credits	ON	OFF	OFF
	1 Coin - 4 Credits	ON	ON	OFF
	1 Coin - 3 Credits OR 2 Coins - 7 Credits	OFF	ON	ON
	1 Coin in Left Slot- 1 Credit, 1 Coin in Right Slot- 5 Credits*	OFF	OFF	ON
	1 Coin in Left Slot- 1 Credit, 1 Coin in Right Slot- 4 Credits*	ON	OFF	ON
	2 Coins in Left Slot- 1 Credit,1 Coin in Right Slot- 3 Credits*	ON	ON	ON

	b. GAME TIMES Game Clock Time	Approx. Play Time	Bonus Time	Switch 6	Switch 7
	:32	2:Ø8	:24	OFF	OFF
F/S	**:48**	**3:12**	**:36**	**ON**	**OFF**
	1:Ø4	4:16	:48	OFF	ON
	1:12	4:48	1:Ø4	ON	ON

	c. BONUS TIME (Extra time awarded when selectable number of points are made. Maximum of 2).	Switch 2	Switch 3
	8,ØØØ	OFF	OFF
F/S	**13,ØØØ**	**ON**	**OFF**
	18,ØØØ	OFF	ON
	25,ØØØ	ON	ON

* Requires dual harness.
F/S=factory setting.
switch 1 is not used adn should be off.

FREEPLAY: For those wishing to demonstrate FAX™, a freeplay mode may be achieved by turning switches 2 through 8 ON.

II. MODES OF OPERATION

A. AUTOMATIC SELF-TEST MODE

FAX™ automatically tests the logic data and audio boards on power up. To run the Control and Color Test, activate the coin switch while powering up.

You may bypass both diagnostic modes by depressing either the one or two player start button while powering up. After 8 seconds of the message "STAND BY VERSION X", (where X is a number representing the software version) the Attract Mode appears.

1. LOGIC DIAGNOSTIC TESTS

a. The RAM Test

When FAX™ is first turned on, a processor and video RAM test are done. If the RAM passes, it goes immediately into the EPROM test, without a message indicating it passed the RAM test.

If a RAM chip fails, an attempt is made to indicate the RAM chip where a failure was detected. Since the screen depends on a properly functioning RAM, this indication may not be displayed. A failed RAM may be indicated by a digit from Ø to 3 in every position on the screen. The code for these digits is as follows:

Number on Screen	RAM chip to check on logic board	Number on Screen	Location on Plane Interface board
Ø	4A,5A (2114)	3	U1 (6116)
1	7B,8B (2114)		
2	9C (6116)		

The RAM test cycles if the failure is persistent

b. The EPROM Test

If the RAM test passes, the EPROM test begins. The message "PROGRAM EPROM CRC TEST" first appears on the screen to indicate the FAX™ program logic Eproms are been tested. One by one, "X"`s appear on the screen. Each X indicates half of a 2732 EPROM, in locations 13A through 6A, on the logic board has passed the diagnostic test. Note that each EPROM is represented by two X`s. To indicate the FAX™ Questions and Answer Data Eprom`s are been tested. After 16 X`s appear the message "DATA EPROM CHECKSUM TEST" appears on the screen. Again X`s will appear to indicate 2764 EPROMS in locations 1C through 8C, 1B through 8B and 1A through 8A on the MEMORY EXPANSION & I/O BOARD*, have passed the diagnostic test. Each EPROM is represented by one X with the first X assigned to 1C and the last to 8A.

If any failure is detected during the EPROM test, an alpha/numerical digit appears instead of "X" with a "BAD EPROM" message. The key for which chip to check is as follows:

DATA EPROM CHECKSUM TEST

Ø 1 2 3 4 5 6 7 8 9 A B C D E F G H I J K L M N

1C 3C 5C 7C 1B 3B 5B 7B 1A 3A 5A 7A
2C 4C 6C 8C 2B 4B 6B 8B 2A 4A 6A 8A

PROGRAM EPROM CRC TEST

Ø1 23 45 67 89 AB CD EF
13A 12A 11A 1ØA 9A 8A 7A 6A

*NOTE: All locations may not be filled depending on the amount of memory required. (I.E. 7A and 8A are presently empty.)

2. AUDIO DIAGNOSTIC TESTS

While the Logic Board tests are underway, the Audio board is also being checked.

Five seconds after power on, one or more quick beeps, like an organ chord, are heard. This is part of the Exidy Audio Diagnostic Test. The number of beeps that sound indicate different conditions of the Audio board. The following code is an indication **only**, of where to first check the Audio Board. Because this diagnostic test only evaluates certain components, other circuitry is relied upon for the test. Should this other circuitry fail, the diagnostic test may not, then, point directly to the failure. Please use the results of this test as a guideline for further troubleshooting.

The code is as follows:

Ø beep: If no beeps are heard, along with a hum or random notes, this may indicate a failure in 3A and/or 7A, or volume control have been turned off.

1 beep: All audio hardware is OK. However, be sure to check the Attract Mode Cycle for a possible message to check the Audio Board. In occasional instances, this can occur. The message will further direct you.

2 beeps: ZERO PAGE RAM failure. Check 6532 RAM I.O. Timer Array at location 7B on the audio board.

3 beeps: (will not occur)

4 beeps: ROM failure

5 beeps: INTERRUPT failure. Check 6532 at location 7B.

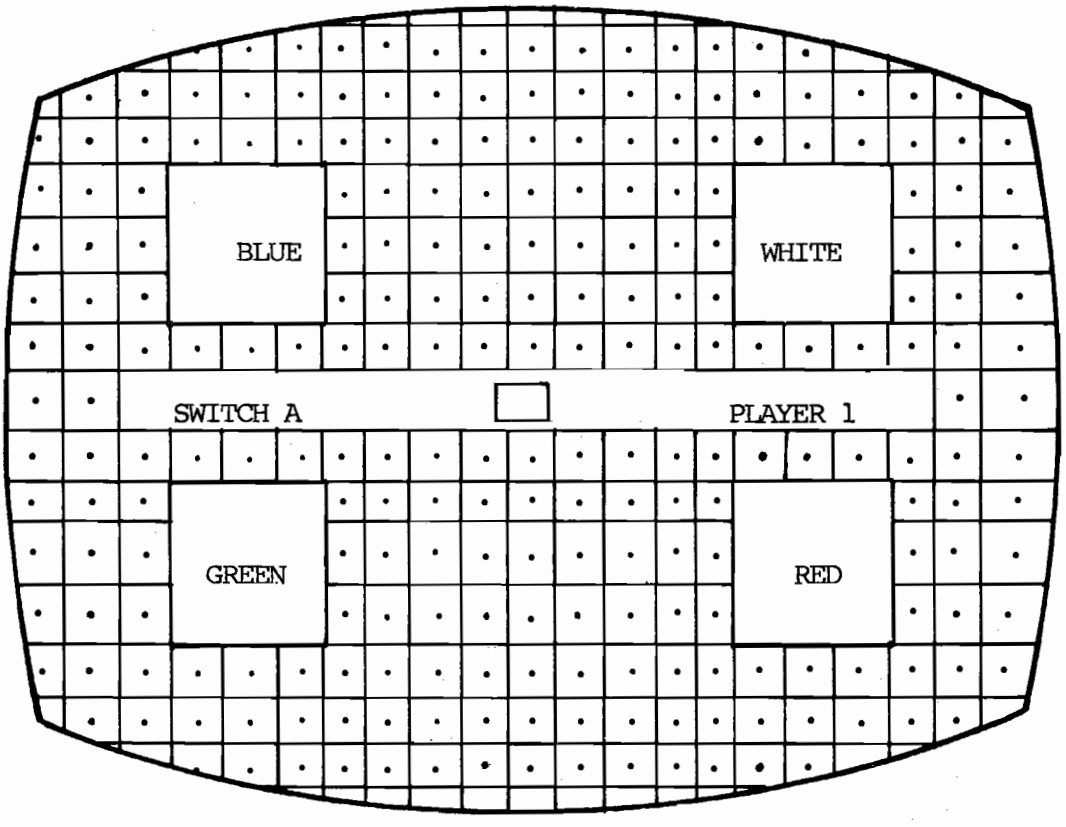
In addition, this message appears during the Attract Mode **only** if the Audio Board needs to be checked:

"AUDIO COMM ERROR"
or
"TEST ERROR"

3. CONTROL AND COLOR DIAGNOSTIC TESTS

If desired, you may test all player controls and screen colors for monitor adjustments To do so, activate either coin switch at power-up. The game then enters the Control/Color Test Mode. This mode lasts for 1ØØ seconds to give you time to test and make adjustments. After that, the Attract Mode begins.

In the Control/Color Test Mode, the screen shows this pattern:



The grid pattern tests your screen for any distortion or convergence.

The solid blocks of color (blue, white, green, and red) allow you to adjust the color. When either of the player control buttons (one player or two player) or coin switches (coin 1 coin 2) are activated, their name appears below the blue box. When any of the lettered answer buttons ("A" through "D" for player 1 or 2) are activated, their name appears below the blue and white boxes.

B. THE ATTRACT MODE

After FAX™ goes through its automatic self-diagnostic test mode on power-up, a series of screen displays are shown repeatedly. The first screen identifies the game and manufacturer, along with credit information. The second screen gives game instructions. The third screen is the dean's list, with the initials and scores of the eight highest scoring players.

The final screen shows the comparative progress display. The cycle then repeats.

C. GAME PLAY MODE

FAX™ is a timed trivia game of multiple choice, YES/NO, and TRUE/FALSE questions for either one or two players. Naturally the object of the game is to correctly answer as many questions as possible and score as many points as possible. A player first selects one of the four categories and the difficulty level (choice of three). After each question appears on the screen, the possible answers will appear directly below. The player only has one chance to answer the question. He cannot change is mind once an answer is chosen. The quicker a question is answered correctly, the more points are scored. The game is played until time runs out. Bonus time is awarded for high scores. In a two player game both players play simultaneusly and the first correct answer wins the points.

D. VANITY MODE

Anytime a player's score exceeds one of the fifty current high scores, he is eligible to enter his initials in the Vanity Table. Only the top eight scores will be displayed in the Attract Mode. If both players of a two player game are record high scorers, the higher of the two is first invited to enter his initials. To do so, he uses the A thru D buttons. Use the "A" or "B" button to run the alphabet letters up or down respectively. Once the desired letter appears enter it in by depressing either the "C" or "D" buttons. The game will return to the Attract Mode either after all the initials have been entered or after approximately 1ØØ seconds have elapsed.

APPENDIX A: SCHEMATICS

PAGE 1, GAME LOGIC PCB

1. Master Oscillator (1D)

From this oscillator all dynamic operations are derived, such as the processor clock, the main element and line counters, the shift register clocks, as well as all other forms of timing signals.

2. Element (Horizontal) Counters (1C, 1E, 2E)

These components form the final stages of horizontal timing. All operations in this game requiring horizontal positioning or timing have their origin here. Note that, beginning with signal HCLK (from Clock Divide Counter 2D), there are 256 counts prior to setting signal E256 high. When this signal goes high, it indicates that the horizontal blanking period is in progress. At this time the final counter (1E) is preloaded with a higher number than previously loaded. This creates a shorter count the second time around. The shorter count measures the retrace interval. When the retrace count is finished, the counter preloads with a lower number, establishing a longer count sequence again for "real time" sweep of the electron beam across the face of the CRT.

3. Line (Vertical) Counters (4F, 5F, 6E)

These components form the entire vertical timing operation starting with a clock derived from horizontal timing. These counters count 256 times and then preload with a higher number, causing a shorter count the second time. This shorter count measures the vertical retrace interval. Note that signal L256, when high, indicates vertical blanking is in progress. After the completion of the vertical retrace count, the counters once again preload with a lower number. This way they count 256 times during the sweep of the electron beam down the face of the CRT, allowing the horizontal timers to sweep one complete horizontal line for each count of the vertical counters. Thus, the electron beam reaches the bottom of the CRT, after completing 256 horizontal line sweeps. It then begins the vertical retrace count, and the whole cycle begins anew with the beam starting again at the top of the CRT.

4. Screen RAM Addresses (7D)

During the time the screen RAM is examined by the logic for output to the monitor screen, addresses must be applied to the screen RAM to count up at a rate corresponding to the image cells conceptually arranged on the screen in a 32 x 32 matrix. The counts used here, 4 from the element counters, and 4 from the line counters, fulfill this timing requirement. The least significant element count used (E8) represents an interval exactly eight times that of one element. The least significant line count used represents an interval exactly eight times that of one horizontal line, or eight times a single line count. Dividing a 256 element line by 8 yields 32, and likewise dividing a 256 line vertical sweep by 8 yields 32. Thus the screen RAM address lines (RAMØ through RAM9) count at a rate that creates 32 horizontal counts and 32 vertical counts as the electron beam sweeps the face of the CRT. This makes 1Ø24 conceptual "image cells" into which can then be inserted images of 8 elements by 8 lines. For more information concerning these images, refer to the text for pages 2 and 3 of the Logic Schematics.

5. Coin Input Decoding (1H)

Some models of FAX™ contain two separate coin inputs for special coinage applications. NOR gate 1H combines these separate inputs, making signal 5COINT, which sets the interrupt flip-flop (6E on page 8) when either coin input becomes active, thus forcing the microprocessor to jump to the interrupt service routine. This interrupt driven operation prevents ever missing a coin when inserted. However, this also means that when a game is first powered up, the coin input must be inactive. If for some reason the coin input switch is enabled at the time of power up, the game comes up with test pattern ilustrated in page 9.

6. Blanking and Video Clocking (5H)

Flip-flop 5H merely combines blanking and all other video.

1. Screen Controller PROM (6D)

This PROM controls the direction of data flow into and out of the screen RAM and character generator RAM. It prevents timing errors and buss conflicts, assuring that the microprocessor can write to either the screen or character generator RAM, or read back from either.

2. Screen RAM (7B, 8B)

The screen RAM is comprised of two 1Ø24 x 4 static RAMs, configured to act as a single 1Ø24 x 8 RAM. This creates a screen matrix of 32 horizontal by 32 vertical positions. A single byte code is stored in each of these positions to represent a particular character. During "real time" (the time the CRT is being swept by the electron beam) these character codes address the character generator RAM.

These character codes, when used as addresses, are combined with the three least significant line counts (L1, L2, L4) to present to the character generator output shift register all the necessary data to form an 8 element wide by 8 line high character on the CRT, located within one of the 1Ø24 positions mentioned immediately above; that is, the 32 horizontal by 32 vertical positions.

The screen, then, is a storage place for single byte codes that call up an 8 x 8 character and place it into the corresponding character cell. This character is stored in the character generator RAM, shown on page 3 of the schematic.

3. Character Image Storage

Shown on this page are two PROMs (9C, 1ØC). They could be used as a permanent set of characters. However, FAX™ uses RAM instead, to increase the flexibility in character manipulation. This portion of RAM appears on page 3 of the Logic schematics.

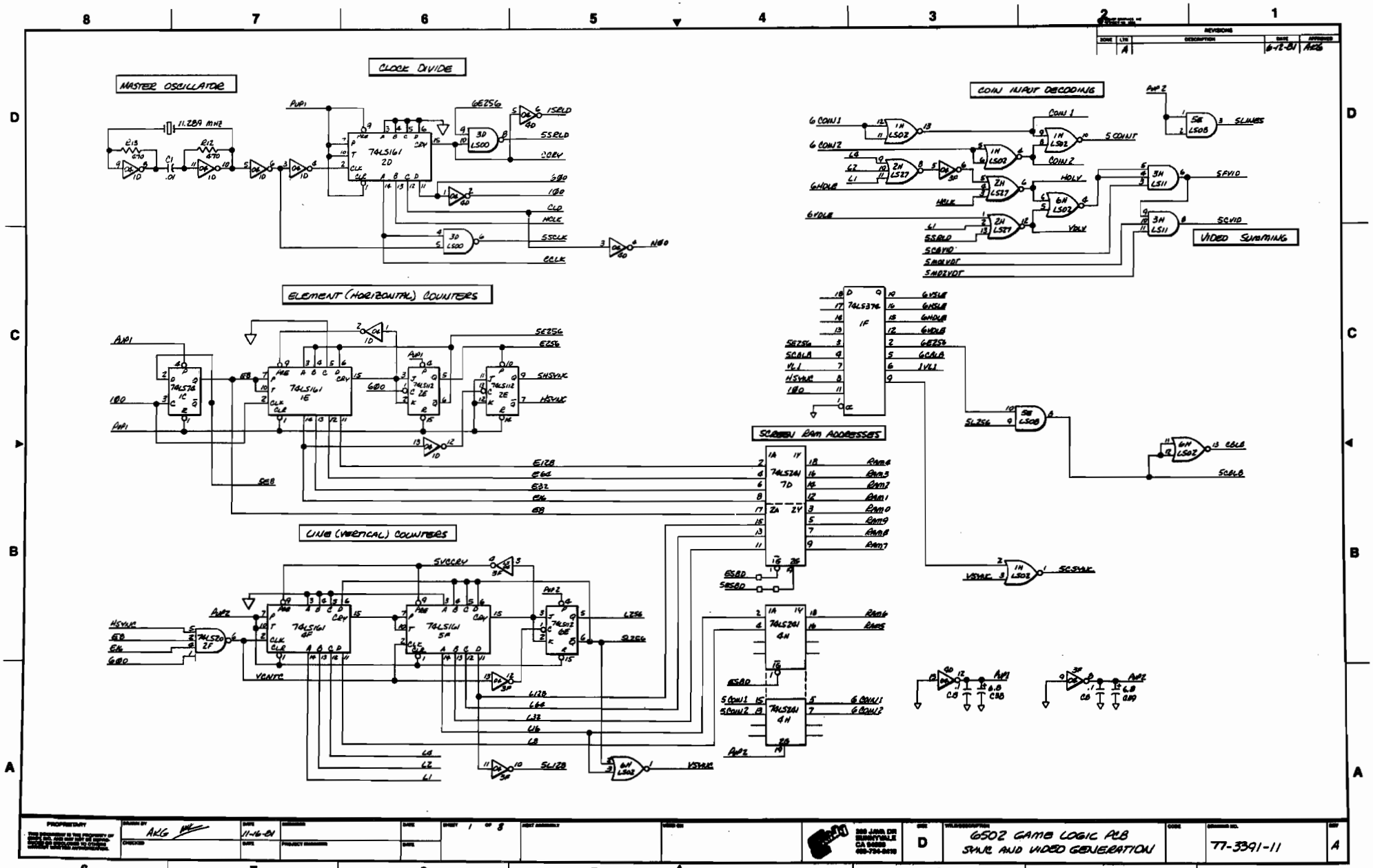
4. PROM Power and Signal Selection (1ØB)

This Dip Shunt configures the logic for different types of PROM devices. For FAX™, however, this Dip Shunt is unnecessary due to the fact that RAM has been used rather than PROM.

5. Character Generator Output Shift Register (12B)

Video from the character generator memory devices (RAM in the case of FAX™) is formed by this shift register as a byte of data that displays one line at a time from left to right on the CRT. This ultimately forms an 8 line high by 8 element wide character positioned on the screen according to the time it is presented to the shift register.

Output from this shift register are all the images seen on the screen except the lower body of the characters climbing the ladders.


MASTER OSCILLATOR
CLOCK DIVIDE
COIN INPUT DECODING
VIDEO SUMMING
ELEMENT (HORIZONTAL) COUNTERS
SCREEN RAM ADDRESSES
LINE (VERTICAL) COUNTERS
11.289 MHZ
74LS161 2D
74LS161 1E
74LS161 4F
74LS161 5F
74LS374 1F
74LS241 7D
74LS241 4H
74LS20 2F
74LS112 2E
74LS112 6E
6E256
1SRLD
5SRLD
CCRY
6Ø0
1Ø0
CLD
HCLK
5SCLK
CCLK
NØ0
6 COIN1
6 COIN2
6HDLE
6VDLE
5 COINT
HOLY
VOLY
5FVID
5CVID
5SRLD
5CBVID
5MD1VDT
5MD2VDT
SLINES
6VSLE
6HSLE
6HDLE
6VDLE
6E256
6CBLB
1VL1
SE256
SCBLB
VL1
HSYNC
1Ø0
SL256
CBLB
SCBLB
SCSYNC
VSYNC
E128
E64
E32
E16
E8
SE8
SHSYNC
HSYNC
SVCCRY
VCNTC
L256
SL256
L128
L64
L32
L16
L8
L4
L2
L1
SL128
VSYNC
ESBD
SESBD
RAM4
RAM3
RAM2
RAM1
RAM0
RAM9
RAM8
RAM7
RAM6
RAM5
5 COIN1
5 COIN2
6 COIN1
6 COIN2
PUP1
PUP2
PROPRIETARY
DRAWN BY AKG
DATE 11-16-81
SHEET 1 OF 8
D
6502 GAME LOGIC PCB
SYNC AND VIDEO GENERATION
77-3391-11
A

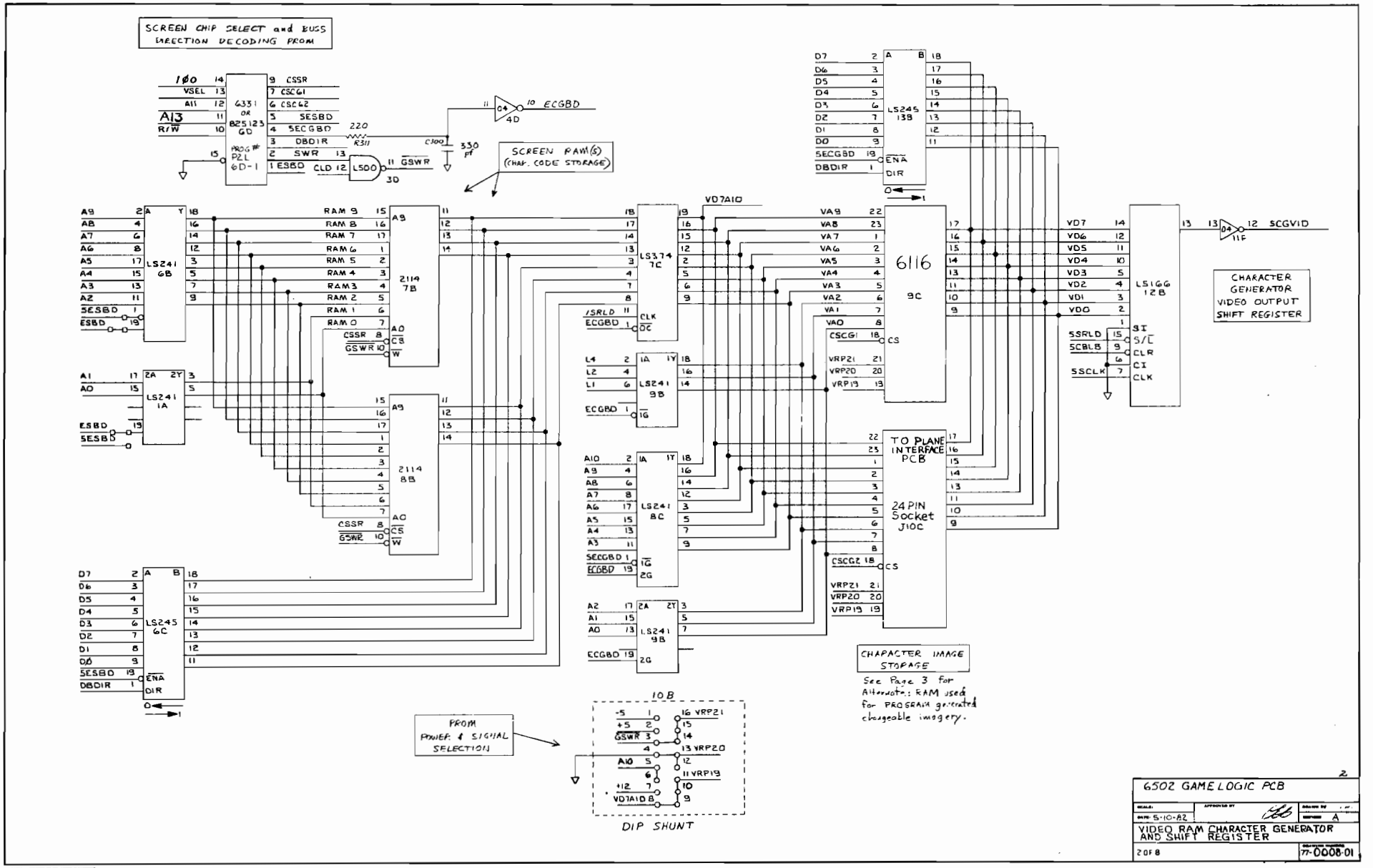
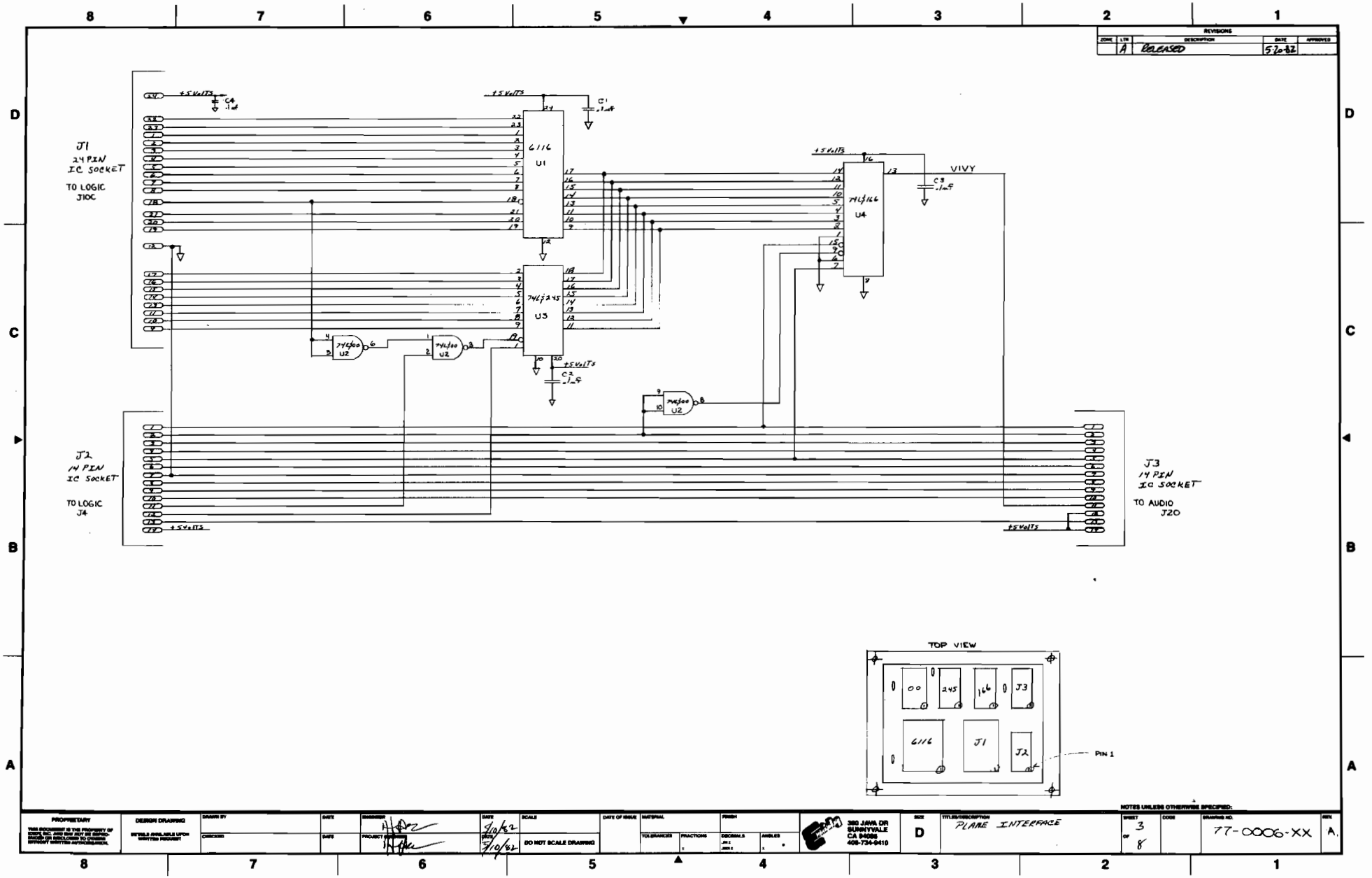

SCREEN CHIP SELECT and BUSS DIRECTION DECODING PROM
SCREEN RAM(S) (CHAR. CODE STORAGE)
CHARACTER GENERATOR VIDEO OUTPUT SHIFT REGISTER
CHARACTER IMAGE STORAGE
See Page 3 for Alternate: RAM used for PROGRAM generated changeable imagery.
TO PLANE INTERFACE PCB
24 PIN Socket J10C
PROM POWER & SIGNAL SELECTION
DIP SHUNT
6502 GAME LOGIC PCB
VIDEO RAM CHARACTER GENERATOR AND SHIFT REGISTER
2 OF 8
77-0008-01
DATE: 5-10-82
A

Image Storage RAM

1. Character Generator Image Storage RAM and Plane Interface Board (9C, U1)

These two RAMs, when used in this configuration, act as a 4096 x 8 bit RAM. The two color images placed on the screen are stored in this RAM by the microprocessor, according to the game program. In this RAM images are established, altered, shifted slightly, and even replaced with a new set, if required by the program.

When called by the logic to do so, the RAM presents, to the character generator shift register, a single byte, representing one line of a particular image. Each image is composed of 8 lines of data, each line is one byte-wide. Thus, 256 images of 8 x 8 bits can be stored here simultaneously and "called up" by the screen RAM to be displayed on the CRT in any of the 1024 character cell positions. A single byte code, stored in the screen RAM, calls up a character. The character may change or move by replacing the single byte code in the screen RAM, or by altering the data in the character generator RAM which forms the image.


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | RELEASED | 5-20-82
J1
24 PIN
IC SOCKET
TO LOGIC
J10C
+5 Volts
C4
.1uf
6116
U1
C1
.1uf
74LS245
U3
74LS00
U2
C2
.1uf
74LS166
U4
C3
.1uf
VIVY
J2
14 PIN
IC SOCKET
TO LOGIC
J4
J3
14 PIN
IC SOCKET
TO AUDIO
J20
TOP VIEW
00
245
166
J3
6116
J1
J2
PIN 1
NOTES UNLESS OTHERWISE SPECIFIED:
PROPRIETARY
DESIGN DRAWING
DRAWN BY
CHECKED
DATE
ENGINEER
PROJECT ENGINEER
DATE 5/10/82
SCALE
DO NOT SCALE DRAWING
DATE OF ISSUE
MATERIAL
TOLERANCES
FRACTIONS
FINISH
DECIMALS
ANGLES
360 JAVA DR
SUNNYVALE
CA 94086
408-734-9410
SIZE
D
TITLE/DESCRIPTION
PLANE INTERFACE
SHEET 3 OF 8
CODE
DRAWING NO.
77-0006-XX
REV
A

PAGE 4, GAME LOGIC PCB

1. The 6502 Microprocessor (2A)

For detailed information concerning this microprocessor, refer to the MOSTEK publication, 6500-10A, MCS Microcomputer Family Hardware Manual.

One feature that should be mentioned here, however, is that this microprocessor has "memory-mapped I/O". This means that all ports interfacing to peripherals of any type must be located within the normal memory map, with no duplication of addresses, since no instructions are specifically oriented toward I/O operations.

2. Power-on Reset circuit (connected to 2A pin 40)

When power is first applied to a game, a particular sequence of events must occur to set up all logic conditions. If this sequence is broken for whatever reason, the microprocessor may become confused, and the game will not start and run.

This sequence is accomplished when the reset line to the microprocessor is the last line allowed to reach a "high" logic level. The Power-on reset circuit makes sure this occurs by utilizing the charge time of an RC network as a delay.

If any kind of power interruption occurs during normal game play, the power-on reset circuit insures that the microprocessor is reset. This alleviates confusing the microprocessor, while it also recreates the original power-on sequence.

3. Processor Workspace RAM (4A, 5A)

The RAM, or workspace, consists of the lowest 1024 bytes of memory and can be divided into three separate sections due to distinctly different functions.

The lowest 256 bytes (0 to FF Hexadecimal) is reserved for special software register operations, and is called "zero page". The processor uses this area to store dynamic variables. For details of this type of operation, refer to 6502 technical literature regarding "Zero Page Addressing".

The next higher 256 bytes (100 to 1FF Hex) is reserved for the 6502 stack. The processor stores return addresses in the stack when interrupted or called to execute a subroutine. The game program may also request the processor to store other kinds of information here for later retrieval.

The next higher 512 bytes (200 to 3FF Hex) are used as a scratchpad area. Miscellaneous calculations and their results are temporarily stored here. If an error in this RAM occurs, the screen will not retain the condition that existed prior to losing the last turn, or between players.

4. Main Address Decoding (5C, 5D, 5E)

This circuit is the first stage of the address line decoding necessary to organize the memory map; that is, it places specific functions or devices within generalized blocks of the memory map, grouped by function.

1. Program Memory (6A through 13A)

These memory devices are 2732 EPROMS. Note that four of the lines to each memory device (PCS0 through PCS7, PAP19, PAP20, PAP21) are programmable through jumper configurations located at 4B and 11B. This allows different memory devices to be used and/or facilitates interconnection to the memory expansion PCB (if used).

2. PROM Address Selection (4B, 5B)

This is a second stage of address decoding, used to select each individual memory device when addressed. Signal ROMSEL (from page 4 Main Address Decoding) selects the Program Memory devices in general, and jumper 4B, together with decoder 5B further defines an address to a particular memory device.

3. Memory Device "Personality" Selection (11B)

The dip shunt, or jumpers block, alters control signal configuration to the program memory devices. This allows the use of alternate size EPROMS and/or those created by different manufacturers whose control signal pinouts may not be identical to one another.

PAGE 6, GAME LOGIC PCB

1. Moving Object Horizontal Position Counters (13F, 15F, 14F, 16F)

Counters 13F and 15F form a byte-wide counter which horizontally positions Moving Object 1 on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of the Horizontal Sync, they begin to count. The count outputs AND'ed through 15E give rise to signal M1HW, the Horizontal Position Window for Moving Object 1. Counters 14F and 16F are the equivalent circuit for Moving Object 2.

2. Moving Object Vertical Position Counters (16E, 12E, 1E, 13E)

Counters 16E and 12E form a byte-wide counter which positions Moving Object 1 vertically on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of Vertical sync, they begin counting. The four count outputs of the least significant of these two counters (M1L1, M1L2, M1L3, M1L4) are sent to the moving object image PROM to specify which line of the image is presently being displayed. The AND'ed outputs of the second counter give rise to signal M1VW, the Vertical Position Window for Moving Object 1. Counters 11E and 13E are the equivalent circuit for Moving Object 2.

3. "Write Moving Object" Decoding (6F, 16H, 5E, 3F)

Consists of two distinctly different functions. 6F and 16H form the circuit that generates the load pulses for the moving object position counters, while 5E and 3F simply prevent the counters from counting during blanking.

4. Color Interface Output (16B)

This is a 14 pin DIP socket used as the connector interface to the color selection circuitry, located on the audio PCB. The signals and their functions are listed below:

Pin #		
1	5SRLOAD	= Shift Register Load Pulse (Neg. True)
2	CBLB	= Composite Blanking
3	CSYNC	= Composite Sync
4	5CVID	= Composite Video (Neg. True)
5	5SCLK	= Shift Register CLock (Neg. True)
6	HSYNC	= Horizontal Sync
7	GND	
8	VSYNC	= Vertical Sync
9	5MO2VID	= Moving Object 2 Video (Neg. True)
10	5MO1VID	= Moving Object 1 Video (Neg. True)
11	DBDIR	= Character Generator Address Line 9
12	CSSR	= NOT USED ON FAX™
13	VD7A10	= Character Generator Address Line 10
14	+5V	

1. Moving Object Multiplexing (14A, 14E)

These two multiplexers pass information to the moving objects image PROM. They contain two codes: one determines which image should appear, and the other specifies which line of that image is to be displayed.

The data passed alternates between data for Moving Object 1 and Moving Object 2, depending on the state of element count E32.

The upper multiplexer (14A) passes the "which image" code, and the lower multiplexer (14E) passes the "which line of that image" code.

2. Moving Objects Image PROM (11D)

This EPROM accepts as an address the image and line codes of moving objects 1 and 2 (see "Moving Object Multiplexing" above). It then presents the appropriate data for one line of the image to the output shift registers.

The timing of the logic insures that the correct pair of shift registers are loaded with the data, then shifted out at the correct time to become, one line at a time, the 16 lines of video for that character (Moving Object 1 or 2).

3. Moving Object Video Output Shift Registers (12D, 13D, 14D, 15D)

Shift registers 12D and 13D together form a 16 bit shift register whose task is to accept, as data, 16 bits (2 bytes) representing a single line of the image for Moving Object 1, then shift these 16 parallel bits out serially to become video. This operation is repeated for 16 consecutive lines, resulting in a video image that is 16 bits wide by 16 lines high on the monitor screen.

Shift registers 14D and 15D together form this same type of circuit, identical in function, for Moving Object 2.

4. Moving Objects Shift Register Load Logic (2F, 16H)

This circuit sends properly timed load signals to the Moving Object Video Shift Registers. These load signals are needed to load the image data into the shift registers at locations 12D, 13D, 14D, and 15D.

5. Moving Object Shift Register Control Logic (15H, 14H)

The input signals to the upper two gates (15H) represent horizontal and vertical position "windows" for the two moving objects (for example, M1HW = Moving Object 1 Horizontal Window, M2VW = Moving Object 2 Vertical Window). These windows allow the Moving Object shift registers to shift only at the right time. This insures the image is generated at the correct position on the screen.

The lower 2 gates of 15H are, in HARD HAT™, used for later decoding in the color selection circuitry, located on the audio and color plane interface PCB's

6. Memory Device Personality Configuration (10D)

This is another Dip Shunt which reconfigures the PC board in order to use an EPROM (11D) of another type or manufacturer.

PAGE 8, GAME LOGIC PCB

1. Interrupt Status Latch (8E)

This latch is set when a coin is dropped or vertical sync occurs. When the latch is set, the CPU is interrupted; that is, signal IRQ goes low. This forces the CPU to jump to the interrupt service routine. The interrupt service routine instructs the CPU to check for a coin input, and then run a debounce routine on the coin bits of ports 9E or 15A, depending on which coin input bit was set at 8E.

If the CPU finds no coin input bit set at latch 8E, it will assume the Interrupt condition was caused by vertical sync. This tells the CPU that it should now jump to the routine that services the normal game play, and that the screen can now be updated with new data. The screen can only be updated during the vertical retrace interval.

2. Option Switch Port (15A)

This port provides input from the option dipswitch, at location 16A. Data from the dipswitch is gated onto the data buss and read by the CPU at game start. This allows such options as number of turns, coins per game, additional game versus extra turn, etc.

Note that one input of this port (labeled COIN 2) does not come from the switch. Instead, it comes from Coin Input 2, and is used for debouncing the auxiliary coin input switch.

3. Control Inputs Port (9E)

This port can provide up to 8 control imputs. For FAX™ only the coin 1 input is used. Data from this port is gated on to the data buss for examination by the CPU during the regular service routine (which is synchronized to the vertical interval).

The COIN1 input to this port is used for debouncing the standard coin input.

4. Moving Image Latch

Only the CPU can write to the moving image latch. This latch contains the code that specifies which image or images are presently being displayed by the hardware moving object circuitry.

5. Audio Board Port

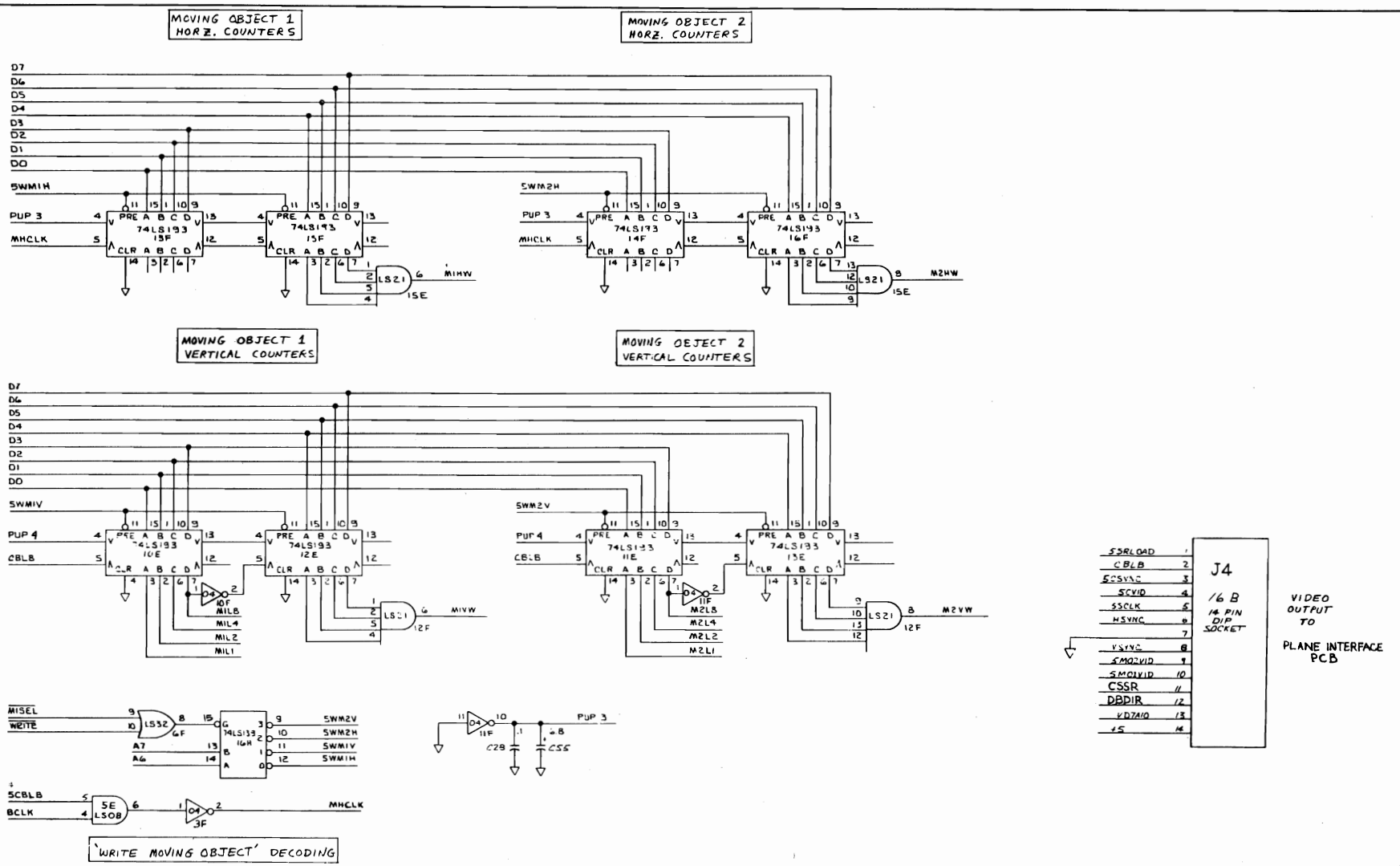
This latch is written to and read by the CPU, and transmits instructions to the audio board when any sounds are enabled, disabled, or the game is initialized. In addition, this port passes data sent to select colors for screen images. For the functions of these instructions, see the audio board schematic and/or description of operation.

6. Control Port Latch (9D)

This latch, used only in table versions, is written to only by the CPU and keeps track of which player is "up", in order to select which controls are active, that is, player one or player two.

7. I/O Decoding (7E)

The upper half of this decoder generates the chip selects for those I/O devices written to by the CPU, and the lower half generates the chip selects for those I/O devices which are read by the CPU. See the detailed memory map for more precise information.



'WRITE MOVING OBJECT' DECODING

6

6502 GAME LOGIC PCB

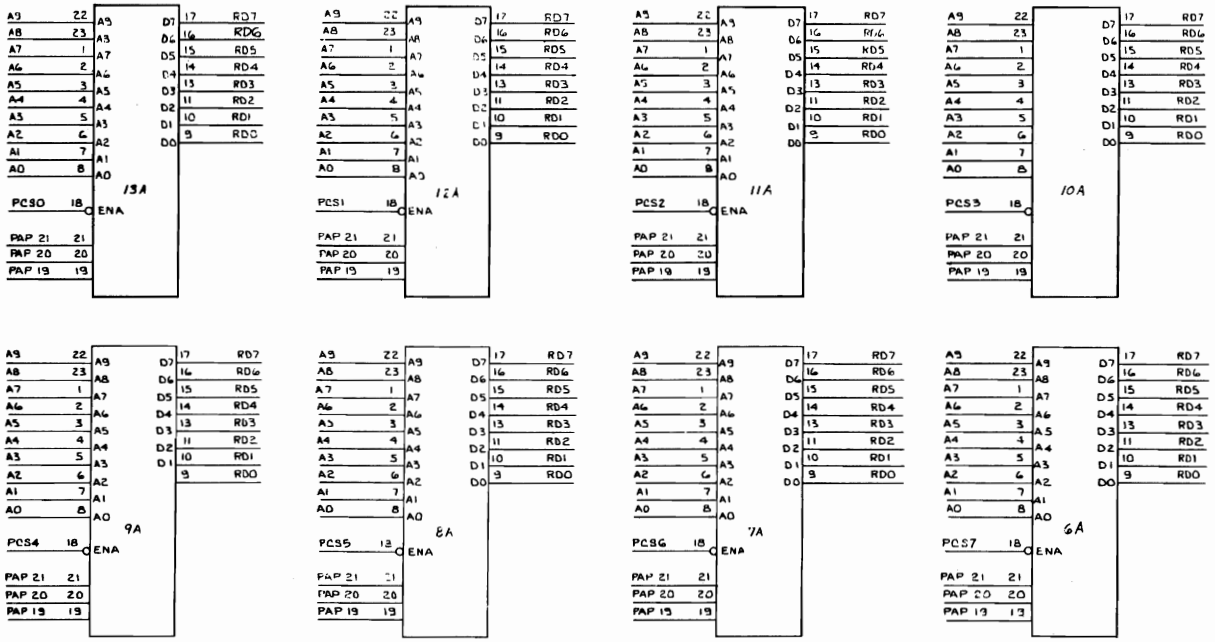
COLOR INTERFACE OUTPUT AND MOVING OBJECT POSITION COUNTERS

6 OF 8

77-0008-01

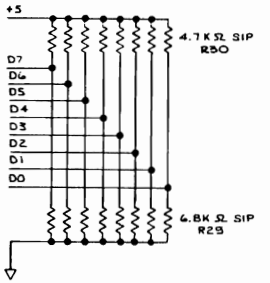
PROGRAM MEMORY

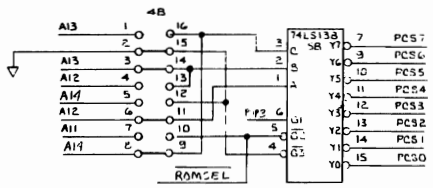
See TECHNICAL MANUAL For PROGRAM #'s.



DATA BUSS TERMINATION

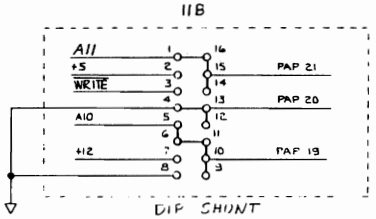
Ringing Suppression





PROM ADDRESS SELECTION

Configuration Shown is for +5V ONLY 2732 EPROMS. See TECHNICAL MANUAL For configuration for other memory devices.



MEMORY DEVICE PERSONALITY SELECTION

Configuration shown is for +5V ONLY 2732 EPROMS. See TECHNICAL MANUAL for configuration for other memory devices.

EXIDY INC.

SCALE:	APPROVED BY:	DRAWN BY
DATE 5-10-82		REVISION A

6502 GAME LOGIC PCB
CPU ROM

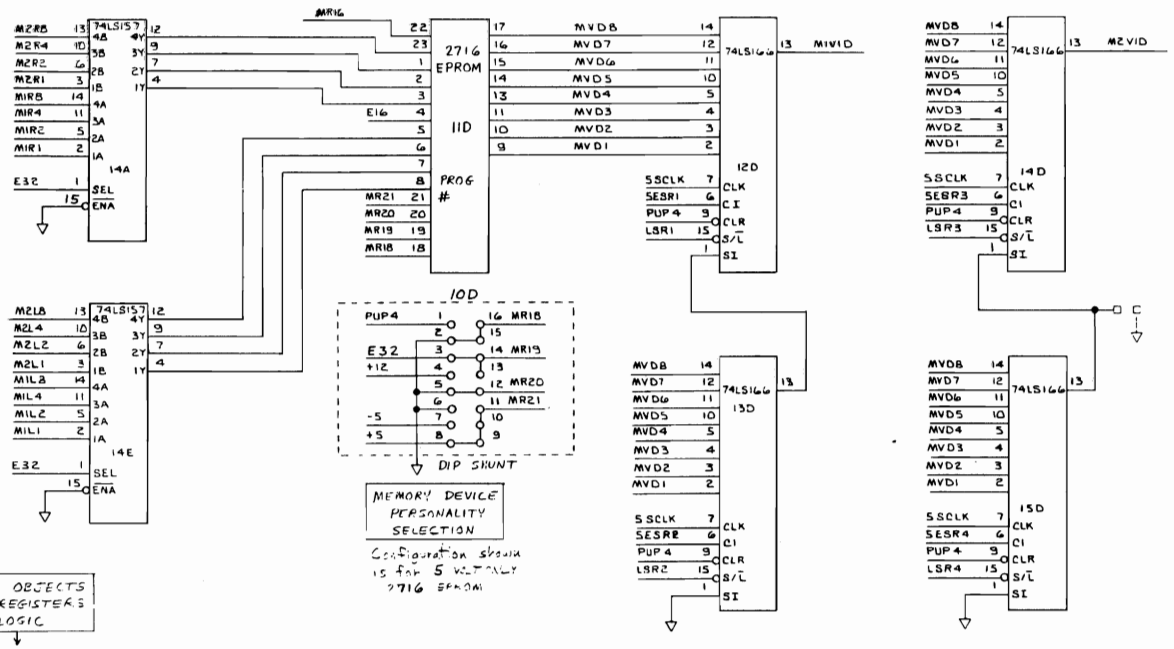
50F8	DRAWING NUMBER 77-0008-01

MOVING OBJECTS MULTIPLEXING

MOVING OBJECTS IMAGE STORAGE

MOVING OBJECT 1 VIDEO OUTPUT SHIFT REGISTER

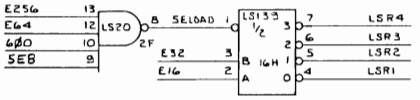
MOVING OBJECT 2 VIDEO OUTPUT SHIFT REGISTER



MEMORY DEVICE PERSONALITY SELECTION

Configuration shown is for 5 voltage 2716 EPROM

MOVING OBJECTS SHIFT REGISTERS LOAD LOGIC



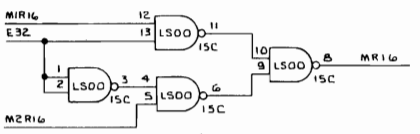
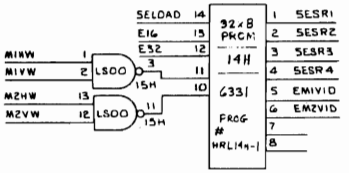
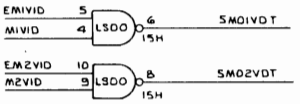
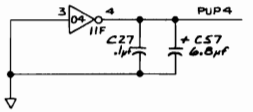


IMAGE SELECTION LOGIC
(Which Moving Object?)



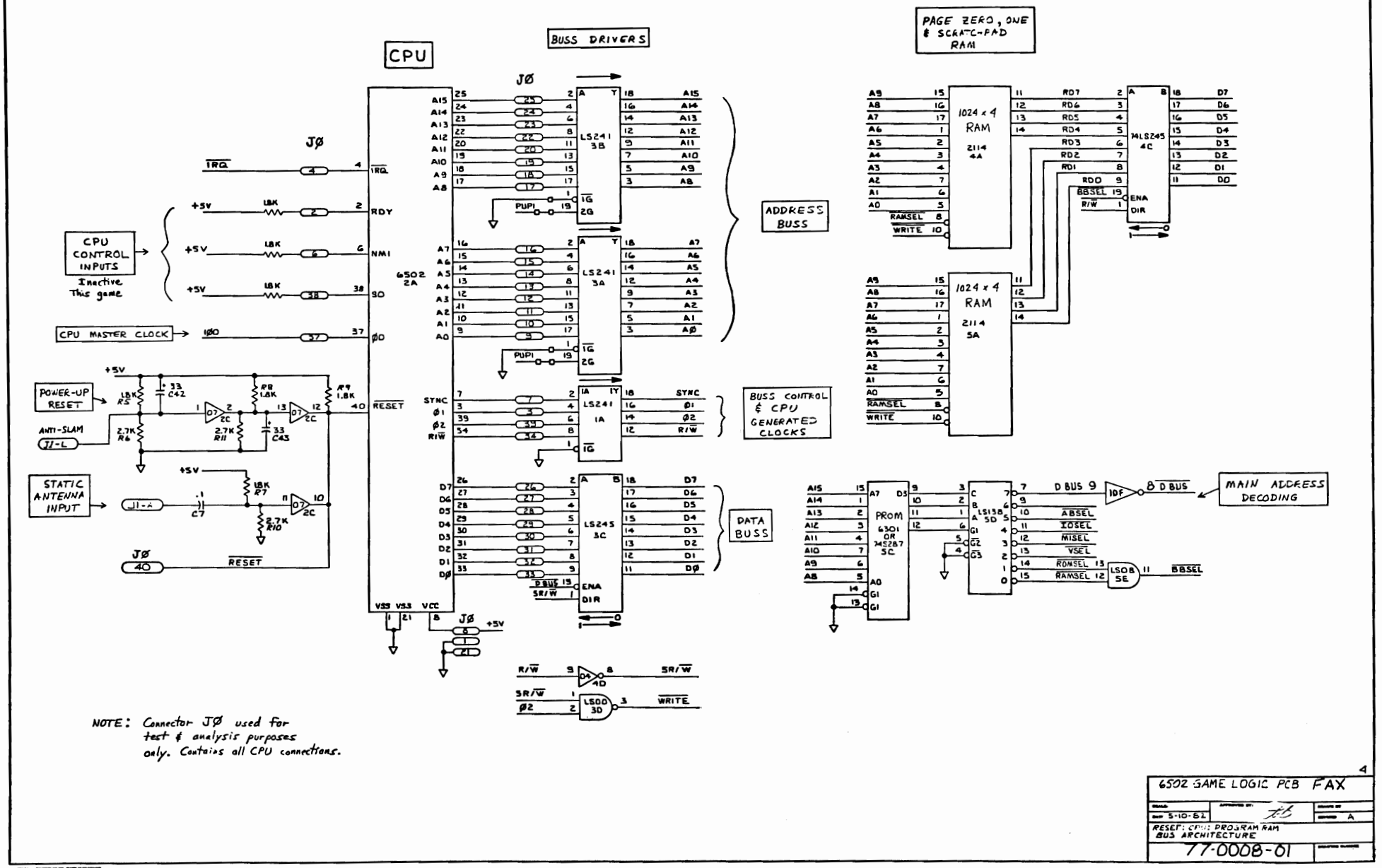


MOVING OBJECTS SHIFT REGISTER CONTROL LOGIC



7

6502 GAME LOGIC PCB	
SCALE	APPROVED BY
DATE 5-10-82	DRAWN BY
	DEPTH A
MOVING OBJECT VIDEO GENERATION	
7 OF 8	77-0008-01



NOTE: Connector JØ used for test & analysis purposes only. Contains all CPU connections.

4

6502 GAME LOGIC PCB FAX		
DRAWN	APPROVED BY:	SHEET OF
DATE 5-10-82		REVISION A
RESET; CPU; PROGRAM RAM BUS ARCHITECTURE		
77-0008-01		DRAWING NUMBER

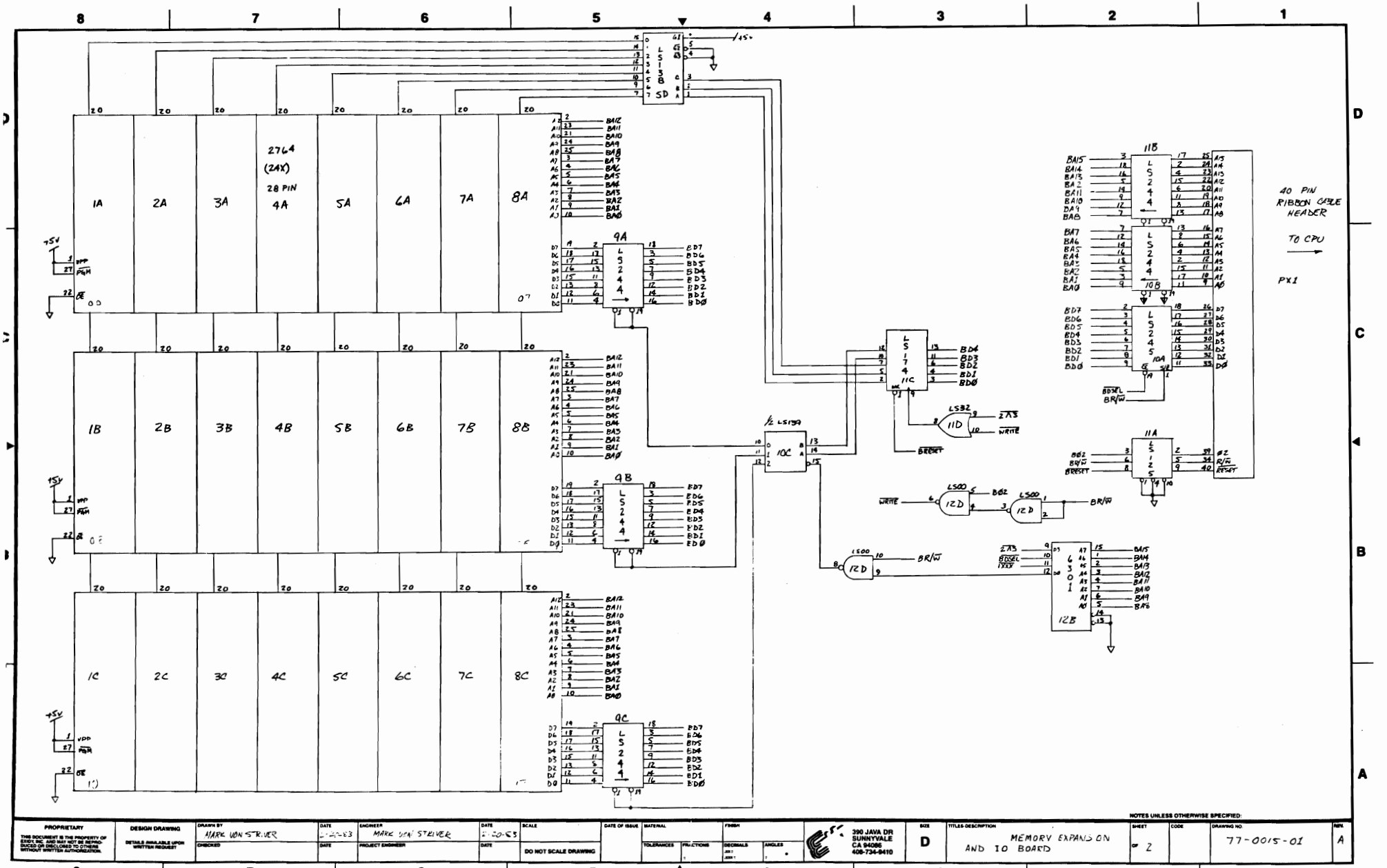
MEMORY EXPANSION AND I/O BOARD

The FAX™ Memory Expansion and I/O Board serves two purposes.

The first is to allow the CPU access to large amounts of data required because of the large number of questions that FAX™ contains (3500 - 4000). The board can hold up to 24 8K byte chip's. The total capacity of the board is therefore 192KB. The CPU can access only one Eprom at a time. The contents of the latch at 11C determines which Eprom resides in the CPU's memory map at any given point in time.

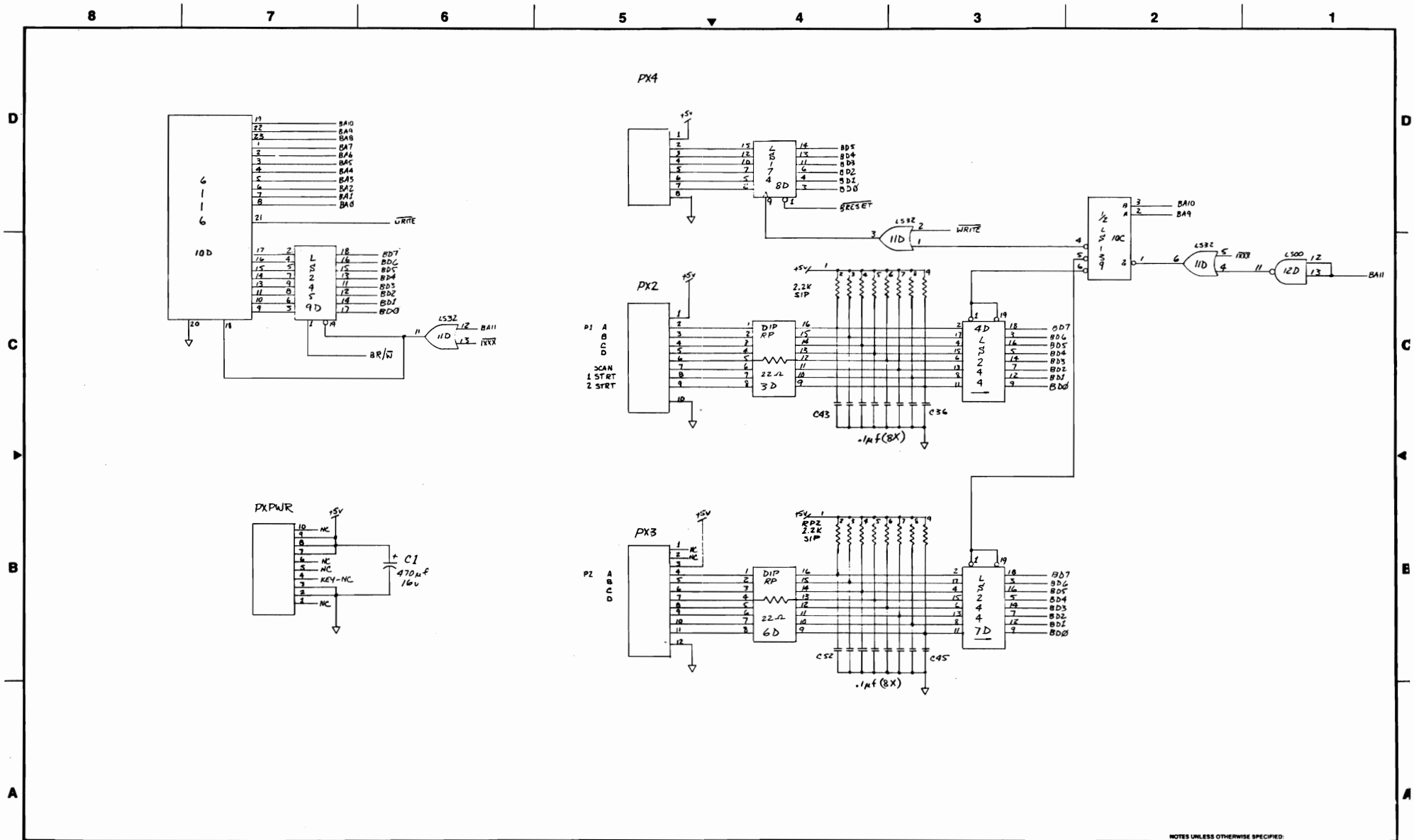
The second function is to provide a mechanism to allow the CPU access to control panel information consisting of "A" through "D" buttons for both player 1 and player 2 as well as player 1 start and player 2 start.

This is accomplished via buffers at 4D and 7D plus associated support circuitry.



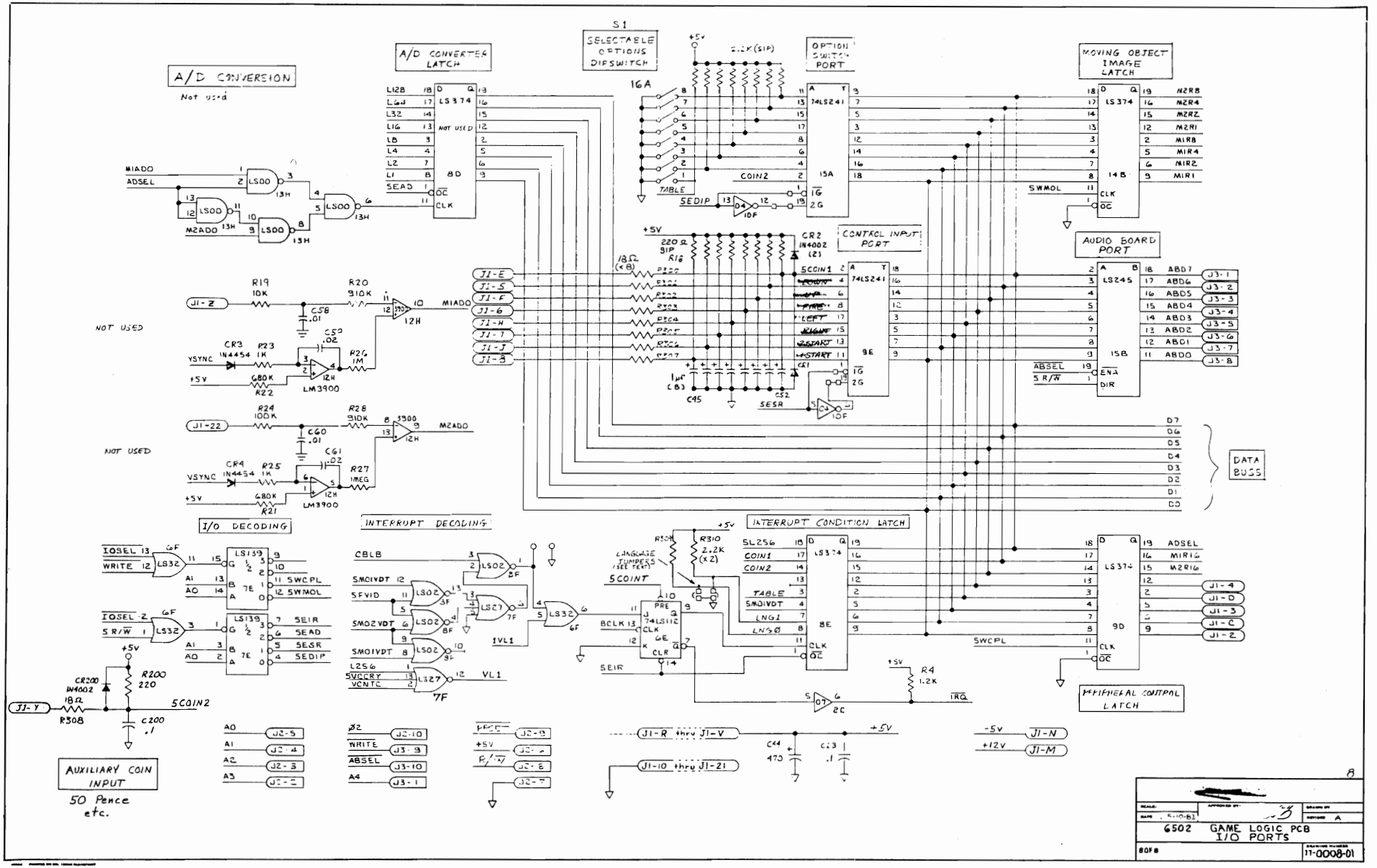
NOTES UNLESS OTHERWISE SPECIFIED:

PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF ESSEX INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY MARK VON STEIVER	DATE 2-20-83	ENGINEER MARK VON STEIVER	DATE 2-20-83	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL TOLERANCES	FINISH FRACTIONS	DECIMALS	ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE-DESCRIPTION MEMORY EXPANSION AND IO BOARD	SHEET OF 2	CODE	DRAWING NO. 77-0015-01	REV. A



PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EMPY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY MARK VON STRUER CHECKED	DATE DATE	ENGINEER MARK VON STRUER PROJECT ENGINEER	DATE 2-7-83 DATE	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL TOLERANCES	FRACTIONS	FINISH DECIMALS ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES DESCRIPTION MEMORY EXPANSION AND IO BOARD	SHEET 2 OF 2	CODE	DRAWING NO. 77-0015-01	REV. A

NOTES UNLESS OTHERWISE SPECIFIED:


A/D CONVERSION
Not used
A/D CONVERTER LATCH
S1
SELECTABLE OPTIONS DIPSWITCH
OPTION SWITCH PORT
MOVING OBJECT IMAGE LATCH
CONTROL INPUT PORT
AUDIO BOARD PORT
NOT USED
NOT USED
DATA BUSS
I/O DECODING
INTERRUPT DECODING
INTERRUPT CONDITION LATCH
PERIPHERAL CONTROL LATCH
AUXILIARY COIN INPUT
50 Pence etc.
6502 GAME LOGIC PCB I/O PORTS
11-0008-01

AUDIO/COLOR PCB-GENERAL DESCRIPTION

The Audio/Color PCB is so named because it contains not only the circuitry required to generate all sounds, but also the main color selection decoding circuitry and video output connector.

This PCB contains a dedicated 6502 microprocessor and circuitry to support the simultaneous generation of many types of sound, including three channel music. The Logic PCB simply sends commands to the Audio/Color PCB via a bi-directional communications port and the Audio/Color PCB takes it from there.

In some cases this PCB even aids the Logic PCB in some of it's calculations when there is not enough processing time available on the Logic PCB.

As a result of this structure, the actual program to generate sounds or music resides on the Audio/Color PCB. There is also a handshake required between the two PCB's in order for the system to power up correctly, and of course, there is no video output without the Audio/Color PCB connected.

1. Logic and Power Interface (P5,J2,J3)

Connector P5 provides the audio/color PCB with all the power it requires to operate. Also fed through this connector are the two speaker output leads. P5 interfaces only to the power supply module and the speaker, through the main harness.

Connectors J2 and J3 are the most significant path of communication between the Logic and Audio/Color PCB's. Address lines, Bi-directional Data lines, processor control lines, and the Audio/Color PCB Select line are all passed through these two connectors.

2. Communications and Address Decoding (9B,13D)

Peripheral Interface Adapter (PIA) 9B, in concert with 8B (another PIA, shown on page two) serves as a bi-directional communications path between the Logic PCB and the Audio/Color PCB. During information transfer between the two PCB's, both PIA's are in use. Information from the Logic PCB microprocessor passes through the PIA at 9B to the PIA at 8B, then to the microprocessor on the Audio/Color PCB. When information is passed the other direction, the path is the same, but the direction is reversed.

During the time that no information transfer is occurring between the two PCB's, both microprocessors can continue to operate independently.

Also shown on page one is 13D, a 3-line to 8-line decoder, used to generate the write signals for the Color Data Latches. These Latches will be covered in the text for page five of the Audio/Color PCB.

1. 6502 Microprocessor (3B)

This microprocessor is the same as that used on the Logic PCB, but is exclusively dedicated to the generation of sound. It can communicate with the Logic PCB microprocessor, and receives it's instructions thereby. Once it has received it's instructions, however, it asserts complete control over all Audio/Color PCB circuitry and ignores the Logic PCB microprocessor until such time as it is informed that another command is ready. Some commands are of a type that must be processed immediately, irregardless of other operations in progress, and some commands can wait until the operations in progress are completed. The program on the Audio/-Color PCB handles all these eventualities appropriately.

2. Peripheral Interface Adapters (8B, 7B)

The PIA at 8B, as mentioned in the text for page one, is used in bi-directional communications between the microprocessors on the Logic PCB and the Audio/Color PCB.

The PIA at 7B is used for two fundamental purposes on this PCB. The first, and most important, is that it contains the RAM that the microprocessor uses for zero page and stack operations. The PIA only contains 128 bytes of RAM, which under normal circumstances would not be sufficient for both zero page and stack. In this case, however, the memory map on this PCB has been altered, so that when the microprocessor thinks it is putting the stack at address 01FFH it is actually putting it at address 007FH.

The second use of this device is that of a programmable interval timer, used for various purposes unique to the specific sounds being generated on this game. The ability of this device to generate interrupts at time out is utilized here.

3. Address Decoding (4B)

Keyboard Encoder (4B) is used here to generate the chip selects of all devices located in the memory map of the Audio/Color PCB.

4. Music Generator (2B)

Another Programmable Counter/Timer device is used here to generate music (and sometimes other special effects) in up to three channels (or voices) simultaneously. The music is created by a special software operating system, and all but the counter/timer chip is therefore invisible.

5. Master Oscillator (A1,B1)

This oscillator is the source of all timing on the Audio/Color PCB. If this clock stops running, so does everything else on the Audio/Color PCB. It is, however, completely independent of the clock and other timing signals generated by the Master Oscillator located on the Logic PCB.

6. Program Memory (5A,6A,7A)

The memory devices used here are 2716 (2048 x 8) EPROMS. The DIP shunt located at 8A is used to reconfigure the control and power supply lines, if necessary, for equivalent devices from different manufacturers, whose pinouts may not be the same.

7. Output Filter Latch (1C)

This latch is used simply to switch different output filter capacitors in or out of the circuit to soften or shade the sound, according to program requirements, or to change the volume.

1. Clock Manipulation and Noise Generation Circuit (3D,4D,6D,5E)

The timers inside Programmable Timer Module 3D can be incremented or decremented either internally by the Phase Two clock input, or externally from the "C" inputs (C1,C2,C3). Both options are used by the program. When the counters are being controlled by the Phase Two clock, the "C" inputs have no effect, and the noise generation circuit is therefore inoperative. In order to generate sounds that are classified as noise, or contain some kind of noise within them, the counters are programmed to decrement in accordance with the input on the "C" inputs. While in this mode, the combination of 6D (Dual "D" Flip-Flop) and 5E (128 Bit Shift Register), are used to "randomize" the clock inputs to the Programmable Timer Module (3D). The "randomizer" can be clocked with either the Phase Two clock or counter output Q1.

2. Amplitude Modulation Control (2D, 7D, 8D, 9D)

Counter (3D) outputs Q1,Q2, and Q3 are already highly complex sounds, but in order to create much more specialized audio they must be modulated in amplitude. Each channel is separately controllable in amplitude by associated Digital-to-Analog converters comprised of analog multiplexers and a resistive ladder network. Three control bits on each multiplexer select a voltage to output, according to which input pin is addressed (since each input pin is tied to a different point, and therefore voltage, in the resistive ladder).

The voltage thus selected is applied to one of the two inputs to each segment of 2D (another triple analog switch). The other input is tied to ground. Note that the control bit to each analog switch segment is one of the previously mentioned count outputs (Q1,Q2,Q3). In this manner, each output can be controlled for frequency and amplitude individually.

Note also that the count output from Q1, unlike Q2 and Q3, first passes through yet another analog switch whose function is to turn off the count output of Q1 prior to reaching the Digital-to-Analog conversion stage. This is done because the Q1 output is the one used for selective clock frequency generation, and would therefore interfere with other sounds if not disabled at the appropriate time.

3. Output Summation and Special Effects Volume Control (2E)

The three segments of Operational Amplifier 2E are configured as voltage followers (for impedance considerations), and their outputs are summed together at the top of a 10K POT, R31. The output volume, therefore is determined by the voltage applied at each input and the adjustment of the POT. Note that the resistors used to sum these three outputs together are large in value, so that each channel will have minimal effect on the others when conflicting signals arrive simultaneously (except, of course, that their sum will appear at the output).

This summed output is then again summed with all other sounds generated by this PCB at the input to the final Power Amplifier.

1. Summing Amplifier and Master Volume Control (3F, R46)

One segment of Operational Amplifier 3F is used here as a point at which all the various sounds generated on this PCB are brought together. Note that the output goes immediately to a 10K POT (R46) which has ground on the other end. The wiper, therefore, varies the final output volume of all sounds together.

2. Integrator and Audio Power Amplifier (3F,10F)

Another segment of Operational Amplifier 3F is used here as an integrator; that is, it is used to "roll off" the higher frequency sounds in order to prevent the power amplifier from going into unwanted oscillation.

The Audio Power Amplifier (10F) is a Dual Audio Amplifier IC configured as a "Bridge Amplifier" and may be either a LM377 or LM378 for Revision A, Audio/Color PCB. Revision letters are located at position 11C. Information regarding this is available in the operators manual for this game, or contact the Exidy Customer Service Department for assistance if you must use an alternate device.

Volume Controls

Master Volume R46, see the fourth page of Audio/Color PCB schematics.

Music Volume R9, see the fourth page of Audio/Color PCB schematics.

Special Effects Volume R3, see the fourth page of Audio/Color PCB schematics.

1. Pattern Character Color Division (10A,9A)

The two segments of Flip-Flop 10A, using the upper two address lines from the character generator circuit, divide the character generator RAM space into four (4) conceptual groups (or quadrants) according to address. This is done in order to assign different colors to different characters.

Using this method, any character stored in a particular quadrant will be the same color as any other character stored in that same quadrant. If the same character is stored in a different quadrant, it will be displayed with a different color. The output of 9A (Two-line to Four-line decoder) applies the separated video lines of these quadrants to priority encoder 10B, whose task is to determine which image is to take visual preference when two or more coincide on the TV screen; that is, which image is to appear to be in the "foreground", and which is to appear to be in the "background".

2. Priority Encoder (10B)

All the video signals generated by the logic PCB are applied to the priority encoder. The signals assigned the higher priority are shown at the top, and the lower priority are shown on the bottom. The output of this device is a 3 Bit code representing the highest priority video line active at that instant. This output code is then sent to the color multiplexers as an address which will select the appropriate color for the imagery generated on that video line. Note that the lowest priority input to the encoder is tied permanently low (active). This insures that when no other video is being generated, there is a background color present, unless of course, the program has selected a background color of black at that time.

3. Color Data Latches (11C,12C,13C)

These latches are addressed directly by the Logic PCB microprocessor. Here the microprocessor stores the data that determines which character is what color. This data is then passed to the color selection multiplexers.

4. Color Selection Multiplexers (11B, 12B, 13B)

Each of the three multiplexers controls the video output to a different color gun in the CRT. One turns the red gun on or off, one turns the green gun on or off, and the third does the same for the blue gun. The output combination of the three multiplexers provides for one of eight possible colors to be displayed at any given instant. The color displayed is determined by two things: what type of video is present (e.g. which character), and what color the microprocessor has currently assigned to that type of video. As mentioned above, the color assignations are stored in the color data latches. The priority encoder (10B) issues the code representing the type of video currently displayed. Using these two pieces of information, the multiplexers look at the appropriate bits in the color latches and send the data directly to the TV to turn the color guns on or off.

5. Video and Sync Signal Polarity Selection (11A,12A)

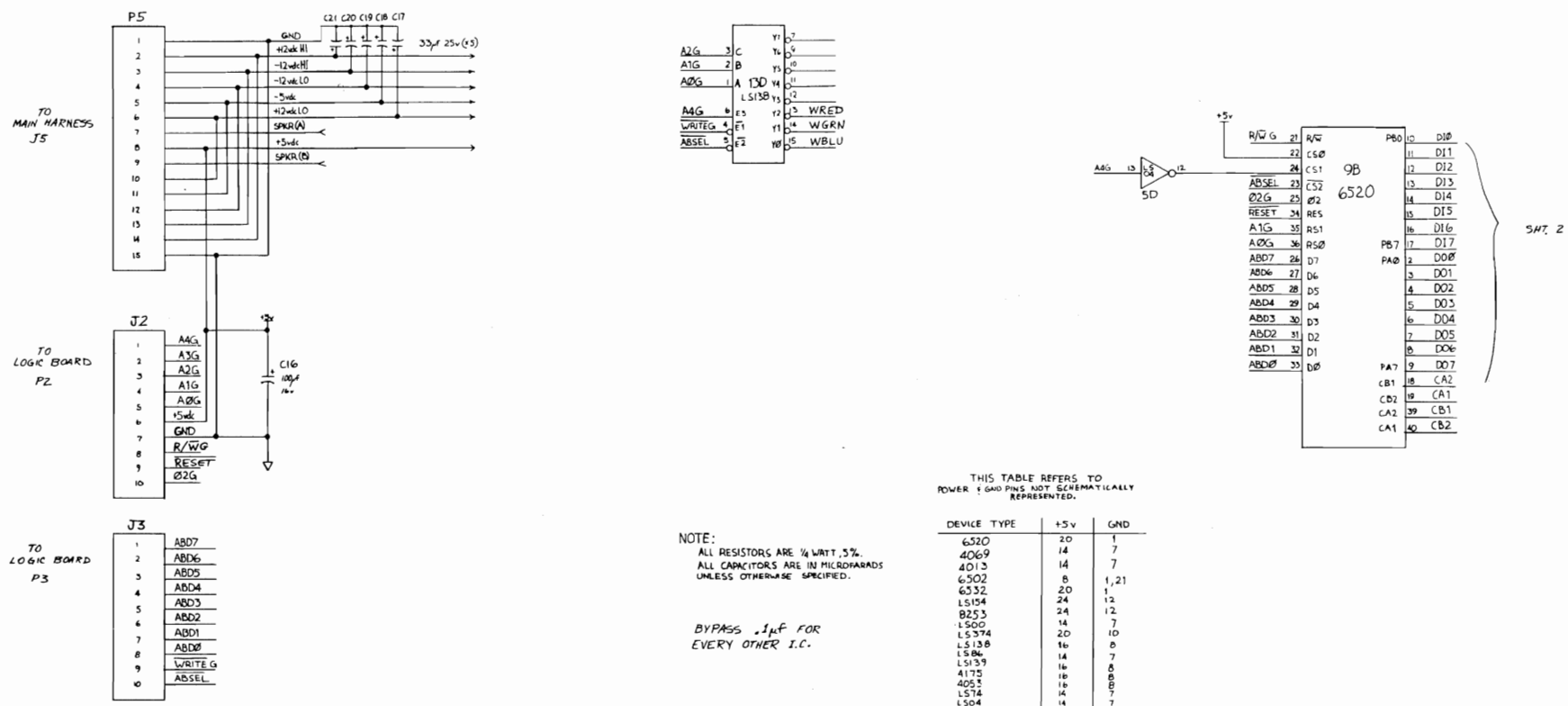
Before being reclocked one last time, all video outputs are passed through an Exclusive-Or gate (11A), so that one input of each segment can be used to invert the video (make it 180 degrees out of phase with respect to the input to the gate). This feature insures compatibility with TV monitors made by several different manufacturers.

The TV Sync signals are also routed through Exclusive-Or gate segments (12A) for the same purpose.

6. Final Video Output Re-synchronization (13A)

To insure that all video signals and sync signals are accurately synchronized in time, they are all re-clocked one last time together by a HEX "D"Flip-Flop. It "cleans up" any spurious irregularities or propagation delays that may have crept into any of the video or sync signals.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASE	5-10-82	[illegible]



NOTE:
ALL RESISTORS ARE ¼ WATT, 5%.
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

BYPASS .1µf FOR EVERY OTHER I.C.

THIS TABLE REFERS TO POWER & GND PINS NOT SCHEMATICALLY REPRESENTED.

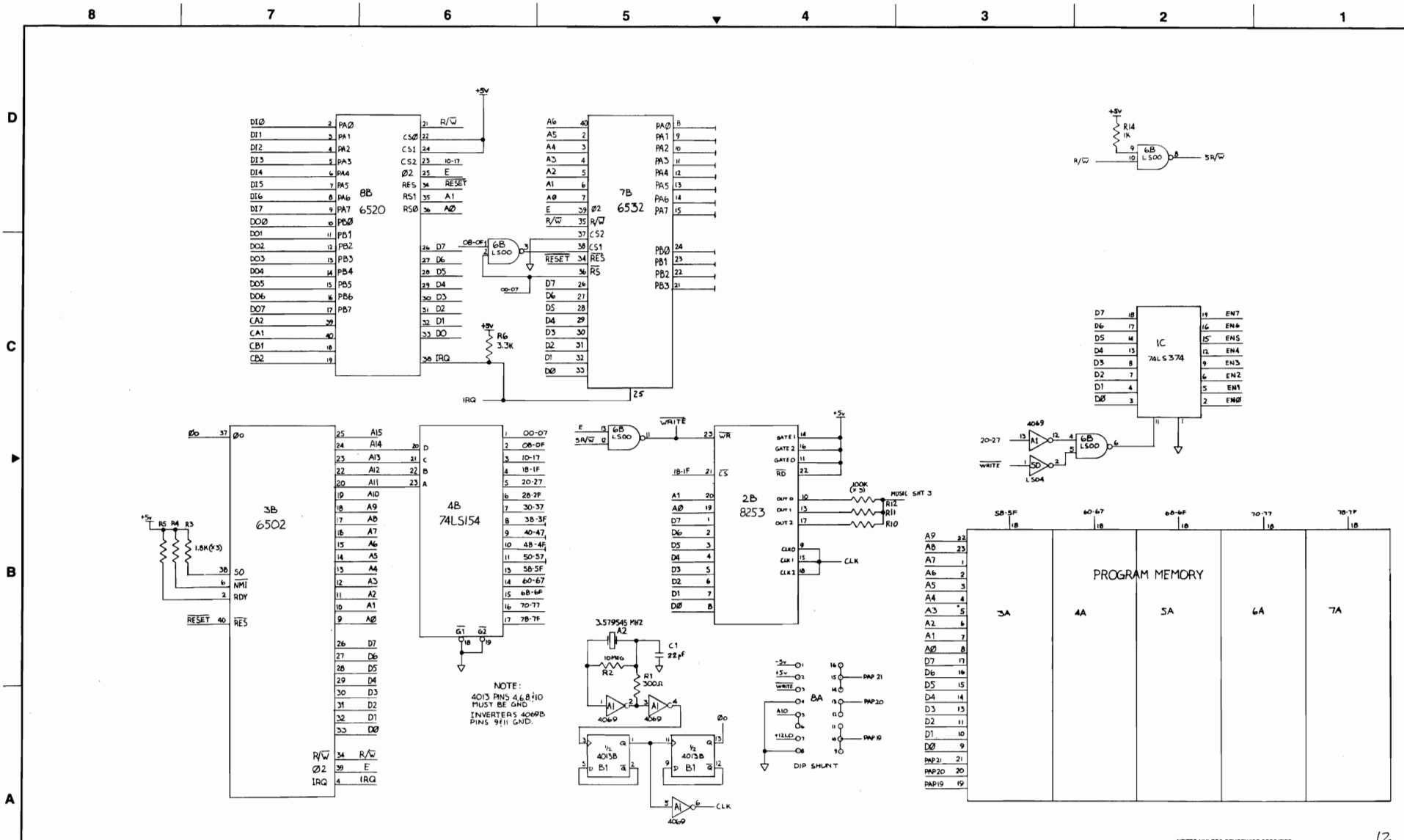
DEVICE TYPE	+5v	GND
6520	20	1
4069	14	7
4013	14	7
6502	8	1,21
6532	20	1
LS154	24	12
8253	24	12
LS00	14	7
LS374	20	10
LS138	16	8
LS86	14	7
LS139	16	8
4175	16	8
4053	16	8
LS74	14	7
LS04	14	7
7406	14	7
4175	16	8
4051	16	8
4562	14	7
74151	16	8
74148	16	8
LS174	16	8

NOTES UNLESS OTHERWISE SPECIFIED

13

PROPRIETARY	DESIGN DRAWING	DRAWN BY	DATE	ENGINEER	DATE	SCALE	DATE OF ISSUE	MATERIAL	FINISH		SIZE	TITLES/DESCRIPTION	SHEET	CODE	DRAWING NO	REV
THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DETAILS AVAILABLE UPON WRITTEN REQUEST	NEAL R. ZOOK	6-8-81	MARK VON STRIVER	6-8-81	DO NOT SCALE DRAWING		TOLERANCES	FRACTIONS	DECIMALS	ANGLES	D	AUDIO/COLOR PCB SCHEMATIC DIAGRAM	1 OF 5		77-0007-01	A
		CHECKED [illegible]	5-10-82	PROJECT ENGINEER	DATE											

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410



NOTES UNLESS OTHERWISE SPECIFIED:

12

PROPRIETARY	DESIGN DRAWING	DRAWN BY	DATE	ENGINEER	DATE	SCALE	DATE OF ISSUE	MATERIAL	FINISH		SIZE	TITLES/DESCRIPTION	SHEET	CODE	DRAWING NO	REV
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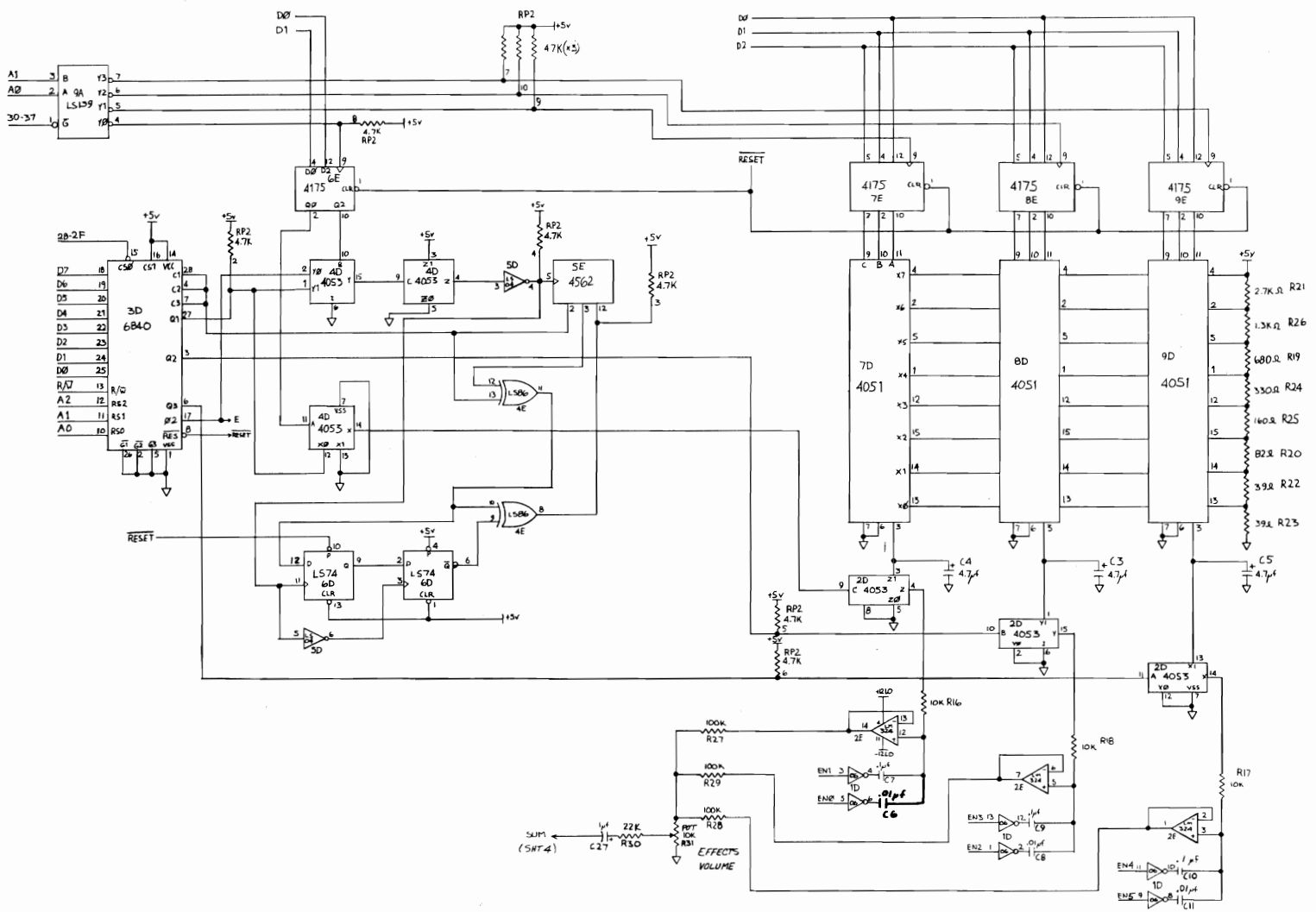
		CHECKED	DATE 5-10-81	PROJECT ENGINEER	DATE											



NOTES UNLESS OTHERWISE SPECIFIED

PROPRIETARY	DESIGN DRAWING	DRAWN BY	DATE	ENGINEER	DATE	SCALE	DATE OF ISSUE	MATERIAL	FINISH		SIZE		SHEET	CODE	DRAWING NO	REV
THIS DOCUMENT IS THE PROPERTY OF EXIDY, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DETAILS AVAILABLE UPON WRITTEN REQUEST	NEAL R. ZOOK	6-9-81	MARK VON STRIVER	6-9-81	DO NOT SCALE DRAWING		TOLERANCES	FRACTIONS	DECIMALS	ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	D	AUDIO/COLOR PCB SCHEMATIC DIAGRAM	3 of 5		77-0007-01	A
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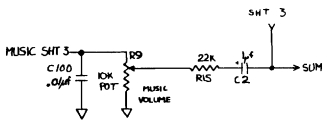
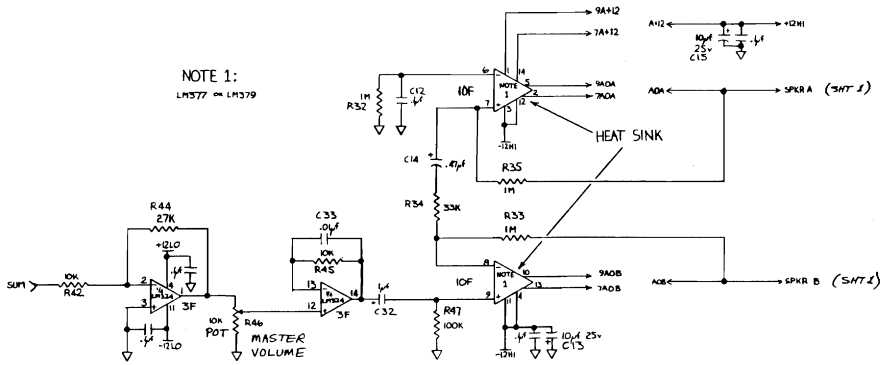
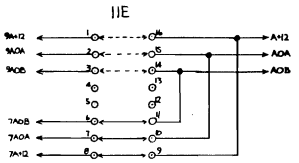


NOTE 1:
LM377 OR LM379



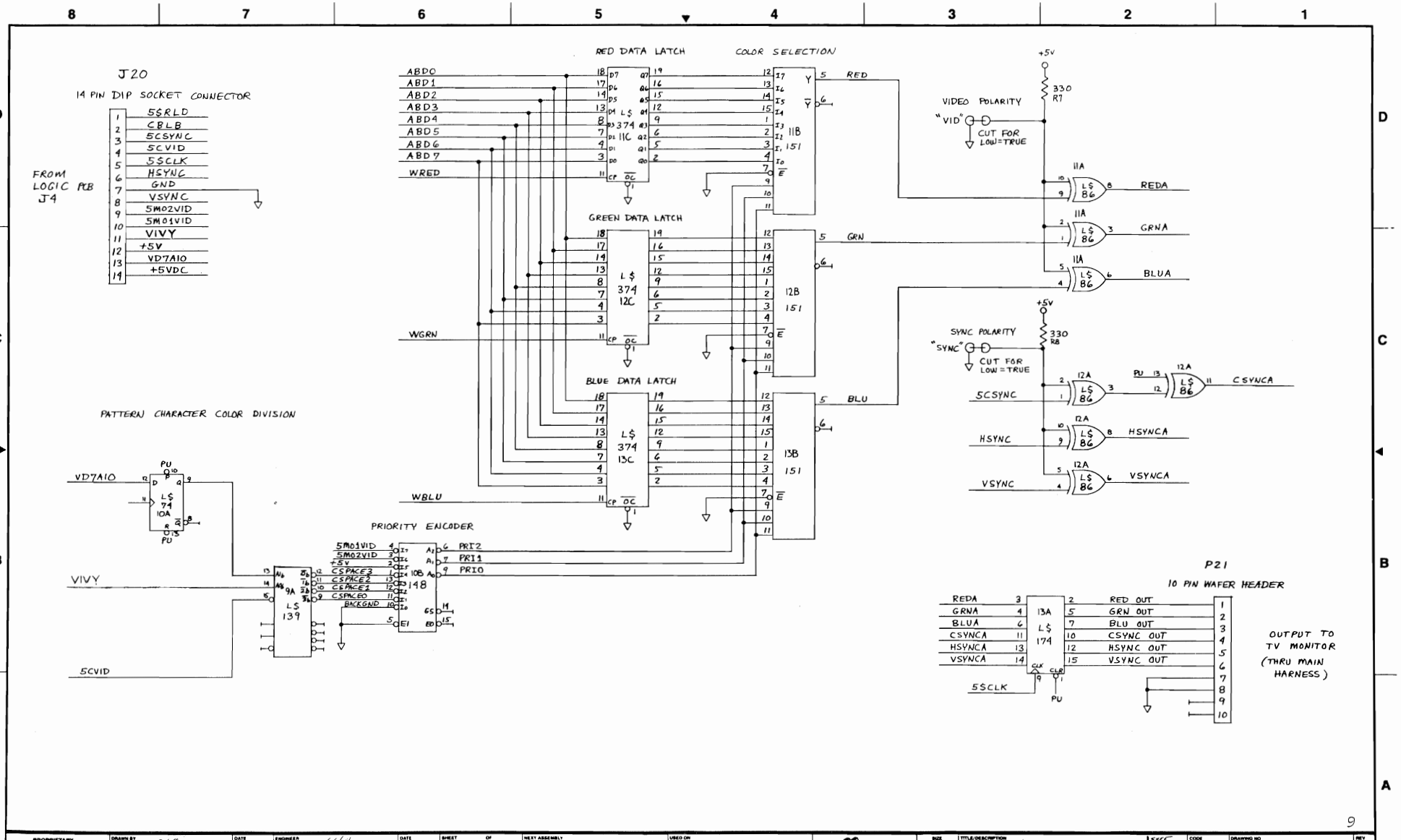
IIE



DIP SHUNT CONFIGURATION
DOTTED LINE FOR LM379
SOLID LINE FOR LM377, LM378

NOTES UNLESS OTHERWISE SPECIFIED:

PROPRIETARY: THIS DOCUMENT IS THE PROPERTY OF ESSEX, INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING: DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY: NEAL R. ZOOK	DATE: 6-9-81	ENGINEER: MACK VON STRIVER	DATE: 6-9-82	SCALE: DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL / TOLERANCES	FINISH / FRACTIONS / DECIMALS / ANGLES	ESSEX	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE: D	AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 4 OF 5	CODE	DRAWING NO. 77-0007-01	REV A
		CHECKED	DATE 5-10-82	PROJECT ENGINEER	DATE										



PROPRIETARY — THIS DOCUMENT IS THE PROPERTY OF ATARI INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DRAWN BY AKH	DATE 6-7-81	ENGINEER AKH	DATE 6-7-81	SHEET 5 OF 5	NEXT ASSEMBLY	USED ON	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLE/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 5 OF 5	CODE	DRAWING NO 77-0007-01	REV A
	CHECKED	DATE 5-10-82	PROJECT ENGINEER	DATE 6-7-81										

APPENDIX B: **ILLUSTRATED PARTS LIST FOR FAX™**

The following is an illustrated parts list to aid you, should you need to order replacement parts for FAX™. The drawings have all parts labeled by a number within a circle. This number refers to the item number on the Parts List directly across from the drawing. In the case of the Final Assembly list, the second drawing has numbers referring to the Final Assembly list found opposite the first drawing.

Following the Illustrated Parts List is a list of parts for the Logic, Audio and Plane Interface boards, Memory Expansion Board and overall cabinet hardware.

A. FAX™ FINAL ASSEMBLY

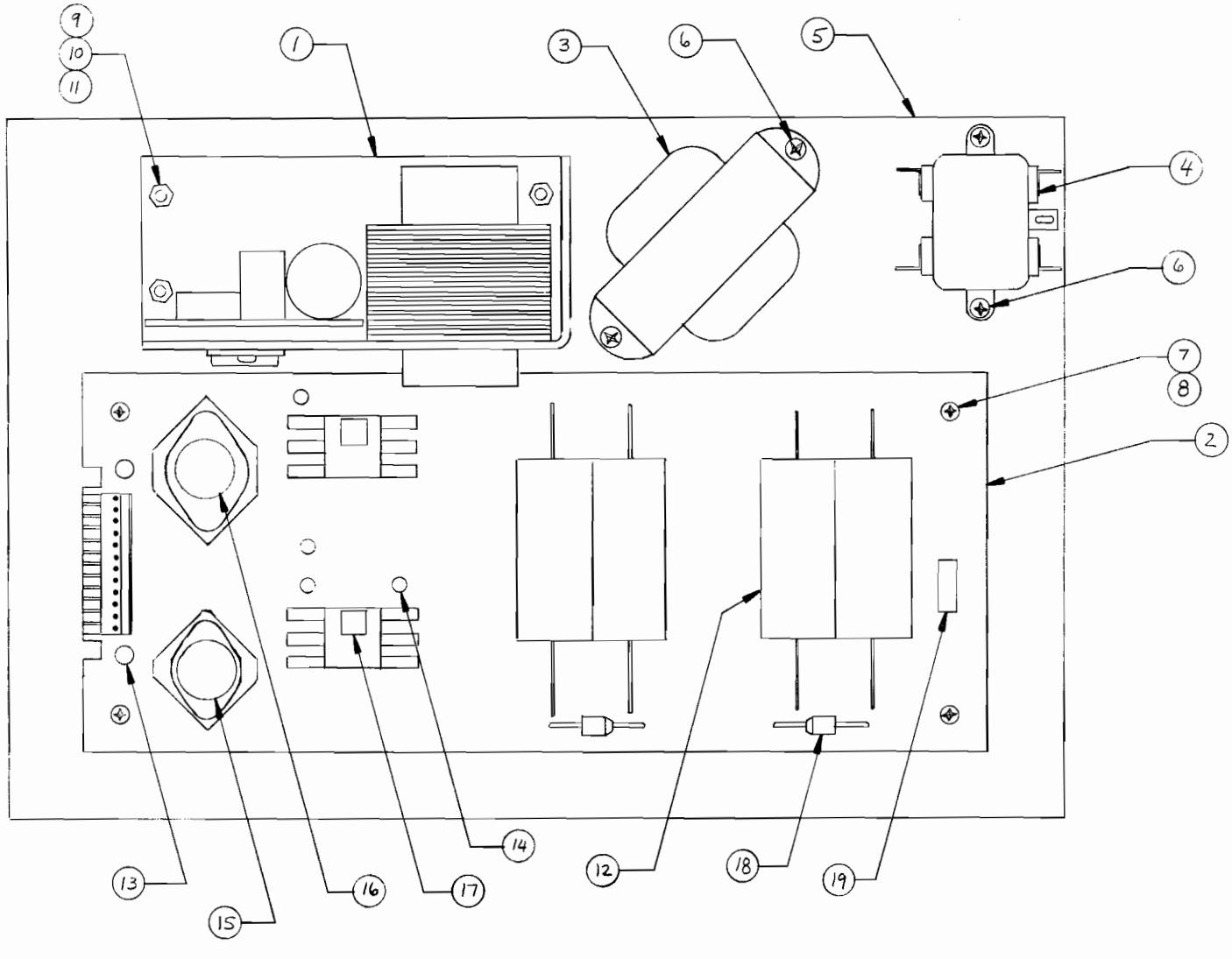
Item	Part Number	Description
	90-0073-00	Assy, Cabinet
	65-0091-00	Speaker Grill
	61-0049-00	Face panel Assy
	65-0092-00	Retainer Channel
	51-2104-25	Screw #8A Sq.Dr.x 1/2
	80-0054-00	FAX™ Display Plex
	65-0090-00	Plex Bracket
	59-0052-00	O-Ring #2 5/32IDx1/16
	54-1100-00	Kep Nut #6-32
	90-0074-00	TV Bezel Assy
	79-0001-00	Monitor, 13in 13K4801
	51-3806-20	Screw, #10 HiLo Pan Hdx3/4
	53-3000-00	Washer #10
	80-0058-00	Anti-Glare Filter, 13in.
	95-0023-00	Fluoresent Bulb
	95-0025-00	Fluoresent Socket Bryant
	49-0028-05	Assy Lamp Harness
	65-0094-00	Bracket Lamp Holder
	50-1102-00	Screw, 6-32x1/4
	51-2204-00	Screw, #8AB Pan Hd x 1/2
	48-3002-00	Switch Assy Starpoint
	48-3003-00	Switch Assy Starpoint
	61-0048-00	Front Door Assy
	61-0035-00	Rear Door Assy
	90-0075-00	Power Supply Assy
	51-2008-01	Screw #8 FH Wood x 1.0
	90-0076-00	Isolation Transformer Assy
	51-2008-01	Screw #8 FH Wood x 1.0
	95-0014-00	Coin Door Assy
	49-0023-05	Assy FAX™ Coin Door Harness
	51-2204-00	Screw, #8AB Pan Hd x 1/2
	65-0089-00	Coin Box Door
	65-0088-00	Bracket Hasp
	50-3306-22	Bolt Carriage 10-24x3/4
	54-3300-01	Kep Nut 10-24

A.FAX™ FINAL ASSEMBLY continued

Item	Part Number	Description
	95-0016-00	Cash Box, Plastic
	65-0099-00	Bracket Coin Counter
	95-0015-00	Coin Counter
	51-2204-00	Screw #8AB Pan Hd.x1/2
	50-0006-00	Screw #4-40 Pan Hd.x3/4
	95-0017-00	Speaker 9x6 Oval
	65-0095-00	Speaker cover
	51-2006-01	Screw #8 FH Wood x3/4
	49-0027-05	Assy Speaker Harness
	48-5001-00	Interlock Switch
	65-0096-00	Interlock Sw.Brk.x.50
	65-0097-00	Interlock Sw.Brk.x.75
	51-2204-00	Screw,#8AB Pan Hd x 1/2
	49-0029-05	Power Cord Assy
	51-2204-00	Screw #8AB Pan Hd x 1/2
	77-0007-05	PCB Audio
	77-0008-05	PCB Logic
	77-0015-05	PCB Memory Expansion
	77-0006-05	PCB Plane Interface
	51-2204-00	Screw #8AB Pan Hd x 1/2
	49-0024-05	Assy FAX™ Main Harness
	49-0026-05	Assy FAX™ Control Harness
	49-0025-05	Assy FAX™ A.C. Power Harness
	51-2204-00	Screw #8AB Pan Hd X 1/2

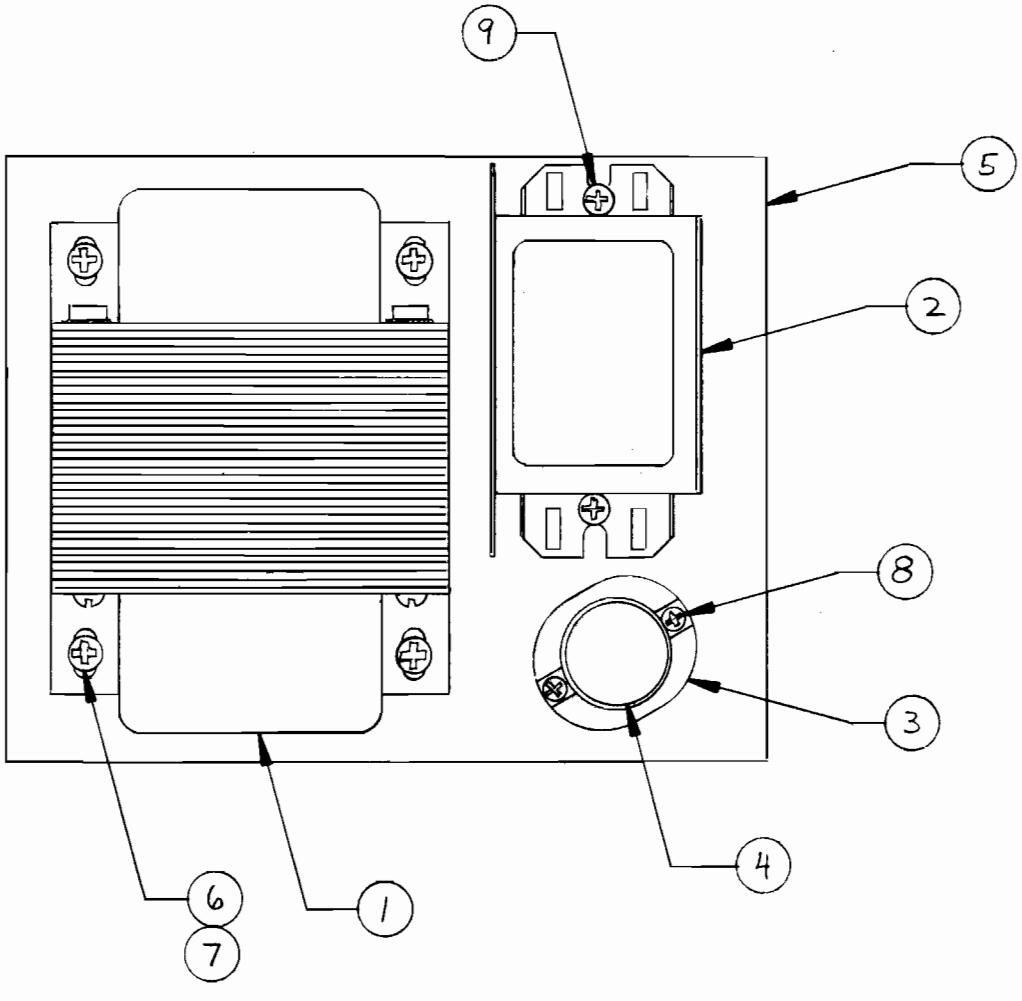
B. FAX POWER SUPPLY ASSEMBLY, 90-0075-00

Item	Part Number	Description
1	32-0001-00	POWER SUPPLY, 5V @ 6AMPS
2	77-0001-05	PCB REGULATOR
3	30-0001-00	XFMR STEP DOWN
4	31-0001-00	EMI FILTER
5	60-0350 00	POWER SUPPLY MOUNTING BOARD
6	51-3204-00	SCREW, #10 AB PAN HD x1/2
7	51-1204-00	SCREW, PAN HD, #6 X 1/2" LG. TYPE AB
8	55-0001-00	SPACER, #6 x .1/8 NON-METALLIC
9	50-1105-00	SCREW, PAN HD. #6-32 x 5/8" LG.
10	53-1004-00	WASHER, FLAT, #6
11	54-1100-01	NUT, KEP, #6-32
12	13-4085-00	CAP ELECT 4000 MF 50V
13	13-3364-00	CAP ELECT 33 MF 25V
14	13-6844-00	CAP ELECT 6.8 MF 25V
15	21-0003-00	TRANSISTOR 2N3055
16	21-0004-00	TRANSISTOR 2N6246
17	21-0006-00	REGULATOR 7912
18	20-0003-00	DIODE 60$1/UT 4010
19	20-0005-00	RECTIFIER, BRIDGE MDA-970-1



C. ISOLATION TRANSFORMER ASSEMBLY, 90-0076-00

Item	Part Number	Description
1	30-0002-00	TRANSFORMER, ISOLATION
2	30-0004-00	FLUORESENT LAMP BALLAST
3	95-0026-00	FLUORESENT STARTER SOCKET
4	95-0024-00	FLUORESENT STARTER (F&S)
5	60-0351-00	MOUNTING BOARD
6	51-3806-20	SCREW, #10 HiLo PAN HD x3/4
7	53-3000-00	WASHER #10 FLAT
8	51-0105-20	SCREW, #4A PAN HD x 5/8
9	51-2204-00	SCREW, #8AB PAN HD x 1/2



D. COIN DOOR ASSEMBLY, 95-0014-00

Item	Part Number	Description
1	95-0014-00	COIN DOOR
2	49-0023-00	COIN HARNESS ASSY

E. LOGIC AND AUDIO BOARD ASSEMBLY 90-0005-00

1	77-0008-05	PWA LOGIC
2	77-0007-05	PWA AUDIO COLOR
3	55-0002-00	SPACER NON-METALLIC #6-32 X 7/8 LONG
4	50-1102-00	SCREW, PAN HD. PHIL #6-32 x 1/4 LG
5	36-0006-00	CABLE ASSY, RIBBON, 14 PIN
6	59-0056-00	WASHER, FLAT, NYLON #6
7	36-0005-00	PLANE INTERFACE RIBBON CABLE
8	77-0006-05	PLANE INTERFACE PCB ASSEMBLY

F. PRINTED CIRCUIT ASSEMBLY-UNIVERSAL POWER SUPPLY, 77-ØØØ9-Ø5

1	77-ØØØ9-Ø4	UNIVERSAL POWER SUPPLY BOARD
2	13-4Ø85-ØØ	CAP, ELECT. 4ØØØMF, 5ØV AXIAL LEAD
3	13-3364-ØØ	CAP, ELECT. DIP 33MF 25V + 2Ø%
4	13-6844-ØØ	CAP, ELECT. DIP 6.8MF 25V + 2Ø%
5	2Ø-ØØØ3-ØØ	DIODE 6ØS1 or UT4Ø1Ø
6	2Ø-ØØØ5-ØØ	RECTIFIER, BRIDGE MDA-97Ø-1
7	21-ØØØ3-ØØ	TRANSISTOR, 2N3Ø55
8	21-ØØØ4-ØØ	TRANSISTOR, 2N6246
9	21-ØØØ5-ØØ	REGULATOR 79Ø5
1Ø	21-ØØØ6-ØØ	REGULATOR 7912
11	84-ØØ12-ØØ	HEATSINK
12	84-ØØ13-ØØ	HEATSINK
13	4Ø-ØØØ2-ØØ	CONNECTOR 12 PIN (WAFER HEADER)
14	5Ø-4Ø27-ØØ	SCREW, PAN HD #4-4Ø x 3/8 LG (PHIL)
15	53-4Ø11-Ø1	NUT, KEP #4-4Ø
16	37-ØØØ1-ØØ	TIE WRAP 5 1/2"

G. LOGIC BOARD, 77-0008-05

Item	Part Number	Description	Location
1	77-0008-04	PCB LOGIC	
2	22-0001-02	I.C. 74LS00	3D, 15C, 15H
3	22-0002-02	I.C. 74LS02	1H, 6H, 8F
4	22-0003-02	I.C. 74LS04	1D, 4D, 3F, 10F, 11F
5	22-0004-00	I.C. 7407	2C
6	22-0005-02	I.C. 74LS08	5E
7	22-0006-02	I.C. 74LS11	3H
8	22-0007-02	I.C. 74LS20	2F
9	22-0008-02	I.C. 74LS21	12F, 15E
10	22-0009-02	I.C. 74LS27	7F, 2H
11	22-0010-02	I.C. 74LS32	6F
12	22-0011-02	I.C. 74LS74	1C
13	22-0012-02	I.C. 74LS112	2E, 6E
14	22-0013-02	I.C. 74LS138	5B, 5D
15	22-0014-02	I.C. 74LS139	7E, 16H
16	22-0015-02	I.C. 74LS157	14A, 14E
17	22-0016-02	I.C. 74LS161	1E, 2D, 4F, 5F
18	22-0017-02	I.C. 74LS166	12B, 12D, 13D, 14D, 15D
19	22-0018-02	I.C. 74LS193	10E, 12E, 13F, 15F, 14FM 16F, 11E 13E
20	22-0019-02	I.C. 74LS241	1A, 3A, 15A, 3B, 6B, 9B, 8C, 7D, 9E, 4H
21	22-0020-02	I.C. 74LS245	3C, 4C, 6C, 13B, 15B
22	22-0021-02	I.C. 74LS374	1F, 14B, 7C, 9D, 8E
23	25-0004-00	MICROPROCESSOR 6502	2A
24	28-0004-00	2114 RAM (1K x 4)	4A, 5A, 7B, 8B
25	24-0011-00	6301 PROM (256x4) P2L5C-1	5C
26	24-0012-00	6331 PROM (32x8) P2L6D-1	6D
27	24-0013-00	6331 PROM (32x8) HRL14H-1	14H
28	20-0001-01	1N4002 DIODE	8E, 9F, 2H
29	02-4712-00	RES. 470 OHM 1/4W 5%	1D, 2H
30	02-1222-00	RES. 1.2K 1/4W 5%	2C
31	02-1822-00	RES. 1.8K 1/4W 5%	1C, 2C
32	02-2222-00	RES. 2.2K 1/4W 5%	7E, 2A
33	02-2722-00	RES. 2.7K 1/4W 5%	1C, 2C
34	09-0007-00	RES. 220 OHM 1/8W 5% 10 Pin Sip	9E
35	09-0004-00	RES. 2.2K 1/8W 5% 10 Pin Sip	
36	09-0008-00	RES. 4.7K 1/8W 5% 10 Pin Sip	15A
37	09-0009-00	RES. 6.8K 1/8W 5% 10 Pin Sip	14A
38	23-0045-00	CAP. .01uf CERAMIC DISC	1D
39	10-1034-1	CAP. .1uf CERAMIC DISC	A/R

G. LOGIC BOARD, continued

Item	Part Number	Description	Location
40	10-1044-1	CAP. 6.8uf 25v DIPTANT	1C, 15D, 6E, 13F
41	13-6844-1	CAP. 33uf 25V ELECTROLYTIC	1C, 2C
42	13-3365-0	CAP. 470uf 10V ELECTROLYTIC	10H
43	13-4775-0	DIPSHUNT JUMPER PAKS 16 PIN	4B, 11B, 10D
44	47-0001-00	DIP SWITCH 8 POS.	16A
45	49-5002-00	CRYSTAL 11.289mhz (SERIES)	1D
46	29-0001-00	10 PIN MALE MOLEX HDR	16C, 16F
47	40-0061-00	DIP SOCKETS 16 PIN LOW PROFILE	4B, 11B, 5C, 6D 14H, 10D
48	44-1601-00	DIP SOCKETS 24 PIN LOW PROFILE	6A thru 13A, 11D
49	44-2401-00	DIP SOCKETS 40 PIN LOW PROFILE	2A
50	44-4001-00	DIP SOCKETS 14 PIN LOW PROFILE	16B
51	44-1401-00	DIP SOCKETS 18 PIN LOW PROFLE	4A, 5A, 7B, 8B, 11C 12C, 13C, 14C
52	44-1801-00	CAP luf DIPTANT	C45 thru C52, 5D, 2H
53	11-1053-00	RES. 220 OHM 1/4W 5%	R200, R311
54	02-2212-00	RES. 18 OHM 1/4W 5%	R300 thru R302
55	02-1802-00	CAP. 330 pf CER. DISC	5D
56		E PROM, 2732 FXL	6A
57		E PROM, 2732 FXL	7A
58		E PROM, 2732 FXL	8A
59		E PROM, 2732 FXL	9A
60	10-2214-4	CAP 220 pf CERAMIC DISC	
61		E PROM, 2732 FXL	10A
62		E PROM, 2732 FXL	11A
63		E PROM, 2732 FXL	12A
64		E PROM, 2732 FXL-6	13A
65		E PROM, 2716 FXL	11D

H. AUDIO/COLOR BOARD ASSEMBLY 77-0007-05

1	77-0007-04	PRINTED CIRCUIT BOARD	
2	22-0013-02	I.C. 74LS138	13D
3	26-0003-00	I.C. 6520	8B, 9B
4	25-0002-00	I.C. 6532	7B
5	25-0004-00	I.C. 6502	3B
6	27-0001-00	I.C. 6840	3D
7	22-0022-02	I.C. 74LS154	4B
8	27-0002-00	I.C. 8253	2B
9	22-0023-00	I.C. 4069	1A
10	22-0055-00	I.C. 4013B	1B

H. AUDIO/COLOR BOARD ASSEMBLY, continued

Item	Part Number	Description	Location
11	22-0003-02	I.C. 74LS04	5D
12	22-0001-02	I.C. 74LS00	6B
13	22-0021-02	I.C. 74LS374	1C, 11C, 12C, 13C
14	22-0024-00	I.C. 4053	2D, 4D
15	22-0025-00	I.C. 4175	6E, 73, 8E, 9E
16	22-0056-00	I.C. 4562	5E
17	22-0011-02	I.C. 74LS74	10A, 6D
18	22-0026-00	I.C. LM324	3F, 2E
19	22-0054-00	I.C. 7406	1D
20	22-0027-02	I.C. 74LS86	11A, 12A, 4E
21	22-0028-00	I.C. 4051	7D, 8D, 9D
22	22-0014-02	I.C. 74LS139	9A
23	22-0057-00	I.C. LM377	10E
24	22-0029-02	I.C. 74LS148	10B
25	22-0030-02	I.C. 74LS151	11B, 12B, 13B
26	22-0031-02	I.C. 74LS174	13A
27	10-1044-1	.1 uf. CERAMIC CAP 25V	1A thru 7A, 9A, 11A, 13A, 1B, 6B, 9B, 11B, 1C, 11C, 13C, 1D 3D, 5D, 7D, 9D, 11D, 13D, 1E, 2E, C7, C9, C10, 3E, 5E, 7E, 9E, C12, 13E, 2F, 4F, 12F, 9E, 2E, 3F
28	10-2204-1	22pf CERAMIC CAP 16V	C1
29	10-1034-1	.01 uf CERAMIC CAP 16V	C6, C8, C11, C33, 1C
30	13-3365-1	33uf CAP, 25V, ELECTROLYTIC W/AXIAL LEADS	C13, C15, C17 thru C21
31	13-1075-00	100uf CAP ELECTRO-LYTIC 16V	C16
32	13-4755-00	4.7uf CAP ELECTRO-LYTIC 16V	C3, C4, C5
33	13-1055-00	1.0uf CAP ELECTRO-LYTIC 16V	C27, C32, C2
34	02-1822-00	1.8K RES. 1/4W 5%	R3, R4, R5
35	02-3322-00	3.3K RES. 1/4W 5%	R6
36	02-1022-00	1K RES. 1/4W 5%	R14
37	02-1062-00	10M RES. 1/4W 5%	R2
38	02-3012-00	300 OHM RES. 1/4W 5%	R1
39	02-1042-00	100K RES. 1/4W 5%	R10, R11, R12, R27 R47, 428, R29
40	02-2232-00	22K RES. 1/4W 5%	R15, R30
41	02-1052-00	1M RES. 1/4W 5%	R32 R33, R35
42	02-3332-00	33K RES. 1/4W 5%	R34
43	02-2722-00	2.7K RES. 1/4W 5%	R21
44	02-2732-00	27K RES. 1/4W 5%	R44
45	02-1322-00	1.3K RES. 1/4W 5%	R26
46	02-6812-00	680 OHM RES. 1/4W 5%	R19
47	02-3312-00	330 OHM RES. 1/4W 5%	R7, R8, R24
48	02-1612-00	160 OHM RES. 1/4W 5%	R25

H. AUDIO/COLOR BOARD ASSEMBLY, continued

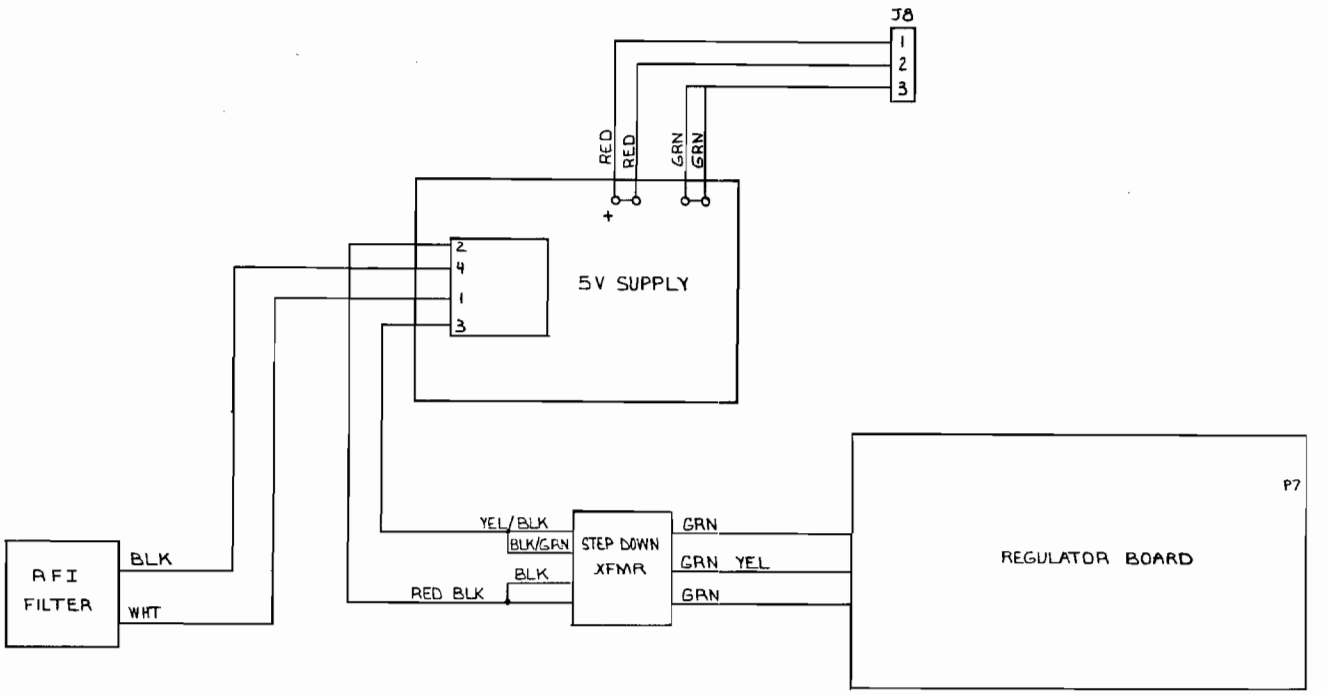
Item	Part Number	Description	Location
49	Ø2-82Ø2-ØØ	82 OHM RES. 1/4W 5%	R2Ø
5Ø	Ø2-39Ø2-ØØ	39 OHM RES. 1/4W 5%	R22, R23
51	Ø7-1Ø32-ØØ	1ØK RES. 1/4W 5%	R16, R17, R18, R42, R45
52	Ø7-ØØØ4-ØØ	1ØK POT	R9, R31, R46
53	Ø9-ØØØ8-ØØ	4.7K RES. PAC 1Ø PIN SIP	4D
54	29-ØØØ2-ØØ	3.579545 MHZ CRYSTAL	2A
55	47-ØØØ1-ØØ	16 PIN DIP SHUNT	8A, 11E
56	44-14Ø1-ØØ	14 PIN DIP SOCKET	J2Ø, 1A, 1B, 5E
57	44-24Ø1-ØØ	24 PIN DIP SOCKET	3A, 4A, 5A, 6A, 7A, 2B
58	44-28Ø1-ØØ	28 PIN DIP SOCKET	3D
59	44-4ØØ1-ØØ	4Ø PIN DIP SOCKET	3B, 7B, 8B, 9B
6Ø	44-16Ø1-ØØ	16 PIN DIP SOCKET	2D, 4D, 8A, 11E, 6E- 9E, 7D-9D
61	13-4735-ØØ	.47 uf CAP ELECTRO-LYTIC 16V	C14
62	4Ø-ØØØ5-1Ø	1Ø PIN MALE CONNECTOR	P21
63	37-ØØØ9-ØØ	1Ø PIN FLAT CABLE ASSEMBLY	J2, J3
64	75-ØØØ6-ØØ	HEATSINK STAVER V7-1	ONLY W/ LM277, LM278
65		E PROM 2716, FXA-2	5A
66		E PROM 2716, FXA-2	6A
67		E PROM 2716, FXA-2	7A
68	41-ØØØ3-ØØ	FEMALE 1Ø PIN	

I. PLANE INTERFACE BOARD 77-ØØØ6-Ø5

Part Number	Description
77-ØØØ6-Ø4	PLANE INTERFACE BOARD
1Ø-1Ø44-1	.1UF CAP., 25 VOLT
22-ØØØ1-Ø2	I.C. 74LSØØ
22-ØØ17-Ø2	I.C., 74LS166
22-ØØ2Ø-Ø2	I.C. 74LS245
23-ØØ45-ØØ	I.C., 6116
44-14Ø1-ØØ	14 PIN SOCKET
44-24Ø1-ØØ	24 PIN SOCKET

J. MEMORY & I/O EXPANSION BOARD 77-0015-05

Part Number	Description
77-0015-04	PCB board
22-0001-02	I.C. 74ls00
22-0010-02	I.C. 74ls32
22-0013-02	I.C. 74sl38
22-0014-02	I.C. 74sl39
22-0020-02	I.C. 74ls245
22-0031-02	I.C. 74sl74
22-0037-02	I.C. 74sl25
22-0061-02	I.C. 74ls244
09-0003-00	22 Ohm Res.Pac
09-0004-00	2.2 k Sip Pac
10-1044-10	.luf cap
13-4707-00	470uf cap ele.16v
40-0005-10	10 pin molex .156
40-0021-10	10 pin inline .100
40-0021-12	12 pin inline .100
41-0005-00	40 pin connector
44-1601-00	16 pin socket
44-2801-00	28 pin socket
23-0076-00	Data E-PROM set FXD-xx Consist of up to 24-2764 EPROMs depending on data version (xx). Location possible are 1C thru 8C, 1B thru 8B, 1A thru 8A.
24-0014-00	Prom FXD-1 12B
49-0030-05	Ribbon Cable



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

ITEM	PART NUMBER	DESCRIPTION	QTY

NOTES UNLESS OTHERWISE SPECIFIED

0 25.4mm
0 1 INCH
DEC M.M.
THIRD ANGLE PROJECTION

MATERIAL
FINISH
FILLETS MAX
BREAK CORNERS
MACHINE FINISH

TOLERANCES UNLESS NOTED
DIMENSION MM INCH
X =
XX =
XXX =
ANGLES =

DFTG DATE
CHK
ENGR
PROJ ENGR

PROPRIETARY
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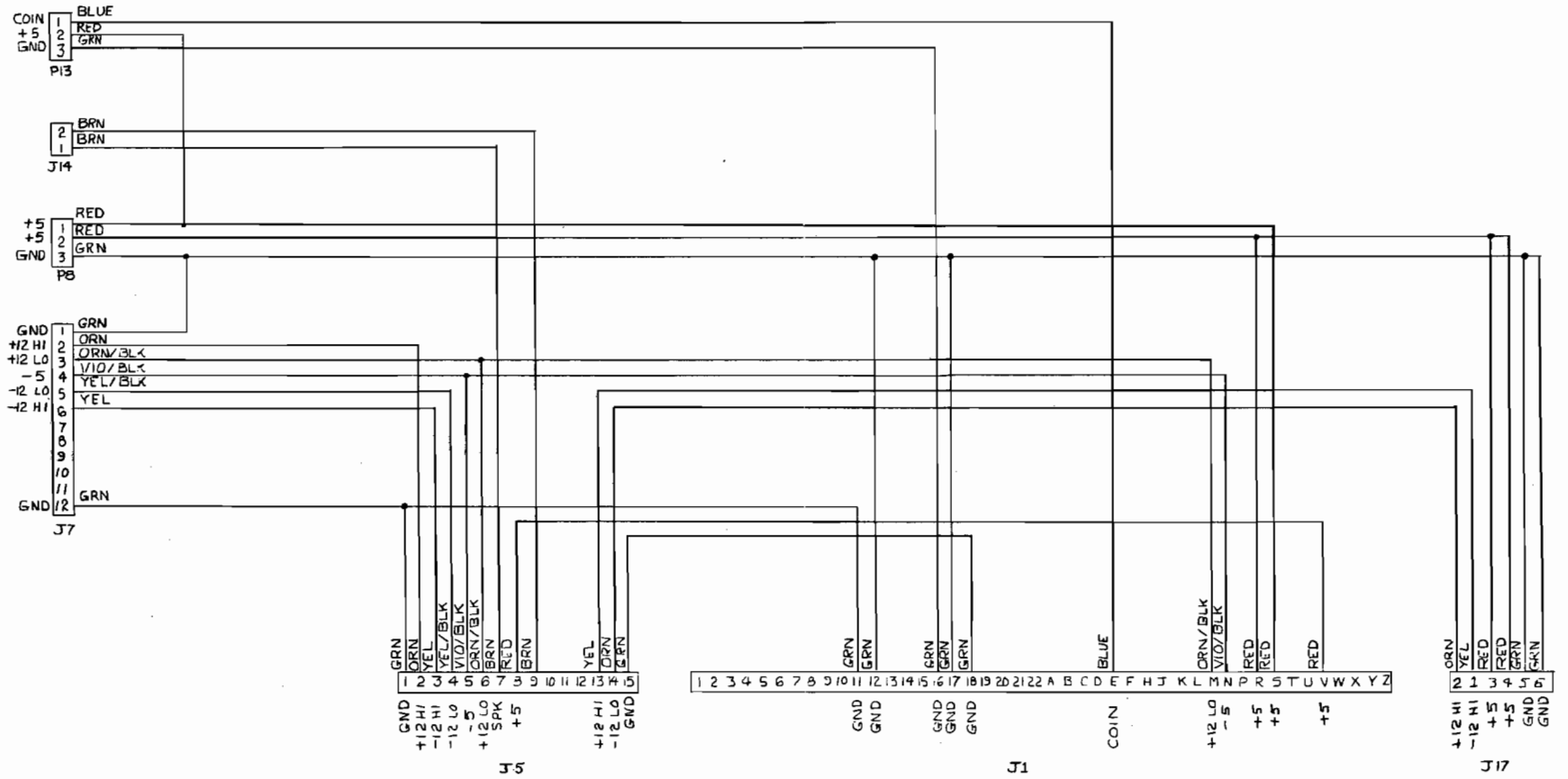
390 JAVA DR
SUNNYVALE, CA 94086
408-734-9410

TITLE WIRING DIAGRAM POWER SUPPLY ASSY.

C CODE IDENT NO. 49-0032-00

SCALE TOT SHT NEXT SHT



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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

DRAWN BY: A. PETRETTO — DATE: 3/25/83
ENGINEER: MARK VON STRIVER
SCALE: DO NOT SCALE DRAWING
DATE OF ISSUE
MATERIAL
FINISH
TOLERANCES — FRACTIONS — DECIMALS — ANGLES
CHECKED — DATE
PROJECT ENGINEER — DATE

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE: D
TITLE & DESCRIPTION: FAX MAIN HARNESS
SHEET — OF — CODE
DRAWING NO: 49-0024-00
REV: A

REVISIONS				
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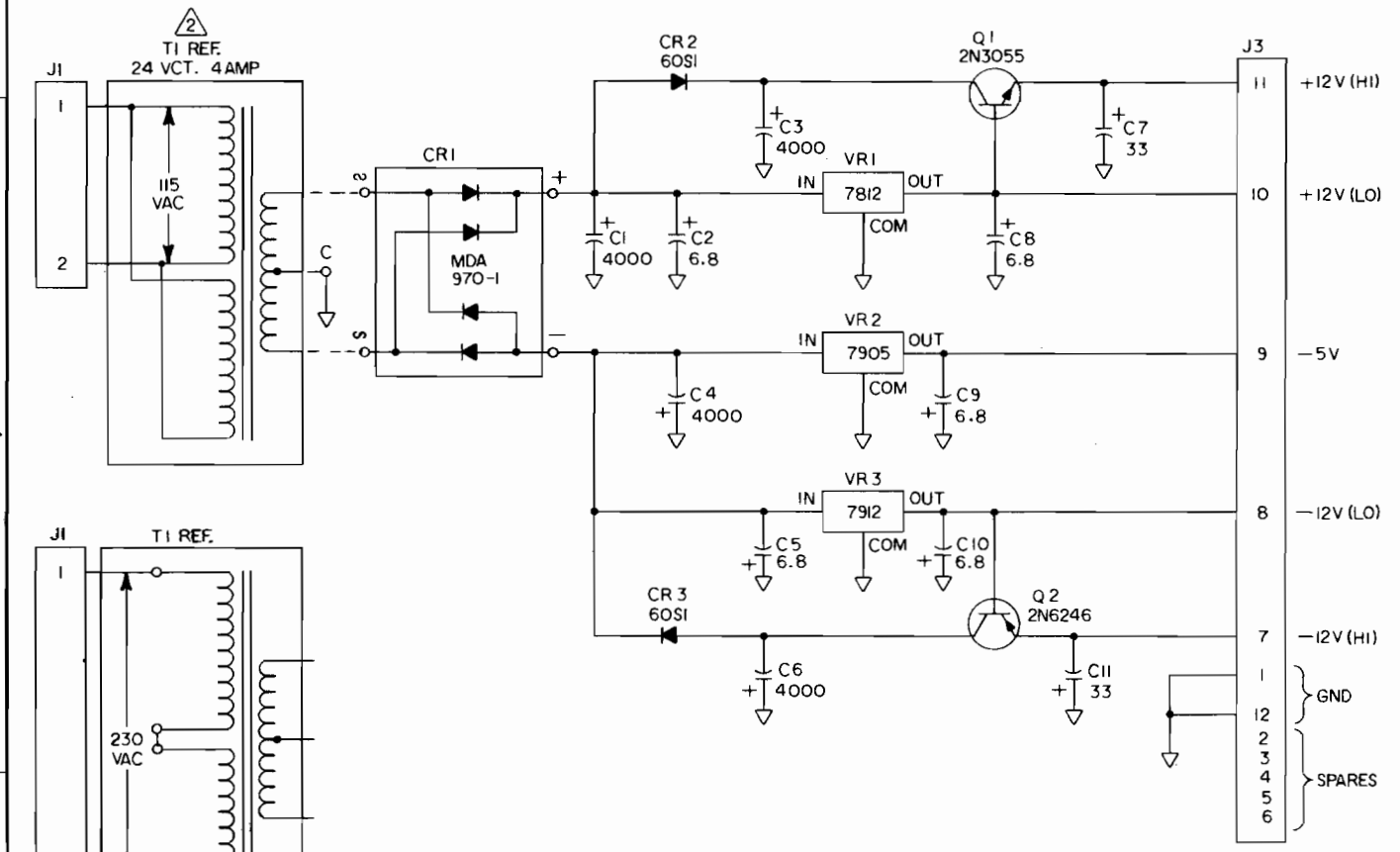
/	H	REVISED PER ECN 100235	7-30-81	[illegible]



2 SHOWN FOR REFERENCE ONLY
1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES UNLESS OTHERWISE SPECIFIED:

SIZE	C
CODE	VT
TITLE DESCRIPTION	ELECTRICAL SCHEMATIC, UNIVERSAL POWER SUPPLY
DRAWING NO	77-3365-11
SHEET	1 OF 1
REV	H
SCALE	—

DO NOT SCALE DRAWING

DATES 7-10-81 7/15/81 7/15/81

DRAWN BY
CHECKED
ENGINEER
PROJECT ENGINEER

DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST

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MATERIAL
FINISH

TOLERANCES
FRACTIONS
ANGLES
DECIMALS

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

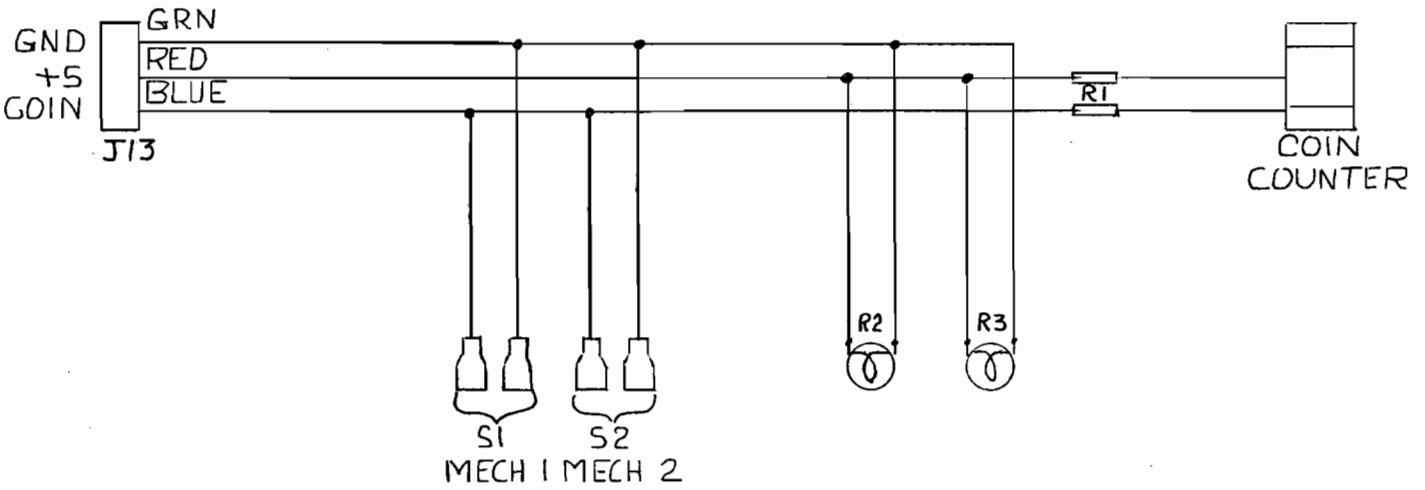
INCH
MM

PROJECTION

NEXT ASSY	USED ON
77-3365-15	VENTURE

TOLERANCES UNLESS OTHERWISE SPECIFIED

PLACES	INCH	MM
X	± /	± /
.XX	± /	± /
.XXX	± /	± /
ANGLES	± /	± /



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

ITEM	PART NUMBER	DESCRIPTION	QTY

MATERIAL
FINISH
FILLETS MAX
BREAK CORNERS
MACHINE FINISH

DEC. M.M.
THIRD ANGLE PROJECTION

TOLERANCES UNLESS NOTED
DIMENSION
.X = ±
.XX = ±
.XXX = ±
ANGLES ±

DFTG P DATE 3/31/93
CHK
ENGR MARK VON STEWER
PROJ ENGR

PROPRIETARY
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390 JAVA DR
SUNNYVALE, CA 94086
408-734-9410

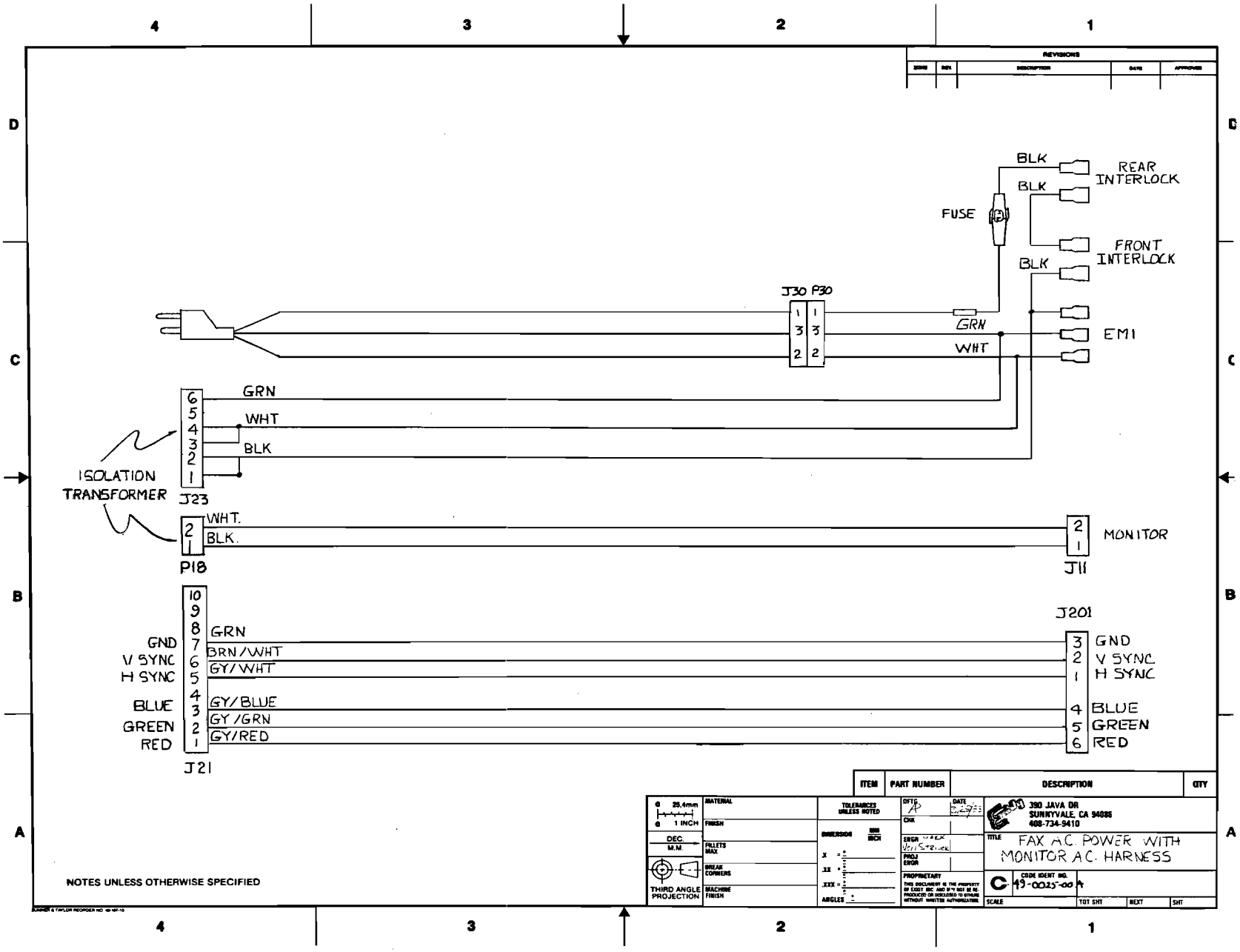
TITLE FAX COIN DOOR HARNESS

B CODE IDENT NO. 49-0023-00 A

SCALE

NOTES UNLESS OTHERWISE SPECIFIED

SUMNER & TAYLOR REORDER NO 40-107-10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REAR INTERLOCK
BLK
FUSE
FRONT INTERLOCK
BLK
J30 P30
GRN
WHT
EMI
GRN
WHT
BLK
ISOLATION TRANSFORMER
J23
WHT.
BLK.
P18
J11
MONITOR
J201
GND
V SYNC
H SYNC
BLUE
GREEN
RED
GRN
BRN/WHT
GY/WHT
GY/BLUE
GY/GRN
GY/RED
J21
GND
V SYNC
H SYNC
BLUE
GREEN
RED
ITEM
PART NUMBER
DESCRIPTION
QTY
MATERIAL
FINISH
FILLETS MAX
BREAK CORNERS
MACHINE FINISH
TOLERANCES UNLESS NOTED
DIMENSION
INCH
ANGLES
THIRD ANGLE PROJECTION
DFTG
CHK
ENGR
PROJ ENGR
PROPRIETARY
390 JAVA DR
SUNNYVALE, CA 94086
408-734-9410
TITLE
FAX A.C. POWER WITH MONITOR A.C. HARNESS
CODE IDENT NO.
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NEXT
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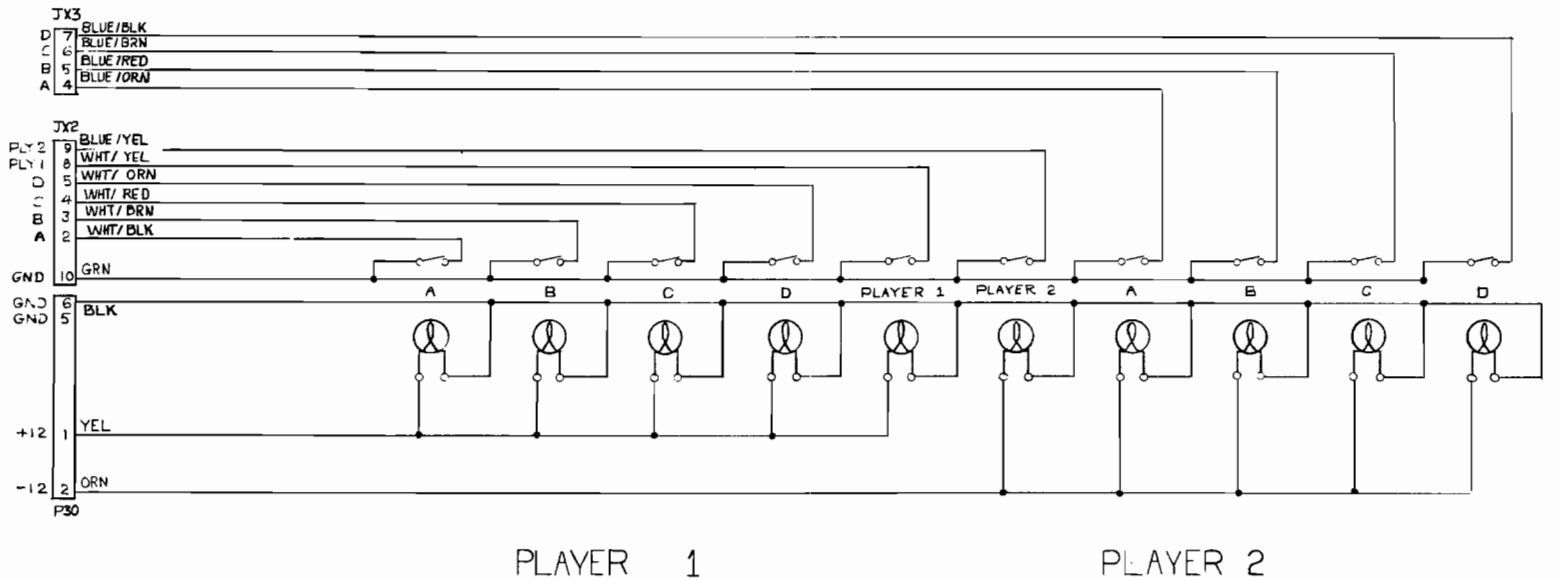

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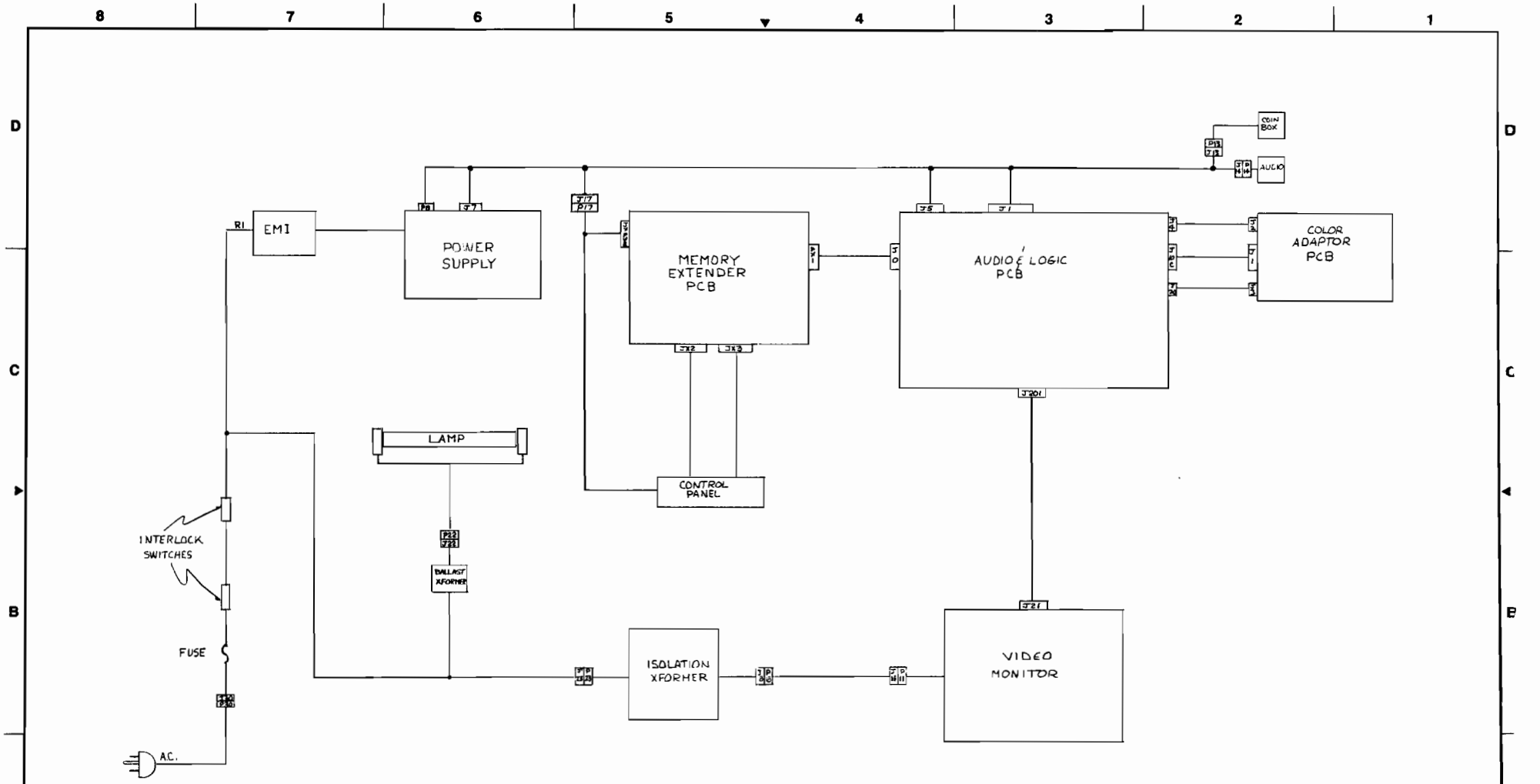
PROPRIETARY THIS DOCUMENT IS THE PROPERTY OF EEOY INC. AND MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN AUTHORIZATION.	DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST	DRAWN BY A PETRETTO CHECKED	DATE 3,25 DATE	ENGINEER MARK VON STRIVER PROJECT ENGINEER	DATE DATE	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL TOLERANCES	FRACTIONS	FINISH DECIMALS	ANGLES	390 JAVA DR SUNNYVALE CA 94086 408-734-9410	SIZE D	TITLES DESCRIPTION CONTROL PANEL HARNESS	SHEET OF	CODE	DRAWING NO 49-0026-00	REV A



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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

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CHECKED — DATE
ENGINEER: MARK VON STRIVER — DATE
PROJECT ENGINEER — DATE
SCALE: DO NOT SCALE DRAWING
DATE OF ISSUE
MATERIAL
FINISH
TOLERANCES: FRACTIONS / DECIMALS / ANGULAR

390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

SIZE: D

TITLES DESCRIPTION: FAX
BLOCK DIAGRAM

SHEET OF
CODE
DRAWING NO
REV

MODELS 13K4801, 13K4806, 13K4851, 13K4856

Power Supply Voltage and Symbols

Symbol	Voltage	Operating Circuit
⊖	15V	Vert. Osc. Sync Blanking CRT Cut-Off
⊗	130V	Horiz. Osc. Horz. Drive Horz. Output Vert. Output
⊙	175V	Video Output

★

SERVICE TECHNICIAN WARNING
X-RAY RADIATION PRECAUTION:

THIS PRODUCT CONTAINS CRITICAL ELECTRICAL AND MECHANICAL PARTS ESSENTIAL FOR X-RAY RADIATION PROTECTION.
FOR REPLACEMENT PURPOSES, USE ONLY TYPE PARTS SHOWN IN THE PARTS LIST.

⚠

CAUTION: FOR CONTINUED SAFETY, REPLACE SAFETY CRITICAL COMPONENTS ONLY WITH MANUFACTURER'S RECOMMENDED PARTS.
AVERTISSEMENT: POUR MAINTENIR LE DEGRE DE SECURITE DE L'APPAREIL NE REMPLACER LES COMPOSANTS DONT LE FONCTIONNEMENT EST CRITIQUE POUR LA SECURITE QUE PAR DES PIECES RECOMMANDEES PAR LE FABRICANT.

OSCILLOSCOPE WAVEFORM PATTERN

The waveforms shown are as observed on the wide band oscilloscope with the monitor turned to a reasonably strong signal and a normal picture. The voltages shown on each waveform are the approximate peak amplitudes.
If the waveforms are observed on the oscilloscope with a poor high frequency response, the corner of the pulses will tend to be more rounded than those shown and the amplitude of any high frequency pulse will tend to be less.

A

1V/DIV 200uSEC/DIV

TP-81

0.5/DIV 5MSEC/DIV

0351 COLLECTOR

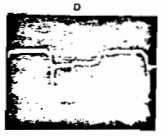
20V/DIV 10uSEC/DIV

TP-31 DC COUPLED
BOTTOM LINE = 0 VDC

2V/DIV 200MSEC/DIV

TP-82

20V/DIV 5MSEC/DIV

D

2V/DIV 10uSEC/DIV

TP-31, AC COUPLED

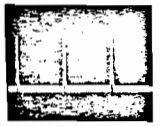
1V/DIV 200u SEC/DIV

B

0.5/DIV 20u SEC/DIV

J402-3

5V/DIV 20uSEC/DIV

NEGATIVE SIDE OF C303

2V/DIV 5MSEC/DIV

I.C. 301, PIN 13

1VDIV 200u SEC/DIV

F

1VDIV 2MSEC/DIV

I.C. 301, PIN 3

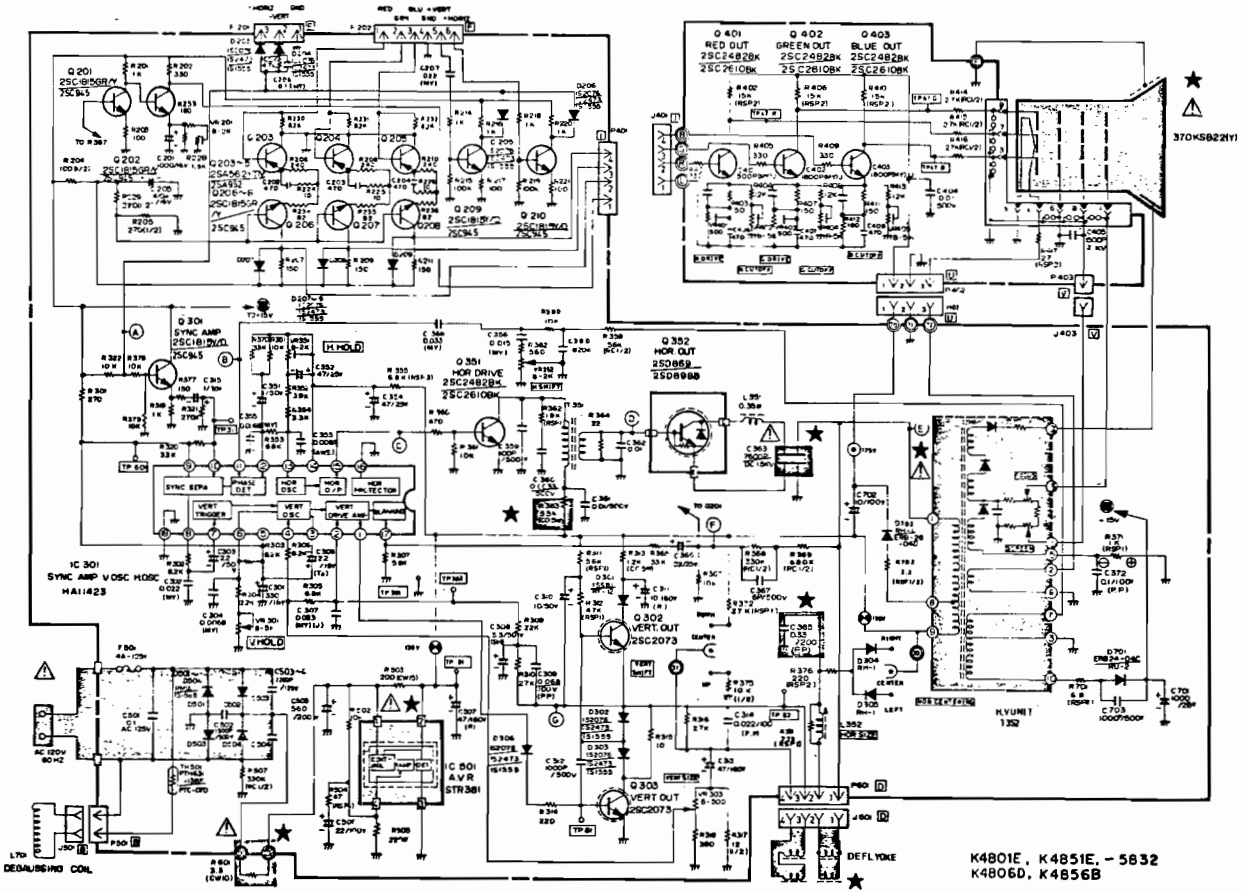
1V/DIV 5MSEC/DIV

I.C. 301, PIN 15

1V/DIV 10uSEC/DIV

F

1V/DIV 20u SEC/DIV



390 JAVA DR. SUNNYVALE, CA 94086 408-734-9410 TELEX 357-499