Cosmic Chasm

MANUAL OF ELECTRONICS

CINEMATRONICS, INC.

HIGH-SPEED VECTOR GAME SYSTEM

MANUAL OF ELECTRONICS

CINEMATRONICS, INC.

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CHAPTER 1

INTRODUCTION

The purpose of this manual is to provide a succinct and workable explanation of the operations involved in Cinematronics' general game system. Block diagrams, schematics, and a parts list are included to further this purpose. Designed around the 68000 Microprocessor, the system will be the foundation for all Cinematronics XY arcade video games in the near future. Manual inserts featuring improvements to the system and information specific to individual games will be forwarded when appropriate.

All Cinematronics games are shipped in ready-to-play condition. Each game should, however, undergo a brief inspection upon arrival. The following list may be used as a guideline:

1. Adjust the +5V DC supply to 4.8-5.1V DC.

2. Make sure all connectors, cables, and socketed ICs are seated properly.

3. Make sure that the audio and game personality modules are securely anchored with both mounting screws. Verify that standoffs are not flexing the game processor board, causing poor game personality module connection.

4. Lock the +5V DC adjustment pot in position with nail polish or a similar compound.

5. Note the game serial number for any future servicing needs.

Now, before continuing, read through the following explanations of the conventions used in this manual:

1. The heading of each major section is followed by one or more numbers in parenthesis. These numbers are schematic page and location references. The first number(s) are the page numbers. Any specific schematic location numbers and letters used are separated from the page numbers by hyphens.

2. All active-low signals are marked by minus signs after their mnemonic names.

3. Individual pin numbers referred to are separated from their IC numbers by hyphens. For example, U1-2 is the same as U1, pin 2.

CHAPTER 2

GAME PROCESSOR BOARD

TABLE 2-1: 68000 SIGNAL DESCRIPTION*

The following table lists the 68000 input and output signals, their mnemonic names, and brief descriptions of their functions.

SIGNAL	MNEMONIC	DESCRIPTION
ADDRESS BUS	A1-A23	23-bit, unidirectional, three-state bus, capable of addressing 8 mega-words of data. Provides the address for bus operation during all 68000 cycles.
DATA BUS	D0-D15	The general data path. 16-bit, bidirectional, three-state bus, capable of transferring and accepting data in either word or byte length.
ASYNCHRONOUS BUS CONTROL		
Address Strobe	AS-	Indicates a valid address on the address bus.
Read/Write	R/W-	Defines the data bus transfer

		as a read or write cycle.
Upper and Lower Data Strobes	UDS-, LDS-	Control the data on the data bus. When the instruction specifies a word operation, the processor accesses both bytes and asserts both data strobes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to access, then issues the data strobes required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is used. When the A0 bit equals one, the lower data strobe is used.
Data Transfer Acknowledge	DTACK-	This input indicates to processor that data transfer is completed, causing bus cycle to be terminated.
BUS ARBITRATION CONTROL CIRCUIT		
Bus Request	BR-	This input indicates to processor that the Refresh Processor desires to become the bus master.
Bus Grant	BG-	This output indicates to the Refresh Processor that the processor will release bus control at the end of current bus cycle.
Bus Grant Acknowledge	BGACK-	This input indicates that the Refresh Processor has become bus master.
INTERRUPT CONTROL	IPL0- IPL1- IPL2-	These input pins indicate the encoded priority level of a device requesting interrupt. Level four is the highest priority, while level zero indicates that no interrupts are requested. The least significant bit is given in IPL0; the most significant

		is contained in IPL2.
SYSTEM CONTROL		
Bus Error	BERR-	Tied high and not used. A bus error condition will be handled by the system's Watchdog Reset.
Reset and Halt	RESET-, HALT-	Applied simultaneously, these external signals cause a total system reset of the processor and external devices.
M6800 PERIPHERAL CONTROL		Three control signals used to allow the interfacing of synchronous M6800 peripheral devices with the asynchronous MC68000.
Enable	E	The standard enable signal common to all M6800 devices. The period for this output is ten MC68000 clock periods (six clocks low; four clocks high at 800 KHz).
Valid Peripheral Address	VPA-	This input indicates that the device or region addressed is a M6800 family device and that data transfer should be sychronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.
Valid Memory Address	VMA-	This output is used to indicate to M6800 peripheral devices that there is a valid address on the address bus, and that the processor is synchronized to enable. This signal only responds to a valid peripheral address input which indicates that the peripheral is a M6800 family device.
PROCESSOR STATUS	FC0, FC1, FC2	These function code outputs indicate the state and the

		cycle type currently being executed. The information indicated by the function code outputs is valid whenever the address strobe is active. When all three outputs are high, an interrupt acknowledge cycle is being performed.
CLOCK	CLK	The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency of 8MHz.

*All information included in this table has been taken directly from: MOTOROLA DATA SHEET, MOTOROLA Semiconductor Products Inc., copyright 1982.

PART I: THEORY OF OPERATION

A. 68000 MICROPROCESSOR (1,2)

Two processors work together on the Game Processor Board: the 68000 central processor and the Refresh Processor. A standard microprocessor, the 68000 is based upon the 16-bit, 68000 microprocessor chip. A block diagram of the 68000 system's major functional units, including address and data bus buffers, is shown in Figure 1. The locations of the blocks in the diagram approximate their actual positions on the right side of the Game Processor Circuit Board. Detailed descriptions of the functions of and relations between each block and a discussion of the Refresh Processor system follow this section.

Two Programmable Array Logic circuits (PALs) are used on the Game Processor Board: U76 and U77. The PAL circuits consist of an array of AND and OR circuits, whose interconnections are programmed to provide the desired logic function of the inputs to the outputs. U76 provides primary address decoding for EPROM (OEP-) and RAM (RAMW-, OER-, RAMS-). ROMMS- is the basic decode signal for the lower portion of the 68000 memory map which includes EPROM and miscellaneous circuitry. RAMAS- is the corresponding signal for the RAM and Audio that constitute the upper portion of the memory map.

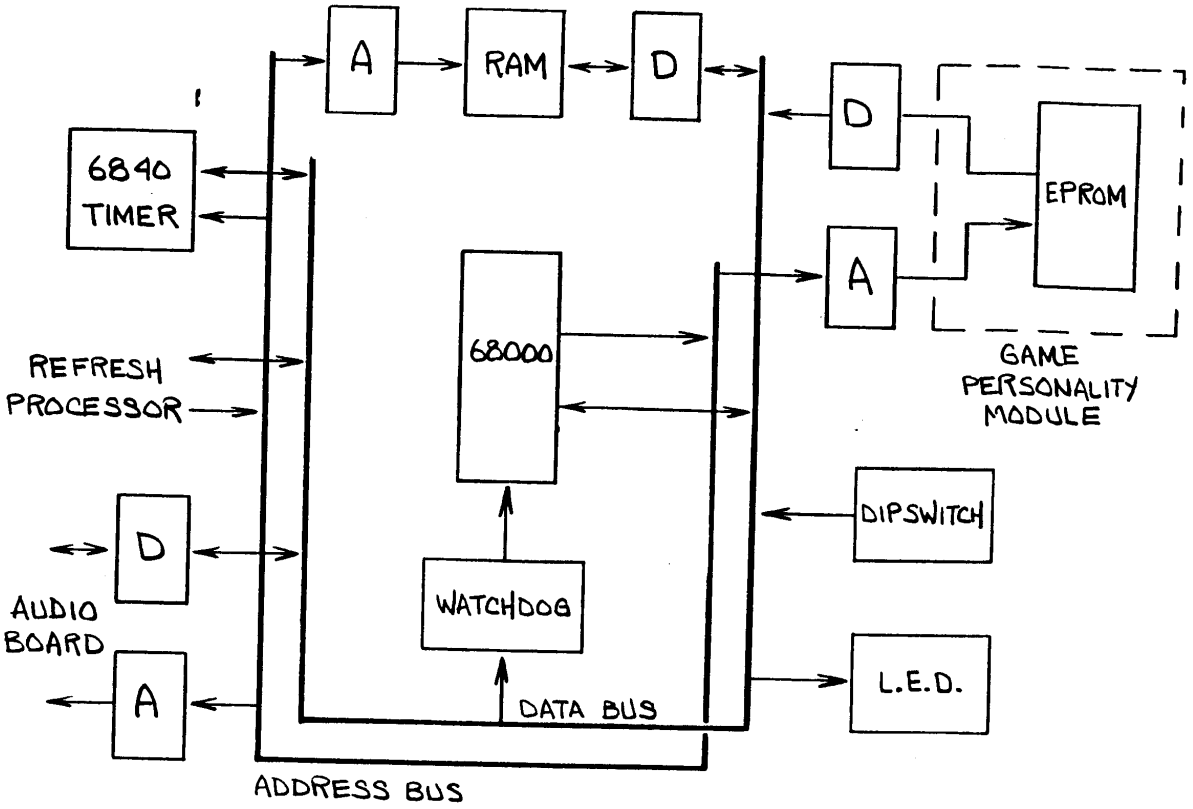
U77, the second PAL, generates the DTACK- signal required in the 68000 bus cycle operation. It determines whether or not delays need to be introduced for slow EPROMs and/or the Audio Board Interface. U77 also provides three signals used in Refresh Processor operations, QAS, QACK-, and QACK2-, along with a decode signal for the miscellaneous circuitry, MISC-. MISC- is further decoded through U74 to produce enables for the 6840 Timer (TS-), the Refresh Processor Control/Status (RPS-), the dipswitch/LED (DS-, LED-), and the Watchdog Timer. A shift register, U91, provides delays from the start of a bus cycle which are used in the generation of DTACK- and Refresh Processor signals.

B. GAME PERSONALITY MODULE (Game Personality Schematics)

The program stored in the EPROMs that make up this unit of the Game Processor Board determines the character or "personality" of the game and thus changes from game to game. There may be as many as sixteen EPROMs on the personality module, and these may be either of two types: 2732 (4K x 8) or 2764 (8K x 8).

FIGURE ONE

68000 PROCESSOR



The schematics and printed circuit layout for the Game Personality Module are for the 28-pin 2764 devices. The pinout for the 2732's is a subset of these, with the chips mounted in the lower 24 pins of the 28-pin site. The sixteen EPROMs are organized as eight pairs of 2 byte words. U1 through U8 are upper bytes, and U9 through U16 are lower bytes. The base address of the EPROM is location 0 in the system memory map.

C. RAM (3)

The RAMs on the Game Processor Board function as temporary storage and contain tables of drawing instructions. A RAM may consist of as many as ten 4016 or 6116 chips, both of which are organized as 2K x 8 bits.

The schematics and printed circuit layout for the RAMs are for 28-pin 8K X 8 devices to be used in the future. The pinout for the 4016/6616s is a subset of these, with the chips mounted in the lower 24 pins of the 28-pin site. The ten RAMs are organized as five pairs of two byte words. U7 through U11 are upper bytes, and U21 through U25 are lower bytes. The RAM base address is FFB000 hexadecimal in the memory map.

Provision has been made in some boards for battery backup of two of the RAM chips, U11 and U25, during power-down. If this option is not furnished, CR2 is replaced with a jumper, and U5 is deleted with pins 3 and 4 jumped together. In addition, BT1, R26, CR1, R25, and RP1-RP4 are deleted.

D. 6840 TIMER (3)

A programmable timer, the 6840 (U19) determines the rate of drawing by generating an interrupt at intervals of approximately twenty-five milliseconds. The 6840 has three sixteen-bit channels which are programmed through sixteen eight-bit control, status, and data registers. These registers are addressed by the three least significant processor address bits, A1-A3, and the read/write line. They are accessed on the lower data byte D0-D7. Eight of these registers may be read, and the other eight written into, by the 68000.

The base address of the eight timer registers is 40000 hexadecimal. The 6840 uses the 68000's E Clock as its input. The E Clock is one-tenth the processor's operating frequency, which is 800 KHz for an 8MHz 68000.

E. WATCHDOG RESET (2)

Sometimes referred to as the "Sanity Timer", the Watchdog Timer automatically resets the game processor in the case of system failure. The Watchdog is serviced by writing a "1" to data bit D8 at address

70000 hexadecimal. Derived from the 68000's E Clock, the time-out interval is approximately 164 milliseconds. If the Watchdog is not serviced again in that interval, a system reset is performed.

A system reset asserts the 68000 reset and halt lines to reset the 68000 and its software. It also initializes random sequential logic on the game processor and resets the Z80 Audio Board. System reset also occurs when power is first applied to the system and when the Manual Reset Switch, S2, is depressed.

F. DIPSWITCH AND LED (3)

An eight-position dipswitch, S3 provides the 68000 with game configuration input. The LED (DS1) provides output from the 68000. Its seven- segment and decimal-point display indicates various overload or error conditions. The decimal point itself is tied directly to the Watchdog Timer. See the Table 2-2 below for a list of the various LED displays and their explanations.

The dipswitch and the LED occupy the same address in the system memory map: the lower byte (D0 through D7) of location 60000 hexadecimal. The dipswitch is read, and the LED is written into, at this location. A logic "0" is an ON in both functions.

TABLE 2-2

DISPLAY	EXPLANATION
O	DRAWING OVERLOAD/AUDIO NOT READY
E	ERROR CONDITION/PROCESSOR TRAP
BLINKING DECIMAL	WATCHDOG RESET

G. INTERFACE TO THE Z80 AUDIO PROCESSOR BOARD (3)

The interface to the Z80 Audio Processor Board consists of eight bits of bidirectional data (AD8 through AD15) and eight bits of address (AA1 through AA8). Two control signals are present: an audio I/O strobe (AIOS-) to indicate valid address/data, and a read/write line (AR/W-) for data transfer direction. An interrupt (IA-) from the Audio Board to the Game Processor and a reset signal from the Game Processor to the Audio Board are also provided. The 256 byte Audio Interface is found in the upper bytes (D8 through D15) of the memory map, starting at address F80000 hexadecimal.

H. REFRESH PROCESSOR (4,5,6)

Built from discrete TTL logic, the Refresh Processor specializes in drawing, or "refreshing", the picture on the color XY monitor. A block diagram of the Refresh Processor is shown in Figure 2. The diagram illustrates the Refresh Processor system's major functional blocks in their approximate positions on the left side of the Game Processor Circuit Board.

The Refresh Processor fetches its drawing instructions from a table, or queue, in the 68000 RAM by accessing 16-bit words from the 68000 data bus. Three of the sixteen bits carry operation code, twelve carry data, and one is unused.

The three bits of operation code decode in the Instruction Decoder into the following eight operations:

Initial X Position
Initial Y Position
X Drawing Rate
Y Drawing Rate
Color Information
Line Length
Control Instructions: JUMP and HALT

The twelve bits of data go onto the vector bus as an operand for the desired operation. Note, however, that the HALT operation has no operand.

The X and Y rate operations determine the slope of the line drawn by regulating the rate at which the X and Y position counters are incremented. The color information breaks down into three four-bit fields: Red, Green, and Blue. The line length operation is always last, indicating the end of the instruction sequence and triggering the circuitry to begin drawing the line. The JUMP instruction causes a jump to a specified RAM address for the next drawing instruction. When the Refresh Processor receives a HALT instruction, it sends an interrupt to the 68000 Microprocessor and ceases to draw.

Blanking is an automatic function of the Refresh Processor. There are two kinds of blanking: X/Y and Dot. If a line draws up to the edge of the monitor screen, the X and Y blanking circuitry guarantees a clean cutoff and eliminates wraparound by holding the X/Y counters in position and blanking the beam. Dot blanking prevents dots from appearing at the vertices of angles formed when two lines meet on the screen.

The X and Y DACs are 561-type, ten-bit digital to analog converters. The color DACs are three four-bit discrete digital to analog converters. The conversions are accomplished by combining digital open collector outputs in a weighted resistor network.

FIGURE TWO

REFRESH PROCESSOR

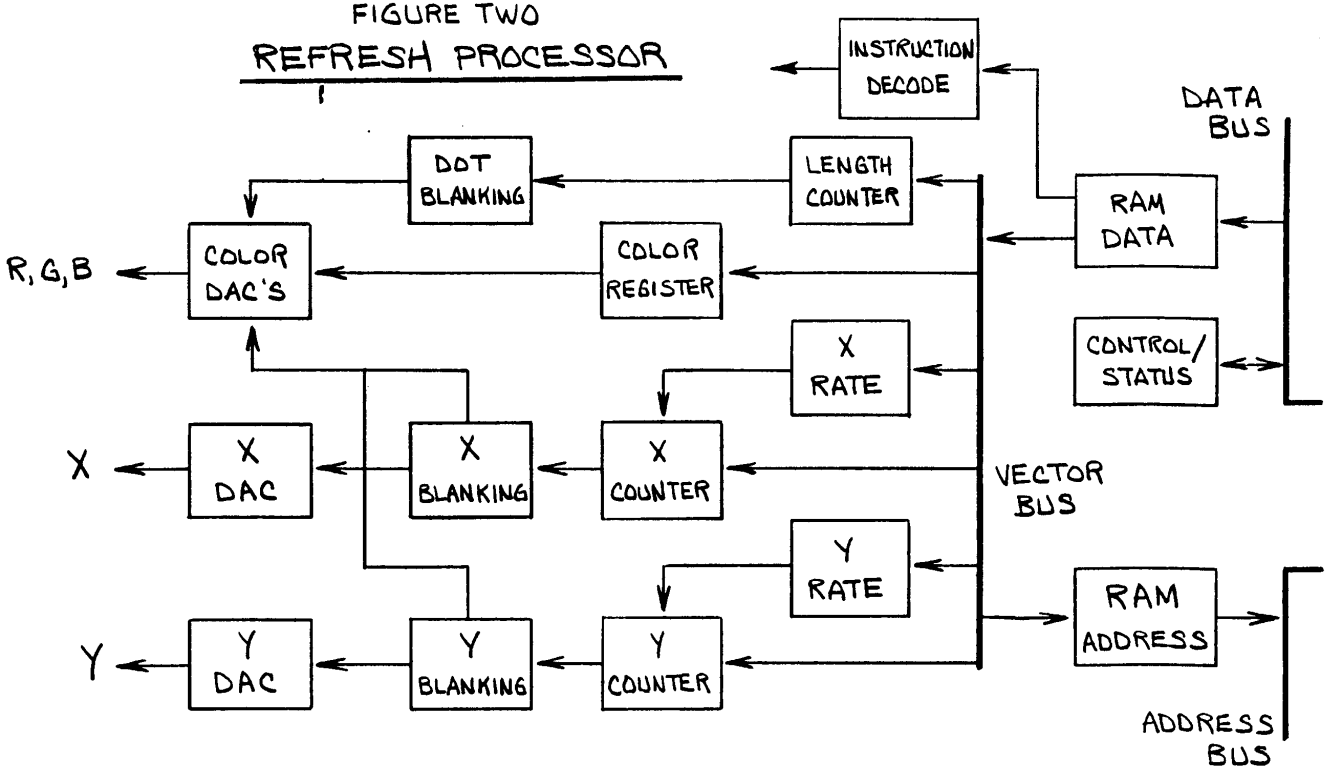


TABLE 2-3: REFRESH PROCESSOR SIGNALS

SIGNAL	MNEMONIC	DESCRIPTION
Queue Address Strobe	QAS-	Controls the address strobe signal during Refresh Processor operation.
Queue Acknowledge	QACK-	Clocks instructions into RAM data register (U59, U60) and increments RAM address counters (U85, U86, U103, U104).
Queue Acknowledge Two	QACK2-	Enables intruction decoder U53.
Refresh Processor Bus Request	RBR-	Indicates that the Refresh Processor wants to fetch an instruction from RAM.
Refresh Processor Interrupt	IR-	Indicates that the Refresh Processor is finished drawing.
Draw	DRAW-	Active when a line is being drawn.
Vector Line Length	VLNTH-	Loads length counter (U41, U42, U52) and begins drawing.
X Position	X-	Loads X position counters (U36, U48, U55).
X Drawing Rate	DELTA X	Loads rate at which the X-rate generators will operate.
Y Position	Y-	Loads Y position counters (U69, U80, U98).
Y Drawing Rate	DELTA Y	Loads rate at which the Y-rate generators will operate.
Line Color	COLOR-	Loads color registers (U32, U33).
Jump to other RAM locations	JUMP-	Loads RAM address counters with jump address.
Queue Halt	QHALT-	Stops Refresh Processor Operations.
Queue Reset	QRST-	Indicates that the Refresh Processor is not running.
Queue Start	QSTRT-	Starts Refresh Processor Operation.
Clear Queue Counter	CLQCNT-	Disables RAM address buffers

		(U72, U73).
Start Drawing a Line	START-	Allows rate multipliers to increment the position counters.
Dot Blanking	DOTBLK-	Disables monitor guns while they are not drawing a line.
6MHz Clocks	6MHz A, B, C, D	Buffers clocks used throughout the Refresh Processor System.
Y Position Blanking	INT BLK Y	Indicates that the Y-beam position has gone out of bounds.
X Position Blanking	INT BLK X	Indicates that the X-beam position has gone out of bounds.
Rate Y Rate X Position up/down count for Y and X	RATY- RATX- Y UP/DN X UP/DN	Control the incrementing and decrementing of the Y and X position counters.

PART II: TROUBLESHOOTING PROCEDURES FOR THE GAME PROCESSOR BOARD

A. 68000

Put the 68000 in FREE-RUN test mode by moving the W6 jumper to the test position and removing the S1 dip jumper to disable unwanted signals. Reconnect the DTACK- signal in one of two ways: either by jumpering P4A, pins 10 and 11, or by replacing the S1 jumper with an eight-position dip switch and turning only switch 1 on. The second method lends more flexibility in testing, as it allows for individual enabling of signals. The abbreviated names of the disabled signals are printed on the circuit board next to S1.

In the FREE-RUN mode, a pseudo NO-OP is forced onto the 68000 data bus. All other devices capable of driving the data bus are disabled. While free-running, the 68000 should march through its address space, toggling the address lines along with the address and data strobes and the DTACK- line. The 68000 signals are grouped together on the P4A and P4B test connectors. Table 2-4 shows the layout of P4A, P4B, and other miscellaneous test points.

TABLE 2-4: 68000 TEST CONNECTORS

SIGNAL	PIN		SIGNAL	SIGNAL	PIN		SIGNAL
D4	1	2	D3	D5	1	2	D6
D2	3	4	D1	D7	3	4	D8
D	5	6	AS-	D9	5	6	D10
UDS-	7	8	LDS-	D11	7	8	D12
R/W-	9	10	DTACK-	D13	9	10	D14
(DTACK-)	11	12	BG-	D15	11	12	GND
(BG-)	13	14	BGACK-	GND	13	14	A23
(BGACK-)	15	16	BR-	A22	15	16	A21
(BR-)	17	18	+5VDC	+5VDC	17	18	+5VDC
+5VDC	19	20	CLK	A20	19	20	A19
GND	21	22	GND	A18	21	22	A17
HALT-	23	24	RESET-	A16	23	24	A15
VMA-	25	26	E	A14	25	26	A13
VPA-	27	28	BERR-	A12	27	28	A11
IPL2-	29	30	IPL1-	A10	29	30	A9
IPL -	31	32	FC2	A8	31	32	A7
FC1	33	34	FC	A6	33	34	A5
A1	35	36	A2				
A3	37	38	A4				
SPARE	39	40	SPARE				

NOTE: Signals in parentheses are taken on the other side of the S1 shunt.

TEST POINTS

TP1	AS-
TP2	CLK (8MHz)
TP3	6 MHz A
TP4	A23
TP5	QRST-
TP6	START-

B. REFRESH PROCESSOR

Begin by determining whether or not the Refresh Processor is running. If it is running, QRST- at test point 5 should be toggling. If QRST- is not toggling, but is low, the Refresh Processor is not running. If QRST- is not toggling, but is high, the Refresh Processor is stuck in RUN mode.

Next, check to see if the RBR signal is toggling. If is not toggling, but is low, the Refresh Processor is not requesting the 68000 bus. If RBR is not toggling, but is high, the Refresh Processor is stuck somewhere in the 68000 bus request sequence.

If the RBR signal is working, but the Refresh Processor is still not drawing, make sure that it is not stuck at some point in the bus arbitration process by checking arbitration signals BR-, BG-, and BGACK-.

If the Refresh Processor is getting the 68000 bus, check Refresh Processor signals QAS, QACK-, and QACK2- in the Refresh Processor instruction- fetch process. All of these lines should be toggling.

If all of the lines are toggling, check Instruction Decoder U53 to see if any of the Refresh Processor registers are being loaded with instruction operands. If U53 is decoding only one type of instruction, verify that the RAM address counters are counting.

Lastly, check the X, Y, and Red, Green, and Blue outputs. If there is no X deflection, trace back through the X Position and X Rate generator circuitry. If there is no Y deflection, trace back through the corresponding Y circuitry. If there are no color outputs, trace back through the color DACs and color registers.

CHAPTER 3

Z80 AUDIO PROCESSOR BOARD

The Z80 Audio Processor Board is divided into two sections: the 68000 section and the Z80 section. An extension of the 68000's input/output system, the 68000 section is used to read the player controls and to control the Coin Counter. The Z80 section is used to generate audio and to detect coins. The two sections interact via the Command and Status Registers. Figures 3 through 5 illustrate the major functional blocks of the Z80 Audio Processor Board.

PART I: THEORY OF OPERATION FOR THE 68000 SECTION OF THE Z80 AUDIO PROCESSOR BOARD

A. READ DECODING (5-B4)

There are eleven eight-bit readable registers on the 68000 section of the Z80 Audio Board. Each of these registers has a unique address. (See Table 3-1). The two Read Decoders, U52 and U55, decode the address from the 68000 into eleven separate select lines, one line for each of the readable registers.

When the 68000 needs to read a certain register, the two Read Decoders are first enabled by a combination of Read/Write (R/W-) high and Address Strobe low. A single Read Decoder output is then driven low, corresponding to the selected register. The data from the selected register is gated onto the local 68000 Data Bus Lines, CD8+ through CD15+, then transferred to the 68000 Board via U65. A high on Direction Control U65-1 and a low on U65-19 enable this transfer.

For an example of the above process, suppose the 68000 needs to read the STATUS HIGH register. The 68000 first sends an address word of "01" HEX to the Audio Board via U3, pins 18-32, then to Read Decoders U52 and 55. Address line AA1 goes high, all other address lines low. U52-14 subsequently goes low, thereby selecting the READ STATUS HIGH register. At this time, all outputs on the other Read Decoder, U55, and on the Write Decoder, U54, are high. The data from the READ STATUS HIGH register is then transfered to the 68000 Board in the manner described above.

MAJOR SECTIONS

Z80 AUDIO BOARD

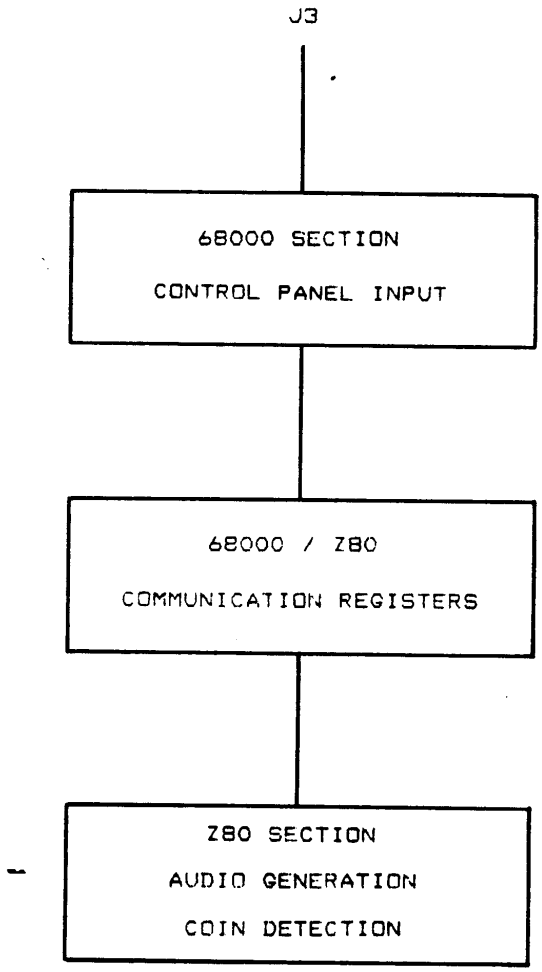
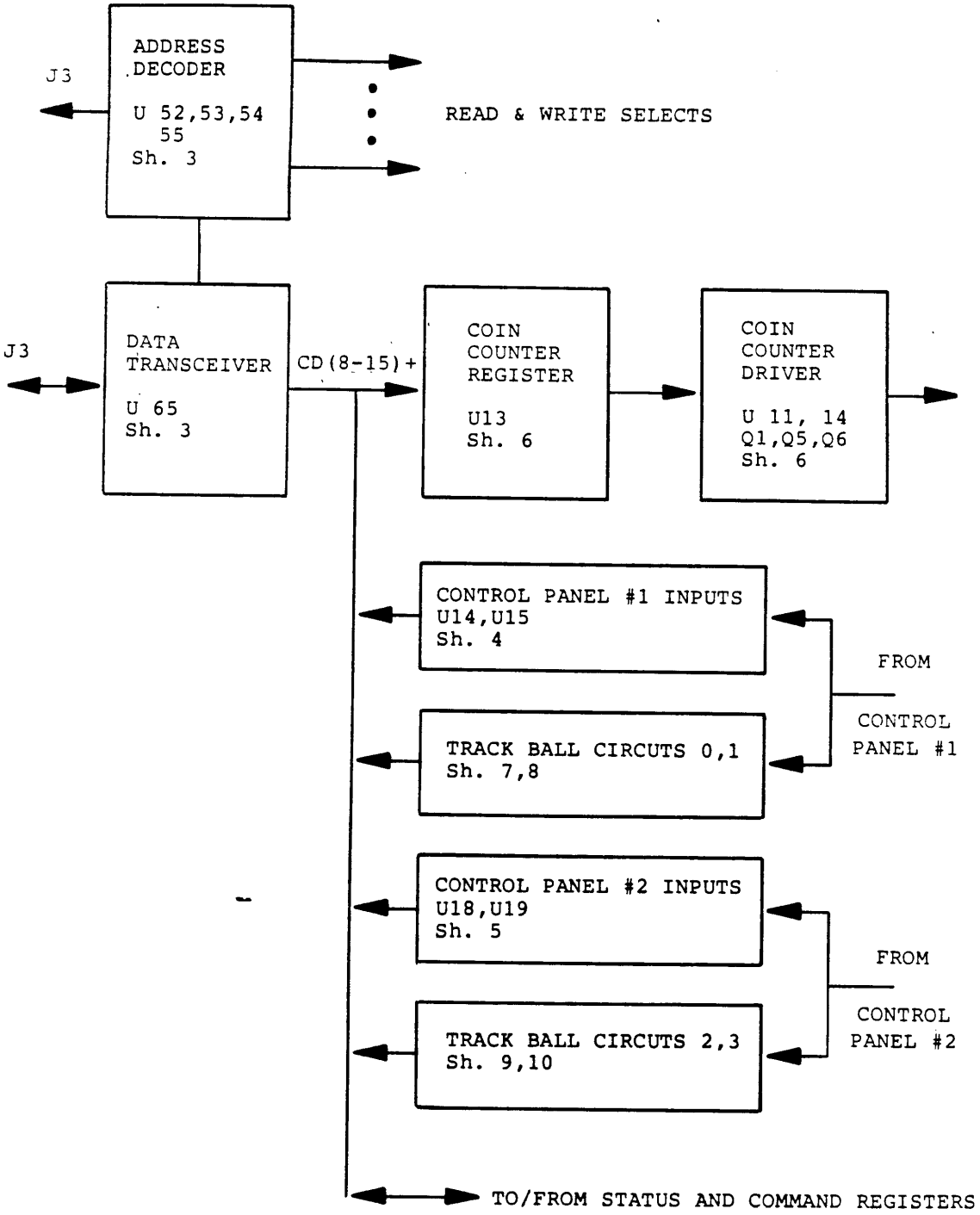


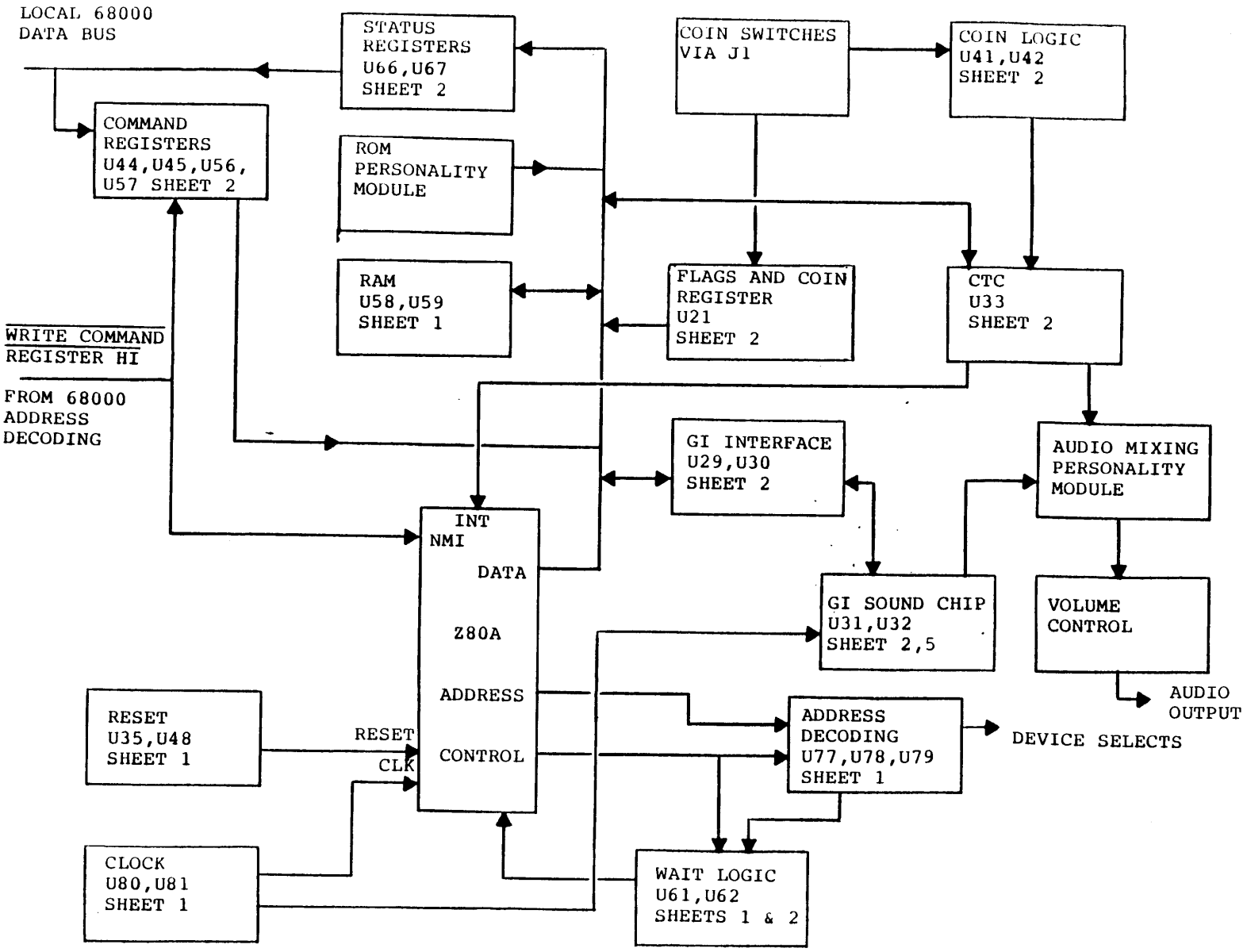
FIGURE THREE

FIGURE FOUR

BLOCK DIAGRAM - Z80 AUDIO - 68000 SECTION



BLOCK DIAGRAM - Z80 AUDIO - Z80 SECTION FIGURE FIVE



B. WRITE DECODING (5-C4)

The Write Decoding process is similar to that of Read Decoding. Here, there are three writeable registers. (See Table 3-2). Each of these has a unique address. The address lines from the 68000 to these registers pass through the Write Decoder, U54. In the Write Decoder, each address line is broken down into three select lines, one line for each of the three writeable registers.

When the 68000 needs to write into a certain register, U54 is enabled by a low on U54-5 R/W- and a low on U54-4. U54 then drives one of its output pins low to select one of the three output/writeable registers. The 68000 data passes via U65 to the local Data Bus lines, CD8+ through CD15+, then into the selected register. A low on U65-1 R/W- and a low on U65-19 enable this transfer.

For example of the Write Decoding process, suppose an address of "0" is selected by the 68000. All address lines are then low, causing U54-15 to go low. A write of 68000 data is strobed into the WRITE COMMAND LOW register, U56, on the Audio Board from the local 68000 Data Bus lines, CD8+ through CD15+. A high-going edge on U56-11, CAS+, enables this transfer.

NOTE: A high-going edge on the signal CAS+ is equivalent to a low-going edge on the signal AIOS, which enters the Audio Board at J3-36 from the 68000.

TABLE 3-1: 68000 READABLE REGISTERS ON THE AUDIO BOARD

ADDRESS ON LINES AA1-AA8	IC	8-BIT REGISTER	DESCRIPTION
0	U67	STATUS LOW	8-BIT DATA WORD FROM Z80 TO 68000
1	U66	STATUS HIGH	8-BIT DATA WORD FROM Z80 TO 68000
2	U27	FLAG REGISTER	SLAM FLAG, TEST SWITCHES, STATUS FULL, COMMAND FULL
3	NOT USED----------		
4	U14	CONTROL PANEL 1	8 SWITCH INPUTS (CONFIGURABLE)
5	U15	CONTROL PANEL 1	8 SWITCH INPUTS (NON-CONFIGURABLE)

6	U18	CONTROL PANEL 2	8 SWITCH INPUTS (CONFIGURABLE)
7	U19	CONTROL PANEL 2	8 SWITCH INPUTS (NON-CONFIGURABLE)
8	U17	TRACK-BALL 0	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
9	U16	TRACK-BALL 1	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
10	U21	TRACK-BALL 2	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
11	U20	TRACK-BALL 3	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL

TABLE 3-2: 68000 WRITE-ABLE REGISTERS ON THE Z80 AUDIO BOARD

ADDRESS	IC	REGISTER	DESCRIPTION
0	U56	COMMAND LO	8 BIT DATA WORD FROM 68000 TO Z80
1	U44	COMMAND HI	8 BIT DATA WORD FROM 68000 TO Z80
2	U13	DRIVER REGISTER	CONTROLS COIN COUNTER AND LAMPS.

C. COIN COUNTER CIRCUIT (4-B2)

Driver register U13, one half of U11, one half of U41, one quarter of U26, Q5, Q6, and Q1 together form the Coin Counter circuit. This circuit is always reset at power-up: the reset pulse sets U11-5 high and U41-5 low, disabling the drive to the Coin Counter by guaranteeing a low at U26-3.

When driver register U13 is written into by the 68000 for the first time after reset, a low is written into U11-2, causing U11-5 to drop low, U41 to be present via U41-4, and U26-3 to go high. Driver register U13 now controls the Coin Counter.

One count of the Coin Counter is accomplished by first turning the Counter on, then off. Assuming that a "1" is written into U13-3, U13-2 goes high, causing Q5 and Q6 to turn on. The collector of Q6 is now at a potential of 1 volt or less. This low voltage causes current to be pulled through R47, thereby turning on Q1. The collector of Q1 goes from 0 volts to very near +15 volts to energize the coil in the mechanical Coin Counter. The Coin Counter is now on.

The Coin Counter de-energizes or turns off when the 68000 writes a "0" into U13-3, causing U26-3 to drop low, and Q5, Q6, and Q1 to turn off.

NOTE: Once U41-5 goes high, it stays high until reset occurs. Also, a toggling of U11-5 has no effect on the circuit's performance.

D. TRACK BALL/SHAFT ENCODER CIRCUIT (7,8)

There are four identical Shaft Encoder circuits. The following is a description of the Track-Ball 0 circuit:

Each Shaft Encoder circuit has two input-filtering networks. One of these is composed of U3, pins 8-10, U4, pins 10-11, R14-R17, CR13, and C4. The input signal to this network is differentiated by C4, then fed to U3-10 via R15. Wired as a comparator with hysteresis, U3 compares the input signal against a reference voltage of 1.75 volts generated by R1 and R2. The output of the comparator, U3-8, is in phase with the input signal. Inverter U4 supplies additional drive before the signal is sent to direction Flip Flop U5. The inputs to U5, pins 11 and 12, are approximately 90 degrees out of phase with each other. The output of the direction Flip Flop, U5-9, is high when the Shaft Encoder is turned clockwise, low when counterclockwise.

E. COUNTERS U2 and U7 (7A-3)

U2 and U7 are cascaded to form an 8-bit up/down Counter. The counting speed is determined by the rate at which clock pulses arrive at pin 14 of both IC's. The direction of the count, either increasing or decreasing, is determined by the state of the up/down input, pin 5 on both IC's. An increasing count occurs when pin 5 of both counters is low. The output of the two counters is fed to the 68000 Board when Bus Driver U17 is enabled by a low on pins 1 and 19 on U17.

F. LAMP REGISTER (4-C1)

Four bits of U13 are used as a Lamp Register. Each player panel may have as many as two LEDs installed in it. To turn on Lamp 0, the 68000 sets U13-6 high, forcing pin 12 on Lamp Driver U12 low and drawing current through R48. The other bits of the Lamp Register operate in a similar fashion.

The LED anode connects to 5 volts on the control panel, the cathode to R48 via J1-19 of the Audio Board.

Note that U12 may not be loaded in games that have no LEDs in their player panels.

G. SLAM SWITCH (4-A3)

Contact bounce at the Slam Switch on the Coin Door sets the Slam Flag. One side of the Slam Switch is connected to ground; the other enters the Audio Board via J1-J. The SLAM- signal, J1-J, is normally pulled up to +5 volts by R107. After filtering by R108 and C77, SLAM- is fed to U11-11. Assuming that the output of the SLAM FLAG+ signal U11-9 is low, any contact bounce at the Slam Switch sets the Slam Flag by causing a "1" to be clocked to U11-9.

The 68000 resets the Slam Flag by setting U13-19 first low, then high. The SLAM FLAG+ signal is sensed by the 68000 via U27-4.

H. TEST SWITCHES (4-A6)

There are three test switches on the Operator Convenience Panel. Each is furnished with a pull-up resistor on the Audio Board. The 68000 reads these switches via U27, pins 2, 15, and 17. All three switches need not be used in all games.

PART II: THEORY OF OPERATION FOR THE Z80 SECTION OF THE Z80 AUDIO PROCESSOR BOARD

A. Z80 (1-B7)

The microprocessor used in this system is a 4 MHz Z80. All of the Z80's address, data, and control outputs are buffered by bus drivers: U70, U72, U73, and U74. These buffers are enabled when the Bus Acknowledge signal BUSAK+ is low, the normal state of BUSAK+ since jumper W11 is omitted.

B. DATA BUS DIRECTION CONTROL

A high Direction Read signal DIR RD- allows the Z80 to write into RAMs and other external devices. A low DIR RD- signal allows the transfer of data from the RAMs, ROMs, and other external devices to the Z80. The DIR RD- signal is low only under either of the following two conditions:

1. When the Z80 wishes to read data. Here, the Buffered Read signal BRD- is low at U36-9.

2. When, during interrupt-acknowledge cycles, the Z80 reads a vector address from the data bus. Here, both the BM1- and the BIORQ- signals are low at U37-1 and U37-2.

The Z80 generates sixteen address lines. After buffering, these lines are referred to as BA0+ through BA15+. BA0+ is the least significant bit. The most significant bit, BA15+, is not used.

Similarly, after buffering by data bus driver U70, the eight data bus lines are referred to as BD0+ through BD7+.

U74 buffers the following five control signals generated by the Z80:

TABLE 3-3

SIGNAL		OCCURRENCE
BM1-	BUFFERED MACHINE CYCLE 1	During instruction fetches.
BMREQ-	BUFFERED MEMORY REQUEST	When the Z80 reads or writes data from or to memory-mapped devices.

BIORQ-	BUFFERED I/O REQUEST	When the Z80 reads or writes data from or to counter timer chip U33.
BRD-	BUFFERED READ	When the Z80 reads data.
BWT-	BUFFERED WRITE	When the Z80 writes data.

U71-23, the bus acknowledge output of the Z80, is not used. The HALT- output is used to turn on the LED. The HALT- signal should normally be high. If this signal drops low, the LED illuminates, indicating a severe problem in the Z80 section of the board.

C. Z80 CONTROL LOGIC

This section describes the generation of three of the six control inputs to the Z80: Clock+, Reset-, and Wait-. The control input Bus Request (BUSRQ-) is not used. Interrupt (INT-) and Nonmaskable Interrupt (NMI-) are described in the CTC and 68000 Communication sections of this manual.

1. CLOCK CIRCUIT (3-B7)

The Clock Circuit provides the Audio Board with a stable source of timing, thus insuring, among other things, that all audio sounds remain in tune. Composed of U81, U80, Y1, and other discrete parts, the Clock Circuit consists of an oscillator and several dividers and drivers.

The oscillator is composed of U81, pins 1, 2, 8, 9, 10, and 11, Y1, R143, R144 and C133. The output of the oscillator circuit is 14.318 MHz clock at U81-2. This signal is fed into divider U80-13. Running at a fixed rate, the oscillator serves as a tuning fork for the Audio Board.

The dividers gear down the oscillator frequency by a factor of four. After first supplying 3.58 MHz to U81, pins 5 and 13, then undergoing an additional division by two, the dividers generate the clock for the GI sound chips by supplying 1.79 MHz at U80-9.

The 3.58 MHz output of divider U80-10 is used to generate SYS CLK+ and CPU CLK+. CPU CLK+ is buffered by a circuit composed of U81, pins 12 and 13, R129, R130, R133, R134, and R135. CPU CLK+ is fed to two places: to the Z80 at U71 and to the CTC at U33. Resisters 113 and 114 act as the terminator for CPU CLK+. CPU CLK+ is in phase with SYS CLK+.

The signal AUDIO CLK at U75-12 has a period of approximately 8.4 microseconds and is not used.

2. RESET CIRCUIT (3-C7)

The Reset Circuit forces the processor and other registers on the Audio Board into their proper initial states and prevents the generation of unwanted sounds. The Reset Circuit may be activated in the following two ways:

a.) Power Up:

The Power-up Reset Circuit is composed of CR4, CR5, R137-R142, C130, Q2, and U48, pins 8 and 9.

At power up, the negative side of C130 is very close to 5 volts. This causes Q2 to be turned on and the output of the circuit, U48-8, to be high. C130 now begins to charge; i.e., the voltage on its negative side goes from 5 volts down to ground. When the negative side of C130 reaches a potential of approximately .7 volts, Q2 turns off, forcing U48-8 low. To provide a clean output pulse at U48-8, R140 supplies positive feedback between U48-8 and the base of Q2. The pulse width at U48-8 is approximately 200 milliseconds.

b.) 68000 Interface:

The signal A RESET- is fed to the audio board at J3-38 and is buffered by U63, pins 4 and 16. U49 is used to "OR" together the two reset inputs. When the 68000 activates its reset line, U49-5 is forced high, U49-4 low. U49-4 is fed to Flip Flop U35 at pins 1 and 2. As long as the clear input to this Flip Flop, U35-1, is low, its output, U35-5, is low.

When the reset pulse becomes inactive, i.e., when pins 1 and 2 of U35 go high, the output of the Flip Flop, U35-5, does not go high until a positive edge is seen at U35-3. U35-5 is buffered by U75 and is fed to the CPU and the CTC. The rest of the Audio Board is reset via the system reset line SYS RESET-.

3. WAIT LOGIC (2-A1)

The Wait Logic forces the Z80 to pause under two conditions:

a.) Instruction Fetches from Memory:

Data from PROM memory is available 450 ns after the PROM has been addressed. Though fast enough for other reads of the PROM by the Z80, this speed is too slow when the Z80 is fetching instructions. Thus, U61 is used to generate a pulse which forces the Z80 to wait for the instruction words from PROM memory.

The pulse is generated in the following manner: Initially high, WM1- is fed to the Z80 via U36, pins 11 and 13. When an instruction fetch occurs, the signal BM1- goes low at U61-2. When the SYS CLK+

completes a low-to-high transition at U61, pins 3 and 11, U61-6 goes high, and U61-9 remains high. The two highs activate the signal WM1-, forcing it low.

The Wait Pulse to the processor is deactivated during the next positive transition of SYS CLK+, as U61-6 remains high and U61-9 falls low.

b.) Z80 Reads or Writes to the GI Sound Chips:

When reading or writing to GI Sound Chips U31 and U32, the Z80 must wait for two Time States, or T-States. For circuit simplicity, the signal ANY I/O-, generated by U60-6, determines when these states need to be inserted. Sometimes active for other reasons, the signal ANY I/O- is always active low whenever the GI Sound Chips are addressed.

The Wait Circuit for the GI Sound Chips is composed of U62, one half of U37, and several additional gates. Wait States during Z80 reads or writes to the GI Sound Chips are generated as follows:

The signal ANY I/O- is inverted by U49, pins 1-3. The outputs of U49 are fed to shift register U62, pins 1, 2, and 9. Low when ANY I/O- is inactive, these inputs to the shift register force all outputs of the shift register to remain low.

When a GI Sound Chip is addressed, U49-1 goes high, causing a "1" to be shifted down the outputs of the shift register. Output pins 3 and 5 of the shift register are wired to U37, pins 9 and 10. (Output pin 3 first passes through an inverter). Low for two clock cycles after the signal ANY I/O- becomes active, the output of this gate, U37-8, is fed to the Z80 via U36, pins 11 and 12.

In addition to generating a delay of two Wait States, the fourth output of the shift register shortens the Write Pulse to the GI Sound Chips. This function is implemented at U37, pins 11-13. Four clock periods after a GI sound chip is addressed, the fourth output of the shift register goes high. This signal is fed to U37-12, forcing the output, U37-11, high.

D. Z80 ADDRESS DECODING (1-C5)

Address decoding is performed by U77, U78, and U79. U79 decodes address lines 12, 13, and 14. The outputs of U79 select four different banks of Rom, two different banks of RAM, and two banks of memory-mapped I/O devices. Each of these banks is 4K long. Address decoding at U79 is enabled when Memory Request signal BMREQ- is active with a low at U79-4. It is disabled during Refresh Cycles (RFSH-) by a low at U79-6.

U77 decodes address lines 0, 5, and 6. Its outputs are used to generate Write Strobes to memory-mapped I/O devices. Also used to

decode address lines 0, 5, and 6, U78 generates Read Strobes for memory-mapped I/O devices. Address line 15 is not used.

E. PROM MEMORY (Audio Personality Schematics, 1)

Located on the Audio Personality Board, PROM Memory U1 and U2 contain the Audio program for the game. Note, however, that U2 is not always used.

F. RAM MEMORY (1-B3)

The RAM Memory stores the variables for the Audio Board. There are two blocks of RAM Memory. The first block consists of U58 and U59 on the main Z80 Audio Board and is only 1K bytes long. The chip-select for this memory block, U59-8, goes low only when the Z80 activates its Read or Write line and the signal SEL RAM 0- goes low. This function is performed at U46, pins 1-3 and U36, pins 1-3.

The second block of RAM, not used in some games, consists of U3 and U4 on the Audio Personality Board.

G. INPUT/OUTPUT

1. GI SOUND CHIPS (2-B6, 2-D6)

The GI Sound Chips, U31 and U32, generate the more complex game sounds. They are interfaced to the Z80 via U29 and U30. U30 temporarily stores data and address words being transferred from the Z80 to the Sound Chips. Whenever the Z80 writes and the signal SEL INT I/O- is low, pins 4-6 on U36 force U30-11 high, causing data from the Z80 data bus to be latched into U30.

The data retained by U30 is then placed onto the GI Sound Chips' data bus, GI D0+ through GI D7+, when U30's output enable pin, U30-1, goes low. U30-1 is controlled by the output of the D-type Flip Flop, U35-8. U35 sychronizes the output of U36-6 with the positive edges of the system clock.

U29 is used to transfer data from the GI Sound Chips back to the Z80. Its control inputs, U29-1 and U29-19, are forced low whenever either Sound Chip is being read.

Both address words and data words are written by the Z80 to the GI Sound Chips. However, only data words are read from the Sound Chips. Two control inputs on each Sound Chip control all reading and writing between the Z80 and the Sound Chips. When an address word is written into U31, the Write Address signal WGA0- falls low at U47, pins 4 and 10, forcing both control inputs, pins 18 and 20 on U31, high. In a similar fashion, the Write Data signal WGD0- at U47-5, and the Read Data signal RDG0- at U47-9 are encoded at U47 to control data

J6-55 feeds into a Volume Control Circuit consisting of one half of U8 and ten discrete parts. U8 is a multiplier. It multiplies the signal at J6-55 by the current flowing into U8-1 to produce an AC signal at U8-8. The current flowing into U8-1 is generated by passing the signal VOLUME A through R53 and R54. VOLUME A connects to the arm of the Volume Control Potentiometer on the Operator Convenience Panel via the main DC harness. The ends of the volume control are connected to ground and -15 volts. Thus, when VOLUME A is grounded, maximum current flows into U8-1, causing maximum gain to be available at U8-8. Conversely, when VOLUME A is at -15 volts, no current flows into U8-1, and no AC signal is available at U8-8. There may be, however, a small DC offset at U8-1, even at zero volume. VOLUME A enters the Audio Board at J1-M.

The output at U8-8 is amplified by U9, which also removes some of the DC offset generated by U8. U9 is wired to have a gain of approximately five for the AC component of the signal. The output at U9-6 is fed to the Audio Amplifier Board via J1-E. The Audio Amplifier Board provides power amplification to drive the speaker.

NOTE: A second, optional, Volume Control Circuit is formed by the other half of U8 and U10. Both Volume Control Circuits may be tied together or operated seperately.

I. COMMUNICATION WITH THE 68000 (4-C6)

The 68000 sends commands to the Z80 via two eight-bit registers: Command Register Low and Command Register High. The Command Register Low is composed of U56 and U57. U56 is an eight-bit latch. Data from the 68000 is strobed into U56 when a positive-going edge occurs on the clock input U56-11, and the enable input U56-1 is low. The Z80 reads the data held in this latch by placing a low on U57, pins 1 and 19.

Composed of U44 and U45, the Command Register High functions similarly to the Command Register Low. The Command Register High, however, has a COMMAND REGISTER FULL+ flag which may be read at any time by the 68000 via U27, pins 8 and 12, or by the Z80 via U28, pins 9 and 11. This flag is composed of U43, pins 8-13.

At power-up, the COMMAND REGISTER FULL+ signal at U43-8 is forced to 0 by the system's reset pulse SYS RESET-, which is fed through U26, pins 11 and 12, to U43-10. When the Command Register High is written into by the 68000, a low on U43-12 clocked into U43 by a positive transition at U43-11 sets the flag. When the Z80 reads the Command Register High, U43-8 is reset to 0 by a low-going pulse on U26-13.

U43-9, the Q output of U43, is wired to the Z80's Nonmaskable Interrupt (NMI-) input to facilitate the rapid response of the Z80 to 68000 commands. The highest priority interrupt on the Z80, NMI- can never be locked out.

J. STATUS REGISTERS (4-C5)

The Z80 sends information to the 68000 via two status registers: Status Register High and Status Register Low. As with the Command Registers, the main difference in the functions of these two registers is that the Status Register High has a STATUS REGISTER FULL+ flag which may be read by either processor.

The Status Register High, U66, is written into by the Z80 when there is a low-going pulse on clock pin U66-11. To read the information held in this latch, the 68000 activates output enable pin U66-1. The STATUS REGISTER FULL+ flag, U43-5, is set when the Z80 writes data into U66 and is cleared when the 68000 reads the data in U66. The flag is also cleared during reset.

K. POWER DISTRIBUTION (9-C6)

Power supply voltages +5, +15, and -15 enter the game electronics package through J1 on the Audio Board. A diode is placed across each supply line to ground to prevent reverse polarity conditions. All three voltages are distributed to the rest of the main Audio Board and the Audio Personality Board via J6, and to the 68000 boards via J2.

CHAPTER 4

SUPPORT ELECTRONICS

PART I: AUDIO AMPLIFIER BOARD

The Audio Amplifier Board provides power amplification to the signal input from the main Audio Board. The Amplifier Board has a differential input at P2, pins 4 and 5. The composite audio signal from the Audio board arrives at P2-4. P2-5 is wired to ground at the Audio Board.

The signal arriving at P2-4 is a composite of the desired audio signals and noise. The signal arriving at P2-5 is noise only. The signal at P2-5 is subtracted from the signal at P2-4; i.e., the noise component is subtracted from the composite noise and audio signal, leaving pure audio. This process occurs as follows:

U3, an LM324, contains four operational amplifiers. One-fourth of U3, pins 5-7, is used to provide a low-impedence biasing voltage, equaling one-half of the supply voltage, to the other amplifier circuits. The signal arriving at P2-4 is coupled by C6 and RF filtered by R4, R5, and C7. It is then buffered by U3, pins 12-14. Similar operations are carried out on the signal arriving at P2-5 by U3, pins 8-10, R2, R3, C4, and C5.

A differential amplifier, composed of U3, pins 1-3, and R9-R12, subtracts the noise component at U3-8 from the composite audio signal at U3-14 to produce a pure audio signal at U3-1.

The pure audio now available at U3-1 is amplified and sent to the speaker as follows. The Audio Power Amplifier is composed of U1, U2, and many discrete components. U1 is wired as a noninverting amplifier with a gain set by R16 and R17. An inverting amplifier, U2's gain is set by R20 and R22. U1 and U2 are wired together in a bridge configuration. Thus, for every signal excursion at U1-4, there is a signal excursion of equal magnitude but opposite direction at U2-4. The pure audio is coupled to U1-1 via R13, R14, and C11. C10 functions as an RF bypass. The input signal for U2 is obtained at the junction of R16 and R17. This signal, though very small in amplitude, is equal in phase to the signal appearing at U1-4. C16 and C24 couple the amplified audio signal to the speaker.

NOTE: Since an unregulated power supply of approximately +10 volts is fed to the Audio Amplifier Board, the power supply voltage for U3 is provided with additional filtering by R8, C9, and C3.

Note also that some games have a different power supply, one capable of supplying an unregulated 14 volts to the Amplifier Board. In these games, U2 and its associated discrete components are unnecessary and therefore not installed. Also, the speaker return is connected to P1-6 (ground) instead of P1-5.

PART II: COLOR XY MONITORS

Two different monitors may be used in the game system: the ELECTROHOME G08-105 and the WELLS-GARDNER 19K6401. These monitors are not directly interchangeable. Power requirements, harnessing and connectors, and signal levels vary between the two. The ELECTROHOME monitor requires 100 volts center-tapped AC, the WELLS-GARDNER 80 volts center-tapped AC. Use of the ELECTROHOME monitor requires the replacement of the 3.3K ohm resistors at R4, R12, and R20 on the Game Processor Board with 2.7K ohm resistors to reduce the color output signal levels. For harnessing and connector differences, refer to the system interconnection diagrams: 11-12056.

PART III: GAME HARNESSES

There are four distinct types of harnesses in the game cabinet: AC Input Harness, Flourescent Lamp Harness, Main DC Harness, and one or two Monitor Harnesses. The AC Input Harness consists of an AC line cord and connections to an interlock switch. This harness brings power to J1 of the power supply.

The Flourescent Lamp Harness takes 120 volts AC from the power supply and distributes it to all flourescent lamps in the game via J3.

The Main DC Harness distributes all of the DC power supply voltages. It also furnishes speaker connections and connects the Audio Board to the Control Panels, the Coin Door, the Operator Convenience Panel, and the Audio Amplifier.

Two different monitors used in production necessitate two different versions of monitor harnessing. All games using ELECTROHOME monitors have two Monitor Harnesses: a Monitor Power Harness and a Monitor Signal Cable. The Monitor Power Harness brings 100 volts center-tapped from J2 of the power supply to P400 of the monitor. A frame ground is also cabled in this harness. The Monitor Signal Cable feeds video signals generated at P2 of the Game Processor Board to P100 of the monitor.

All games using the WELLS-GARDNER monitor have only one Monitor Harness. Through this harness, J2 of the power supply furnishes 80 volts center- tapped AC filament voltage and a frame ground to P100 of

the monitor. The harness also feeds to P100 the Red, Green, and Blue signals generated at P2 of the Game Processor Board. And lastly, the harness feeds the X and Y deflection signals generated by the Game Processor Board to P200 of the monitor.

NOTE: Since there is no grounding strap in the game, all frame grounds are connected within the various harnesses.

Also, two ribbon cables are used. One 34-pin ribbon cable routes power from J2 of the Audio Board to P1 of the Game Processor Board, and one 40-pin passes communication signals between P3 of the Game Processor Board and J3 of the Audio Board.

PART IV: POWER SUPPLY

The Power Supply Plate Assembly is composed of five modules:

1. Audio Amplifier Board
2. Unregulated DC Power Supply
3. +15 and -15 Regulator Board
4. 5 volts DC Power Supply
5. Monitor Power Transformer(s)

Line voltage is routed from J1 of the Power Supply Plate to the Unregulated DC Supply, to the Regulated DC supply, and to the Monitor Transformers. Each of these assemblies has its own line fuse.

The Monitor Transformer(s) supply 100 volts center-tapped to the monitor through J2 of the Power Supply Plate Assembly. The outputs of the 5 volt DC Power Supply and the +15 and -15 Regulator Board are routed directly to the Audio Board via J4 of the Power Supply Plate Assembly. The Unregulated Power Supply provides unregulated +25 and -25 volts DC to the +15 and -15 Regulator Board, and generates +10 volts DC for the Audio Amplifier Board.

The Audio Amplifier Board receives its input from the Audio Board through the main wiring harness and J4 of the Power Supply Plate Assembly. The output of the Audio Amplifier is routed through J4 and the main wiring harness to the speaker.

The flourescent lamp frame ground is obtained via a SPADE LUG connectd to the frame ground terminal block. 110 volts AC are fed to the flourescent lamps through J2 of the 5 volt DC Power Supply. Note that this connection is referred to as J3 of the Power Supply Plate Assembly.

APPENDIX B

SCHEMATICS AND INTERCONNECT DIAGRAMS

TABLE OF CONTENTS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

CONTROL PANEL

SIGNAL LIST
- 8 SWITCH INPUT
- 4 SWITCH, TRACKBALL OR SHAFT ENCODER INPUT
- 2 SWITCH INPUT OR +5V OUTPUT
- 2 SWITCH INPUT OR LED OUTPUT
- 1 RETURN

03-06-2241
03-06-1242 J1 H2 24 PIN

COIN DOOR

SIGNAL LIST
- 1 COIN #
- 1 COIN 1
- 1 5V DC LIGHTS
- 1 RETURN

03-06-2092
03-06-1092 J1 H5 9 PIN

OPERATOR CONVENIENCE PANEL

SIGNAL LIST
- 1 -15V
- 1 VOLUME
- 1 VOLUME RETURN
- 1 TEST SWITCH
- 1 TEST SWITCH RETURN
- 1 COIN COUNTER
- 1 COIN COUNTER RTURN

03-06-2122
03-06-1122 J1 H5 12 PIN

+5VDC ± 4% & ±15VDC

MOUNTING PLATE

DC PWR

09-30-5111 H2 P2 11 PIN

P1 P3

J1 H1 72 PIN

J2 34 PIN

J3 40 PIN

Z80 AUDIO BOARD

J5 P1 GANG PERS. MODULE

J6 P1 AUDIO PERSONL. MODULE

GANG PROC. BOARD

J4 30 PIN

J5 40 PIN

SPEAKER

J4 H6 36 PIN
03-06-2368
03-06-1368

03-06-1092

INTERLOCK SWITCH

POWER SUPPLY
DWG. NO: 11-12110-01

J1 H7

J5 H8 4 PIN

9 PIN

J2 H9 15 PIN

TO FLORESCENT LIGHTS

MONITOR, COLOR X-Y
ELECTROHOME P/N G08105

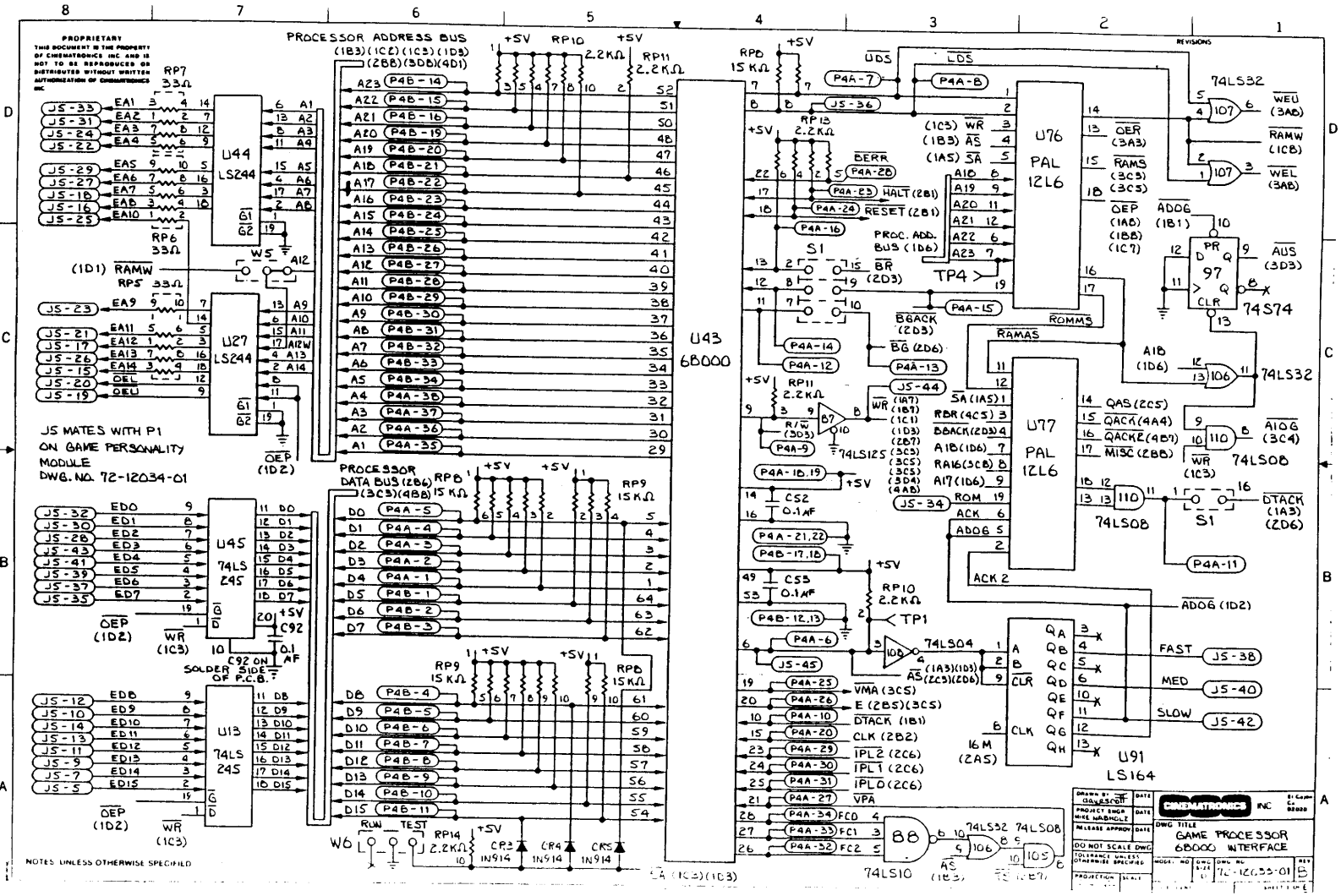
INPUTS
- 1 RED
- 1 BLUE
- 1 GREEN
- 2 X W/RETURN
- 2 Y W/RETURN
- 3 100 VAC C.T.

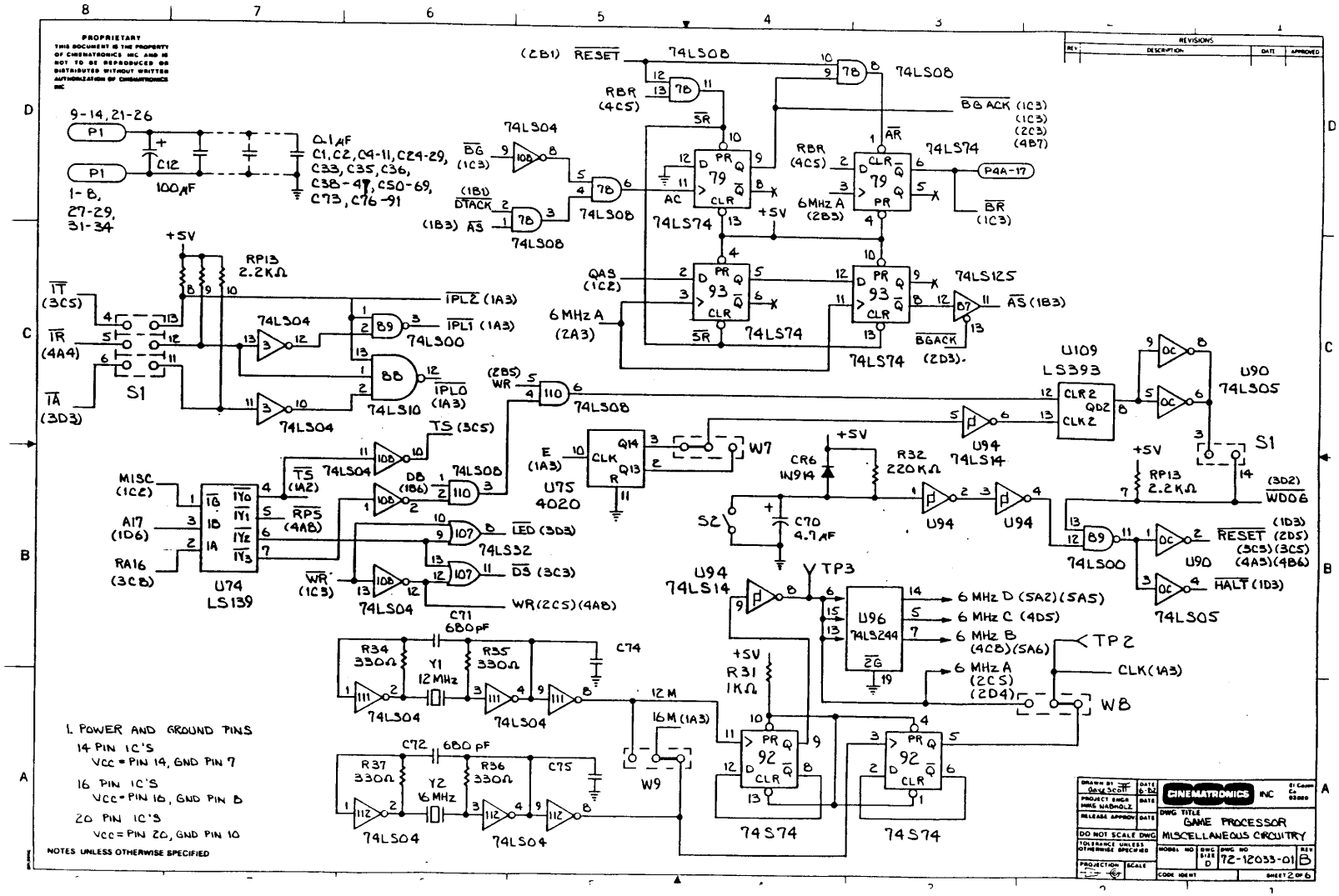
P100 H11 6 PIN
7 R,G,B,X,Y

P104 H10 3 PIN
100 VAC C.T.

NOTES UNLESS OTHERWISE SPECIFIED

MATERIAL	DRAWN BY P. RAMIREZ	DATE 8/3/82	CINEMATRONICS INC
FINISH	PROJECT ENGR	DATE	DWG TITLE INTERCONNECT DIAGRAM 68000 SYSTEM (ELEC)
	RELEASE APPROV	DATE 8/6	
	DO NOT SCALE DWG		MODEL NO
	TOLERANCE UNLESS OTHERWISE SPECIFIED		DWG SIZE D
	PROJECTION	SCALE NONE	DWG NO 11-12056-01 REV A
			CODE IDENT
			SHEET 1 OF 1


PROPRIETARY
THIS DOCUMENT IS THE PROPERTY OF CINEMATRONICS INC AND IS NOT TO BE REPRODUCED OR DISTRIBUTED WITHOUT WRITTEN AUTHORIZATION OF CINEMATRONICS INC
PROCESSOR ADDRESS BUS
(1B3)(1C2)(1C3)(1D3)
(2B3)(3D3)(4D1)
U43
68000
U44
LS244
U27
LS244
U45
74LS 245
U13
74LS 245
U76
PAL
12L6
U77
PAL
12L6
U91
LS164
JS MATES WITH P1
ON GAME PERSONALITY
MODULE
DWG. NO. 72-12034-01
SOLDER SIDE OF P.C.B.
NOTES UNLESS OTHERWISE SPECIFIED
REVISIONS
GAME PROCESSOR
68000 INTERFACE
CINEMATRONICS INC
72-12035-01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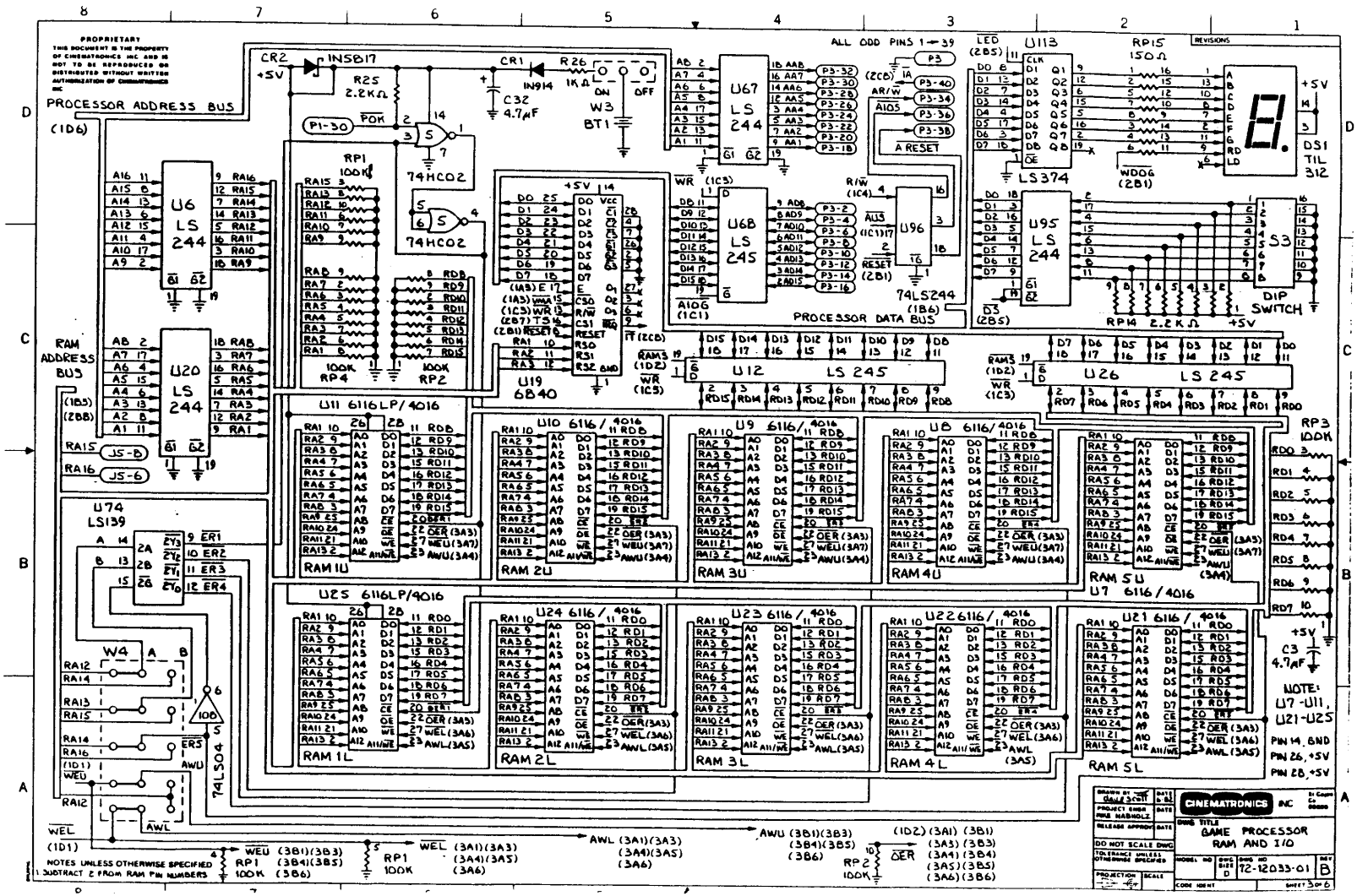
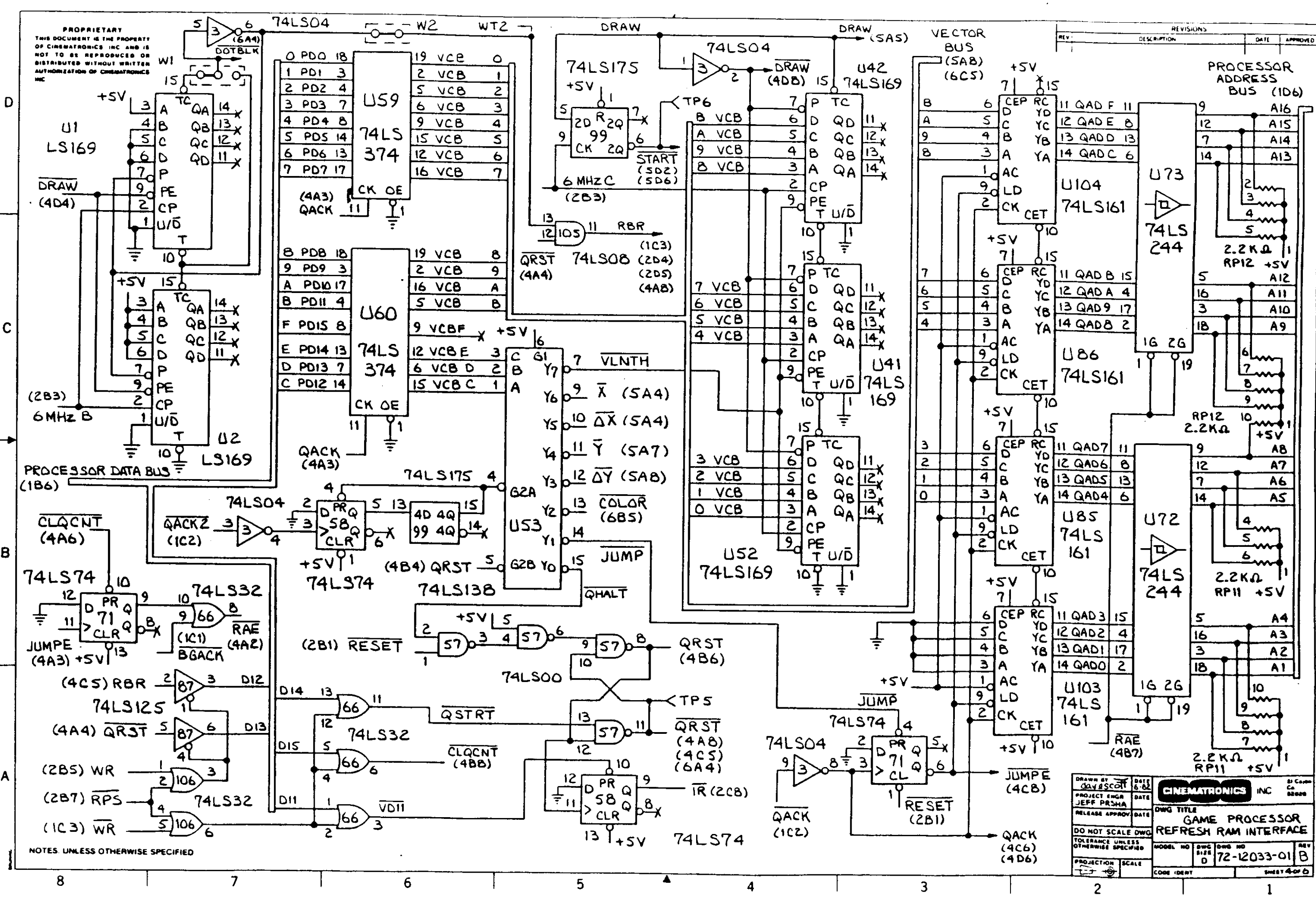
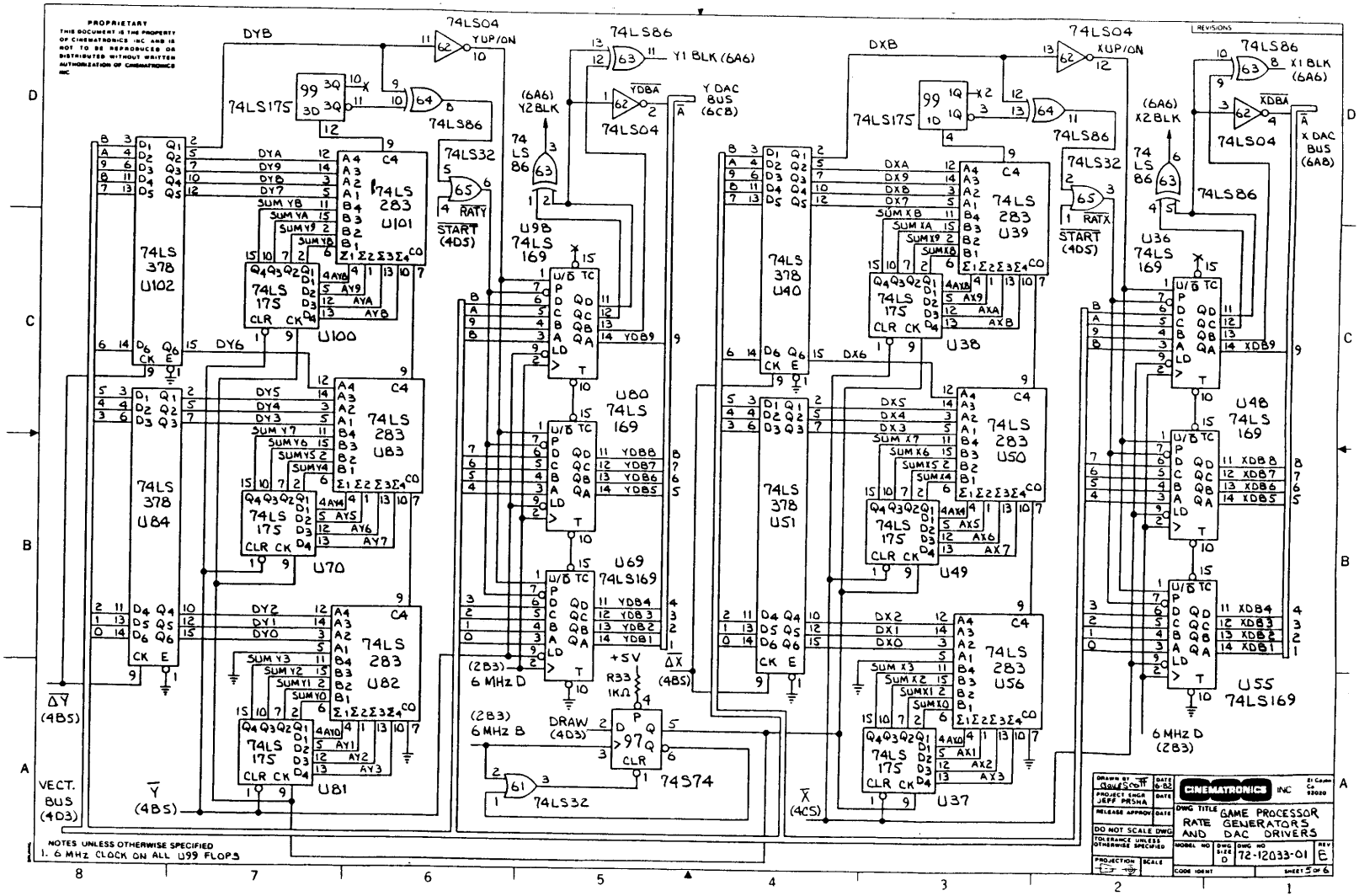
REVISIONS
REV. DESCRIPTION DATE APPROVED
9-14, 21-26
1-8, 27-29, 31-34
P1
C12 100µF
C1, C2, C9-11, C24-29, C33, C35, C36, C38-49, C50-69, C73, C76-91 0.1µF
+5V
RP13 2.2KΩ
S1
IT (3C5)
IR (4A4)
IA (3D3)
74LS04
74LS00
74LS10
IPL2 (1A3)
IPL1 (1A3)
IPL0 (1A3)
TS (3C5)
TS (1A2)
MISC (1C2)
A17 (1D6)
RA16 (3C8)
U74 LS139
RPS (4A8)
DB (1B6)
74LS08
74LS32
LED (3D3)
DS (3C3)
WR (1C3)
WR (2C5)(4A8)
(2B1) RESET
RBR (4C5)
SR
BG (1C3)
DTACK (1B1)
AS (1B3)
74LS74
BG ACK (1C3) (1C3) (2C3) (4B7)
AR
6MHz A (2B3)
P4A-17
BR (1C3)
QA3 (1C2)
74LS125
6MHz A (2A3)
BGACK (2D3)
AS (1B3)
(2B5) WR
U109 LS393
U90 74LS05
U94 74LS14
U75 4020
E (1A3)
Q14
Q13
W7
CR6 IN914
R32 220KΩ
C70 4.7µF
S2
WDOG
(3D2)
RESET (2D5) (3C5) (3C5) (4A5) (4B6)
HALT (1D3)
TP3
U96 74LS244
6 MHz D (5A2) (5A5)
6 MHz C (4D5)
6 MHz B (4C8) (5A6)
6 MHz A (2C5) (2D4)
TP2
CLK (1A3)
W8
C71 680pF
C74
R34 330Ω
R35 330Ω
Y1 12MHz
12M
16M (1A3)
R31 1KΩ
C72 680 pF
C75
R37 330Ω
R36 330Ω
Y2 16MHz
W9
74S74
1. POWER AND GROUND PINS
14 PIN IC'S
VCC = PIN 14, GND PIN 7
16 PIN IC'S
VCC = PIN 16, GND PIN 8
20 PIN IC'S
VCC = PIN 20, GND PIN 10
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE GAME PROCESSOR MISCELLANEOUS CIRCUITRY
DWG NO 72-12033-01
REV B
SHEET 2 OF 6


PROPRIETARY
PROCESSOR ADDRESS BUS
RAM ADDRESS BUS
PROCESSOR DATA BUS
U6 LS 244
U20 LS 244
U67 LS 244
U68 LS 245
U95 LS 244
U96
74LS244
U19 6840
U12 LS 245
U26 LS 245
74HC02
74HC02
74LS374
DIP SWITCH
U74 LS139
74LS04
U11 6116LP/4016
U10 6116/4016
U9 6116/4016
U8 6116/4016
U7 6116/4016
U25 6116LP/4016
U24 6116/4016
U23 6116/4016
U22 6116/4016
U21 6116/4016
RAM 1U
RAM 2U
RAM 3U
RAM 4U
RAM 5U
RAM 1L
RAM 2L
RAM 3L
RAM 4L
RAM 5L
GAME PROCESSOR RAM AND I/O
CINEMATRONICS INC
72-12033-01
NOTES UNLESS OTHERWISE SPECIFIED
1. SUBTRACT 2 FROM RAM PIN NUMBERS


PROPRIETARY
THIS DOCUMENT IS THE PROPERTY OF CINEMATRONICS INC AND IS NOT TO BE REPRODUCED OR DISTRIBUTED WITHOUT WRITTEN AUTHORIZATION OF CINEMATRONICS INC
U1 LS169
U2 LS169
U59 74LS374
U60 74LS374
U53 74LS138
U42 74LS169
U41 74LS169
U52 74LS169
U104 74LS161
U86 74LS161
U85 74LS161
U103 74LS161
U73 74LS244
U72 74LS244
PROCESSOR DATA BUS (1B6)
PROCESSOR ADDRESS BUS (1D6)
VECTOR BUS (SAB) (6C5)
DRAW (SAS)
6 MHz B (2B3)
6 MHz C (2B3)
START (SD2) (SD6)
RBR (1C3) (2D4) (2D5) (4A8)
VLNTH
X̄ (SA4)
ΔX̄ (SA4)
Ȳ (SA7)
ΔȲ (SA8)
COLOR (6B5)
JUMP
QHALT
QRST (4B6)
QRST (4A8) (4C5) (6A4)
IR (2C8)
QSTRT
CLQCNT (4B8)
VD11
RAE (4A2)
BGACK (1C1)
JUMPE (4C8)
QACK (4C6) (4D6)
RESET (2B1)
RAE (4B7)
2.2KΩ RP12 +5V
2.2KΩ RP11 +5V
NOTES: UNLESS OTHERWISE SPECIFIED
DRAWN BY dave scott 6-82
PROJECT ENGR JEFF PRSHA
CINEMATRONICS INC
DWG TITLE GAME PROCESSOR REFRESH RAM INTERFACE
DWG NO 72-12033-01
REV B
SHEET 4 of 6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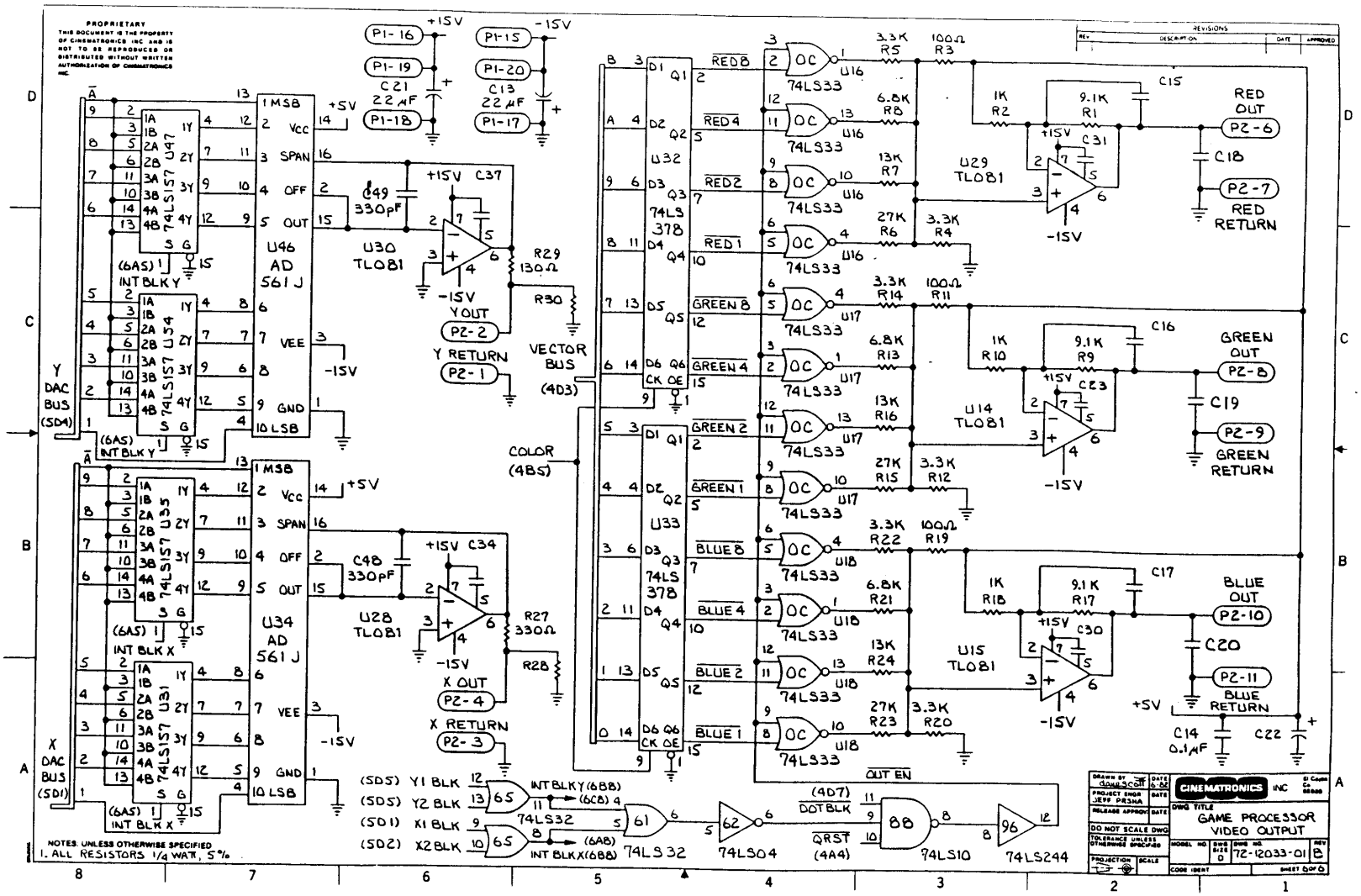
REVISIONS
74LS04
74LS86
74LS32
74LS175
74LS283
74LS378
74LS175
74LS169
74LS74
DYB
YUP/ON
Y1 BLK (6A6)
Y DAC BUS (6C8)
(6A6) Y2BLK
YDBA
DXB
XUP/ON
X1 BLK (6A6)
(6A6) X2BLK
XDBA
X DAC BUS (6A8)
START (4D5)
RATY
RATX
U101
U102
U100
U84
U83
U70
U82
U81
U80
U69
U39
U38
U40
U51
U50
U49
U56
U37
U36
U48
U55
6 MHz D (2B3)
6 MHz B (2B3)
DRAW (4D3)
+5V
R33 1KΩ
VECT. BUS (4D3)
NOTES UNLESS OTHERWISE SPECIFIED
1. 6 MHz CLOCK ON ALL U99 FLOPS
CINEMATRONICS INC
DWG TITLE GAME PROCESSOR RATE GENERATORS AND DAC DRIVERS
MODEL NO
DWG NO 72-12033-01
REV E
SHEET 5 OF 6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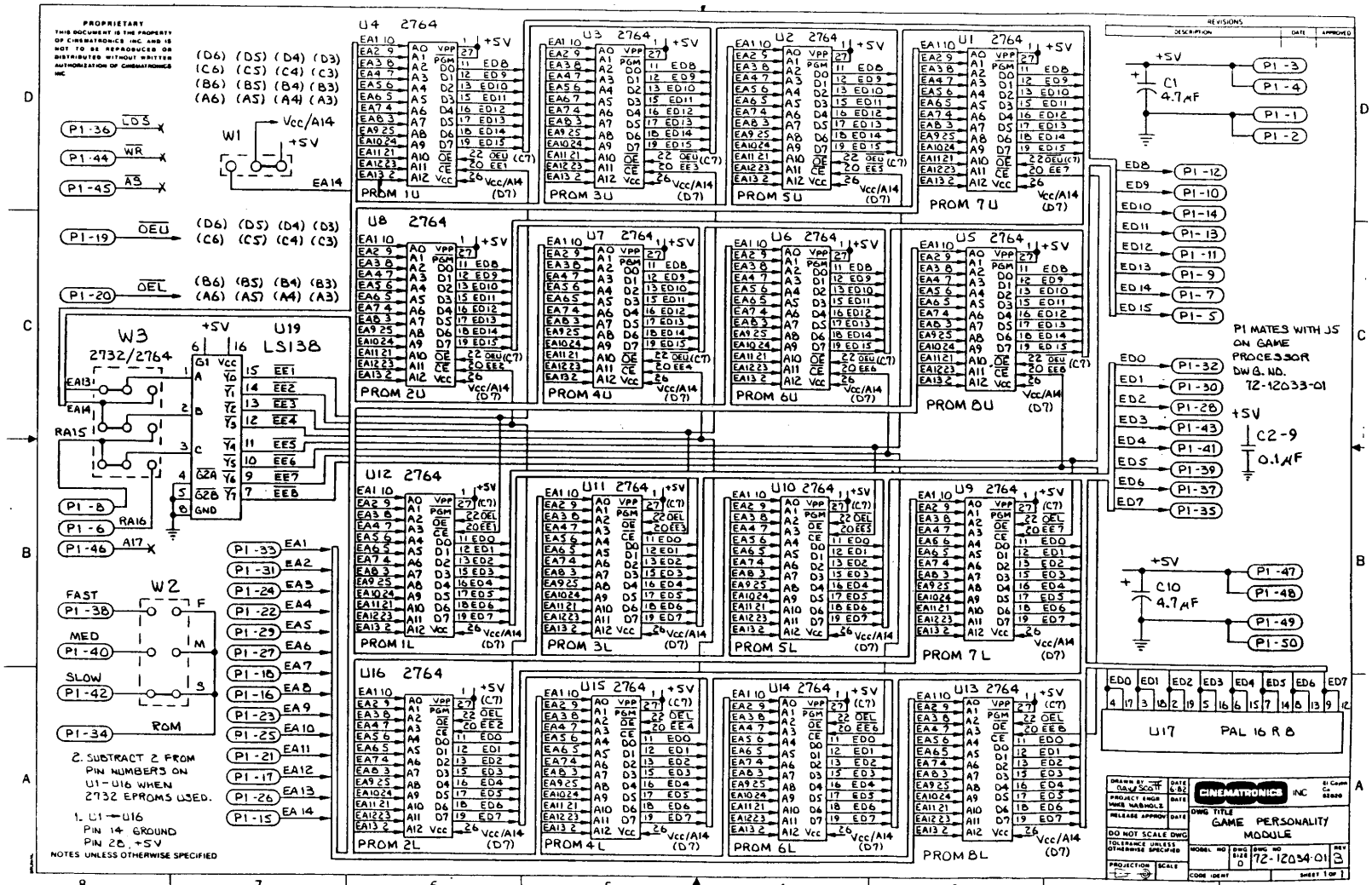
REVISIONS
REV DESCRIPTION DATE APPROVED
P1-16 +15V
P1-19
C21 22 µF
P1-18
P1-15 -15V
P1-20
C13 22 µF
P1-17
Y DAC BUS (SD4)
X DAC BUS (SD1)
74LS157 U47
74LS157 U34
74LS157 U35
74LS157 U31
1 MSB
2 VCC
3 SPAN
4 OFF
5 OUT
6
7 VEE
8
9 GND
10 LSB
+5V
-15V
(6A5) INT BLK Y
(6A5) INT BLK X
U46 AD 561 J
U45 AD 561 J
C49 330pF
C48 330pF
U30 TL081
U28 TL081
+15V C37
+15V C34
R29 130Ω
R27 330Ω
R30
R28
Y OUT
PZ-2
Y RETURN
PZ-1
X OUT
PZ-4
X RETURN
PZ-3
VECTOR BUS (4D3)
COLOR (4B5)
U32 74LS378
U33 74LS378
RED8
RED4
RED2
RED1
GREEN8
GREEN4
GREEN2
GREEN1
BLUE8
BLUE4
BLUE2
BLUE1
74LS33
U16
U17
U18
3.3K R5
100Ω R3
6.8K R8
13K R7
27K R6
3.3K R4
3.3K R14
100Ω R11
6.8K R13
13K R16
27K R15
3.3K R12
3.3K R22
100Ω R19
6.8K R21
13K R24
27K R23
3.3K R20
1K R2
9.1K R1
1K R10
9.1K R9
1K R18
9.1K R17
U29 TL081
U14 TL081
U15 TL081
C15
C16
C17
C18
C19
C20
C31
C23
C30
RED OUT
PZ-6
PZ-7
RED RETURN
GREEN OUT
PZ-8
PZ-9
GREEN RETURN
BLUE OUT
PZ-10
PZ-11
BLUE RETURN
C14 0.1µF
C22
OUT EN
(4D7) DOTBLK
QRST (4A4)
(5D5) Y1 BLK
(5D5) Y2 BLK
(5D1) X1 BLK
(5D2) X2 BLK
INT BLK Y (6B8)
INT BLK X (6B8)
74LS32
74LS04
74LS10
74LS244
NOTES. UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/4 WATT, 5%
CINEMATRONICS INC
DWG TITLE GAME PROCESSOR VIDEO OUTPUT
DWG NO 72-12033-01
REV B
SHEET 5 OF 6


PROPRIETARY
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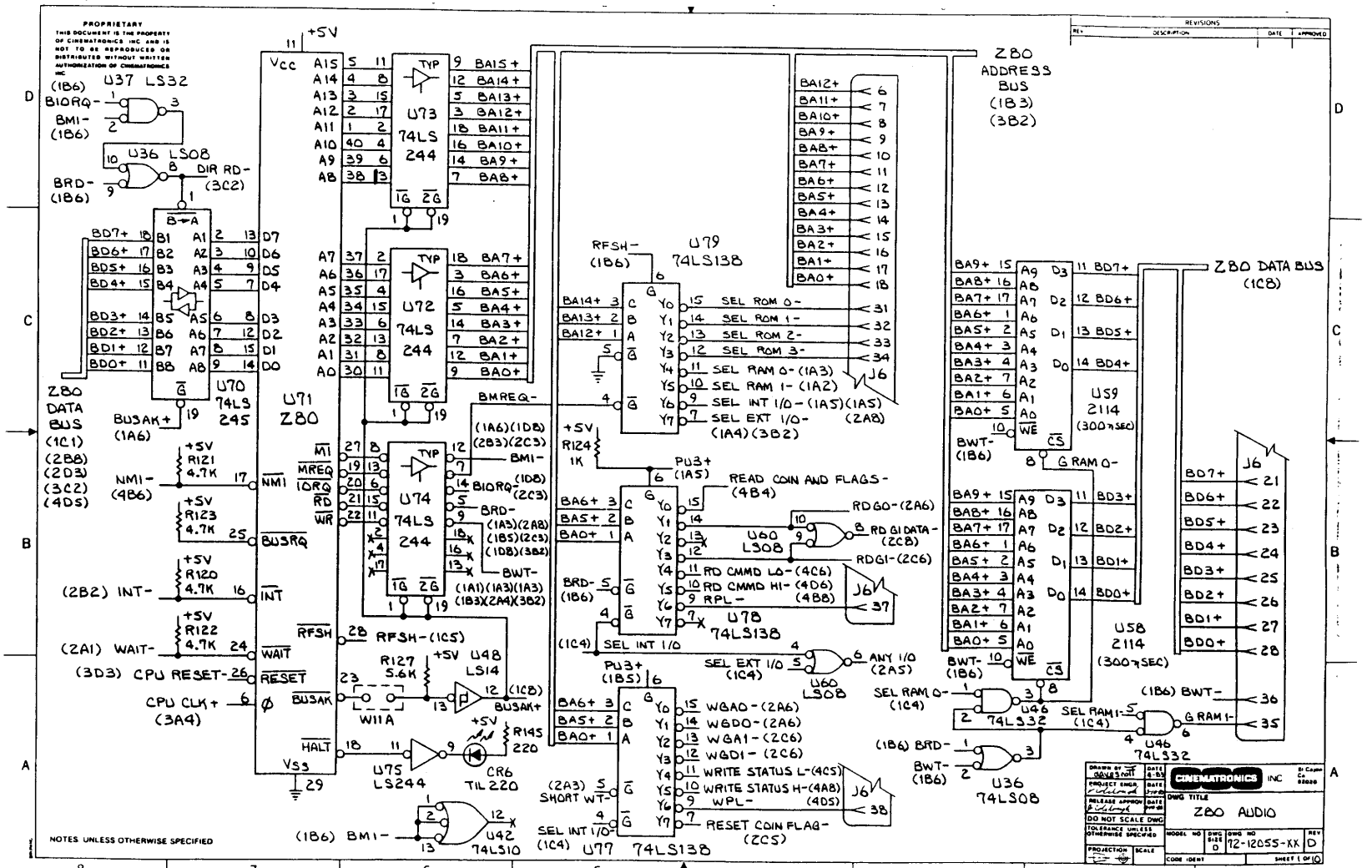
U4 2764
U3 2764
U2 2764
U1 2764
U8 2764
U7 2764
U6 2764
U5 2764
U12 2764
U11 2764
U10 2764
U9 2764
U16 2764
U15 2764
U14 2764
U13 2764
PROM 1U
PROM 3U
PROM 5U
PROM 7U
PROM 2U
PROM 4U
PROM 6U
PROM 8U
PROM 1L
PROM 3L
PROM 5L
PROM 7L
PROM 2L
PROM 4L
PROM 6L
PROM 8L
+5V
Vcc/A14
(D7)
W1
W2
W3
2732/2764
U19 LS138
U17 PAL 16 R 8
C1 4.7µF
C10 4.7µF
C2-9 0.1µF
P1 MATES WITH J5 ON GAME PROCESSOR DWG. NO. 72-12033-01
2. SUBTRACT 2 FROM PIN NUMBERS ON U1-U16 WHEN 2732 EPROMS USED.
1. U1→U16 PIN 14 GROUND PIN 28 +5V
NOTES UNLESS OTHERWISE SPECIFIED
REVISIONS
DESCRIPTION
DATE
APPROVED
CINEMATRONICS INC
DWG TITLE
GAME PERSONALITY MODULE
DWG NO 72-12034-01
REV 3
SHEET 1 OF 1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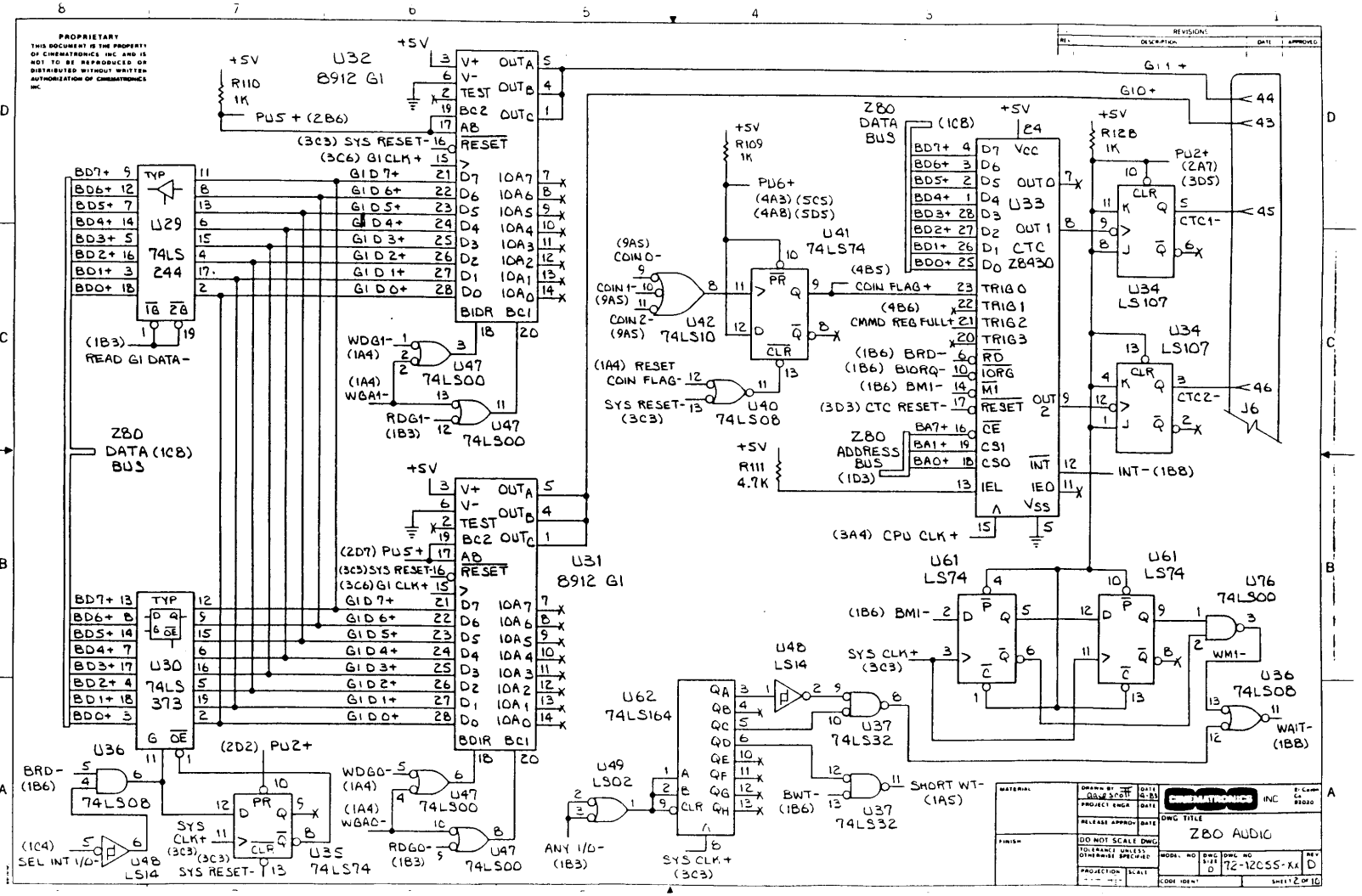
REVISIONS
REV | DESCRIPTION | DATE | APPROVED
U37 LS32
(1B6) BIORQ-
BMI- (1B6)
U36 LS08
BRD- (1B6)
DIR RD- (3C2)
B→A
U70 74LS 245
Z80 DATA BUS (1C1) (2B8) (2D3) (3C2) (4D5)
BUSAK+ (1A6)
U71 Z80
+5V
R121 4.7K
R123 4.7K
R120 4.7K
R122 4.7K
R127 5.6K
W11A
R145 220
CR6 TIL220
U75 LS244
U73 74LS 244
U72 74LS 244
U74 74LS 244
U48 LS14
U42 74LS10
U79 74LS138
U78 74LS138
U77 74LS138
U60 LS08
U59 2114 (300nSEC)
U58 2114 (300nSEC)
U46 74LS32
U36 74LS08
Z80 ADDRESS BUS (1B3) (3B2)
Z80 DATA BUS (1C8)
RFSH- (1B6)
BMREQ-
BMI-
BIORQ-
BRD-
BWT-
RFSH-(1C5)
READ COIN AND FLAGS- (4B4)
RDG0-(2A6)
RD G1 DATA- (2C8)
RDG1-(2C6)
RD CMMD LO-(4C6)
RD CMMD HI- (4D6)
RPL- (4B8)
SEL INT I/O
SEL EXT I/O (1C4)
ANY I/O (2A5)
WGA0-(2A6)
WGD0-(2A6)
WGA1-(2C6)
WGD1-(2C6)
WRITE STATUS L-(4C5)
WRITE STATUS H-(4A8)
WPL- (4D5)
RESET COIN FLAG- (2C5)
SEL ROM 0-
SEL ROM 1-
SEL ROM 2-
SEL ROM 3-
SEL RAM 0- (1A3)
SEL RAM 1- (1A2)
SEL INT I/O- (1A5)(1A5)
SEL EXT I/O- (1A4)(3B2) (2A8)
G RAM 0-
G RAM 1-
SEL RAM 0- (1C4)
SEL RAM 1- (1C4)
(1B6) BWT-
(1B6) BRD-
(1B6) BWT-
(2B2) INT-
(2A1) WAIT-
(3D3) CPU RESET-
CPU CLK+ (3A4)
(1B6) BMI-
SHORT WT- (2A3)
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
DWG NO 72-12055-KK
REV D
SHEET 1 OF 10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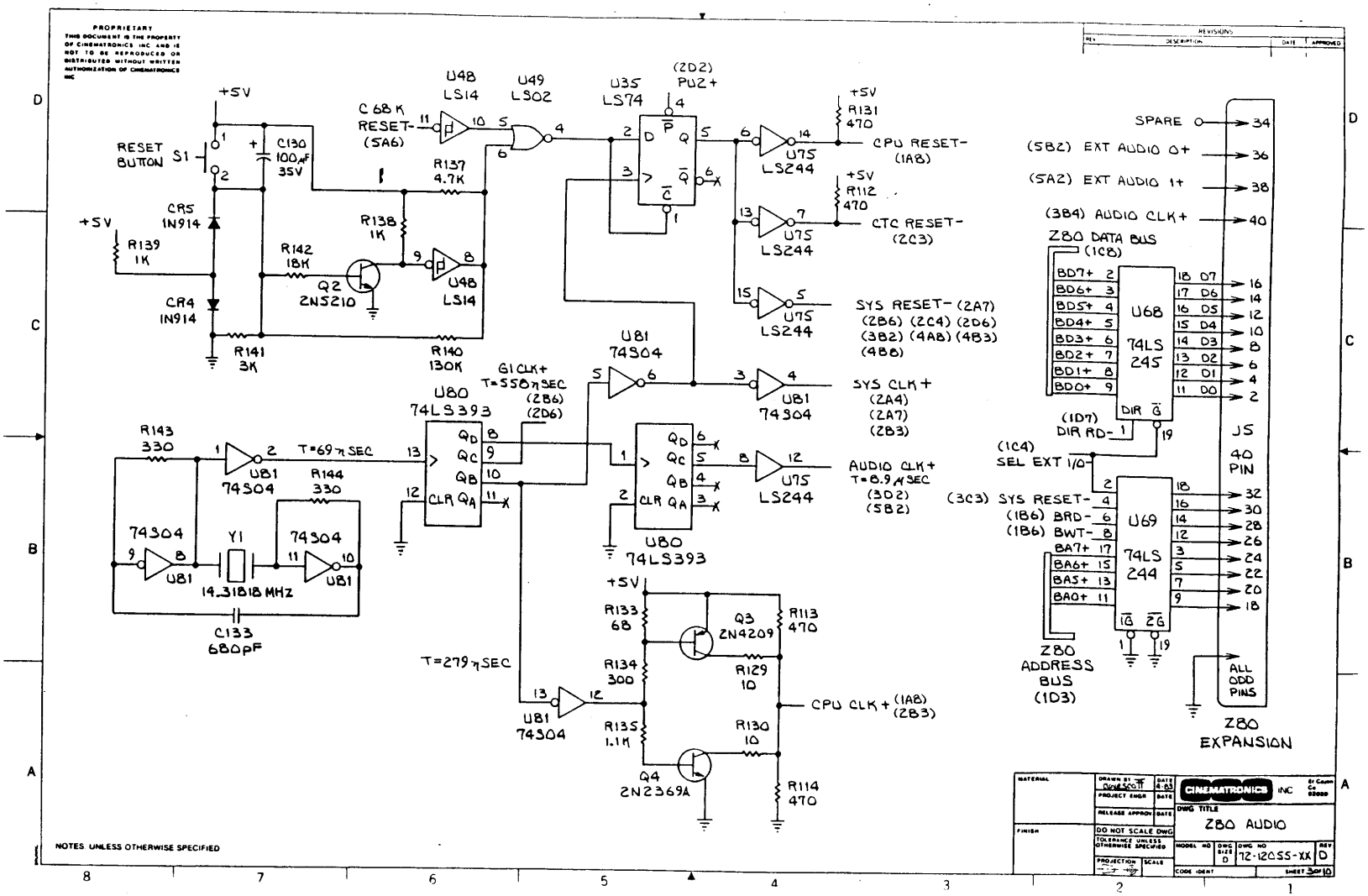
REVISIONS
DESCRIPTION
DATE
APPROVED
U32
8912 G1
U31
8912 G1
+5V
R110
1K
PU5+ (2B6)
(3C3) SYS RESET-
(3C6) G1 CLK+
G1 D7+
G1 D6+
G1 D5+
G1 D4+
G1 D3+
G1 D2+
G1 D1+
G1 D0+
BIDIR
BC1
U29
74LS
244
U30
74LS
373
(1B3) READ G1 DATA-
Z80 DATA (1C8) BUS
WDG1- (1A4)
WGA1- (1A4)
RDG1- (1B3)
U47
74LS00
(2D7) PU5+
WDG0- (1A4)
WGA0- (1A4)
RDG0- (1B3)
U36
74LS08
BRD- (1B6)
(2D2) PU2+
SYS CLK+ (3C3)
SYS RESET- (3C3)
U35
74LS74
(1C4) SEL INT I/O-
U48
LS14
ANY I/O- (1B3)
U49
LS02
U62
74LS164
SYS CLK+ (3C3)
U48
LS14
U37
74LS32
BWT- (1B6)
SHORT WT- (1A5)
R109
1K
PU6+ (4A3) (5C5) (4A8) (5D5)
U41
74LS74
U42
74LS10
(9A5) COIN0-
COIN1- (9A5)
COIN2- (9A5)
(1A4) RESET COIN FLAG-
SYS RESET- (3C3)
U40
74LS08
Z80 DATA BUS (1C8)
U33
Z80 CTC
Z8430
(4B5) COIN FLAG+
(4B6) CMMD REG FULL+
(1B6) BRD-
(1B6) BIORQ-
(1B6) BMI-
(3D3) CTC RESET-
Z80 ADDRESS BUS (1D3)
BA7+
BA1+
BA0+
R111
4.7K
(3A4) CPU CLK+
INT-(1B8)
R128
1K
PU2+ (2A7) (3D5)
U34
LS107
CTC1-
CTC2-
J6
U61
LS74
(1B6) BMI-
SYS CLK+ (3C3)
U76
74LS00
WM1-
U36
74LS08
WAIT- (1B8)
G11+
G10+
MATERIAL
FINISH
DRAWN BY
PROJECT ENGR
RELEASE APPROV
DO NOT SCALE DWG
TOLERANCE UNLESS OTHERWISE SPECIFIED
PROJECTION
SCALE
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
MODEL NO
DWG SIZE D
DWG NO 72-12055-XX
REV D
CODE IDENT
SHEET 2 OF 10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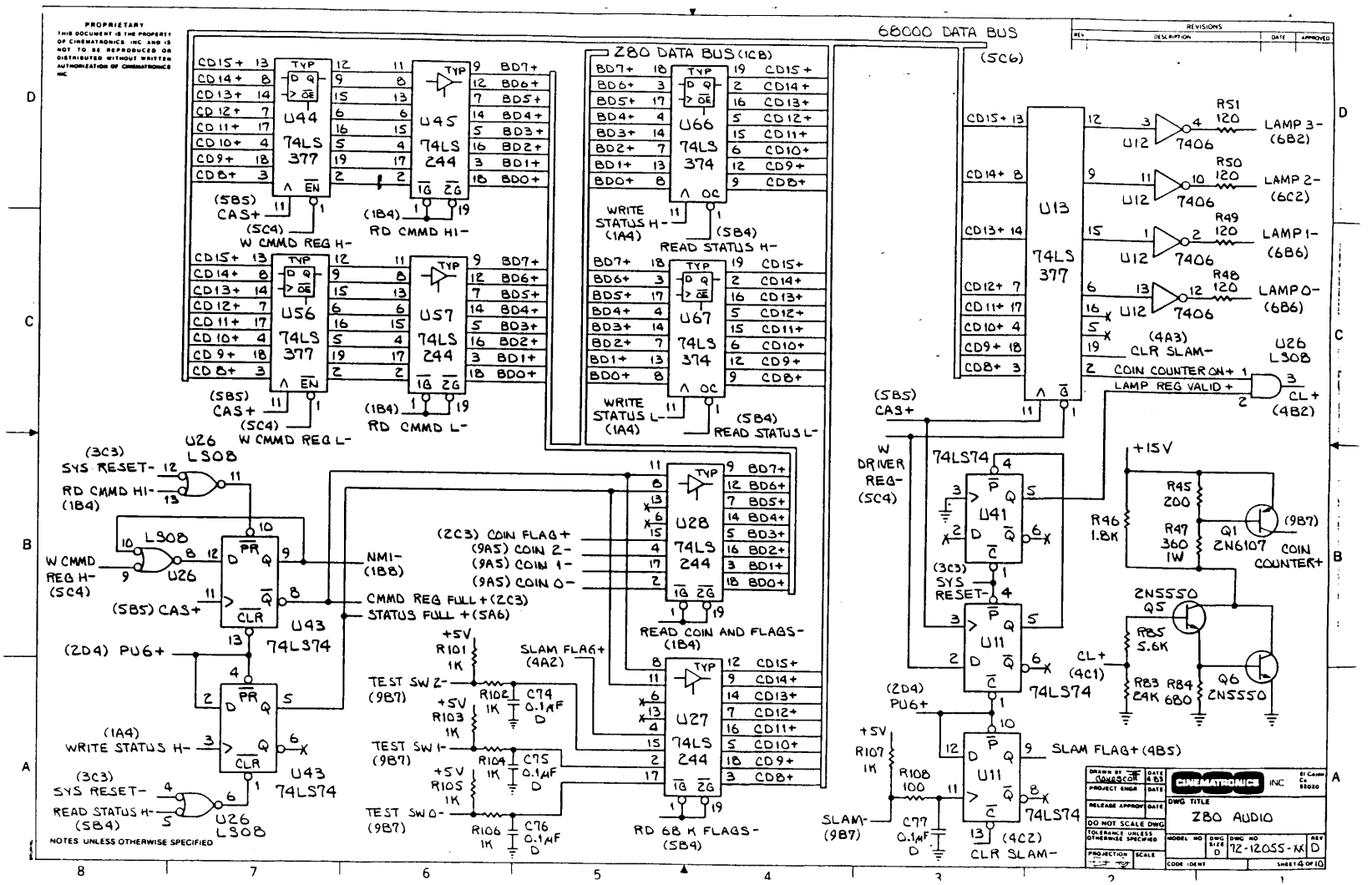
REVISIONS
REV DESCRIPTION DATE APPROVED
+5V
RESET BUTTON S1
C130 100µF 35V
CR5 1N914
CR4 1N914
R139 1K
R141 3K
R142 18K
R138 1K
R137 4.7K
R140 130K
Q2 2N5210
U48 LS14
C 68 K RESET- (5A6)
U49 LS02
U35 LS74
(2D2) PU2+
R131 470
R112 470
U75 LS244
CPU RESET- (1A8)
CTC RESET- (2C3)
SYS RESET- (2A7) (2B6) (2C4) (2D6) (3B2) (4A8) (4B3) (4B6)
U81 74S04
G1 CLK+ T=550nSEC (2B6) (2D6)
SYS CLK+ (2A4) (2A7) (2B3)
U80 74LS393
R143 330
R144 330
T=69nSEC
Y1 14.31818 MHz
C133 680pF
AUDIO CLK+ T=8.9µSEC (3D2) (5B2)
T=279nSEC
R133 68
R134 300
R135 1.1K
Q3 2N4209
Q4 2N2369A
R113 470
R129 10
R130 10
R114 470
CPU CLK+ (1A8) (2B3)
SPARE 0
(5B2) EXT AUDIO 0+
(5A2) EXT AUDIO 1+
(3B4) AUDIO CLK+
Z80 DATA BUS (1C8)
U68 74LS 245
DIR RD- (1D7)
SEL EXT I/O (1C4)
U69 74LS 244
(3C3) SYS RESET-
(1B6) BRD-
(1B6) BWT-
Z80 ADDRESS BUS (1D3)
ALL ODD PINS
J5 40 PIN
Z80 EXPANSION
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
DWG NO 12-12055-XX
REV D
SHEET 3 OF 10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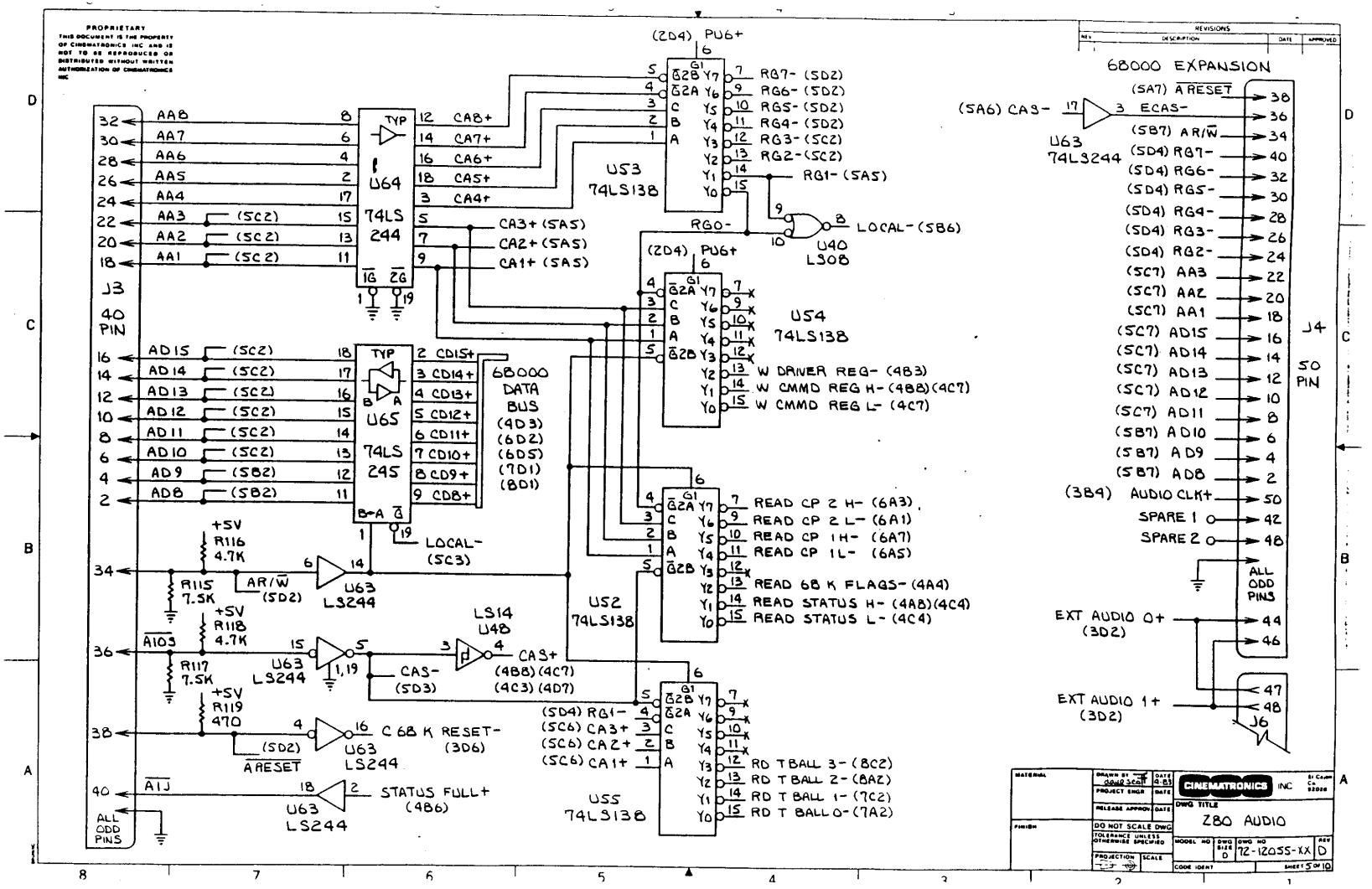
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
68000 DATA BUS
(5C6)
Z80 DATA BUS (1C8)
U44 74LS 377
U45 74LS 244
U46 74LS 377
U47 74LS 244
U66 74LS 374
U67 74LS 374
U13 74LS 377
U28 74LS 244
U27 74LS 244
U41 74LS74
U11 74LS74
U43 74LS74
U26 LS08
U12 7406
(SBS) CAS+
(SC4) W CMMD REG H-
(SC4) W CMMD REG L-
(1B4) RD CMMD H1-
(1B4) RD CMMD L-
WRITE STATUS H- (1A4)
WRITE STATUS L- (1A4)
(SB4) READ STATUS H-
(SB4) READ STATUS L-
(3C3) SYS RESET-
RD CMMD H1- (1B4)
W CMMD REG H- (5C4)
(SBS) CAS+
(2D4) PU6+
(1A4) WRITE STATUS H-
READ STATUS H- (SB4)
NMI- (1B8)
CMMD REG FULL + (2C3)
STATUS FULL + (SA6)
(2C3) COIN FLAG+
(9A5) COIN 2-
(9A5) COIN 1-
(9A5) COIN 0-
READ COIN AND FLAGS- (1B4)
RD 68 K FLAGS- (SB4)
+5V
R101 1K
R102 1K
R103 1K
R104 1K
R105 1K
R106 1K
C74 0.1μF
C75 0.1μF
C76 0.1μF
TEST SW 2- (9B7)
TEST SW 1- (9B7)
TEST SW 0- (9B7)
SLAM FLAG+ (4A2)
SLAM FLAG+ (4B5)
SLAM- (9B7)
R107 1K
R108 100
C77 0.1μF
(4C2) CLR SLAM-
W DRIVER REG- (5C4)
CL+ (4C1)
R46 1.8K
R45 200
R47 360 1W
Q1 2N6107
(9B7) COIN COUNTER+
R85 5.6K
R83 24K
R84 680
Q5 2N5550
Q6 2N5550
RS1 120 LAMP 3- (6B2)
RS0 120 LAMP 2- (6C2)
R49 120 LAMP 1- (6B6)
R48 120 LAMP 0- (6B6)
(4A3) CLR SLAM-
COIN COUNTER 0+
LAMP REG VALID +
CL+ (4B2)
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
DWG NO 12-12055-XX
REV D
SHEET 4 OF 10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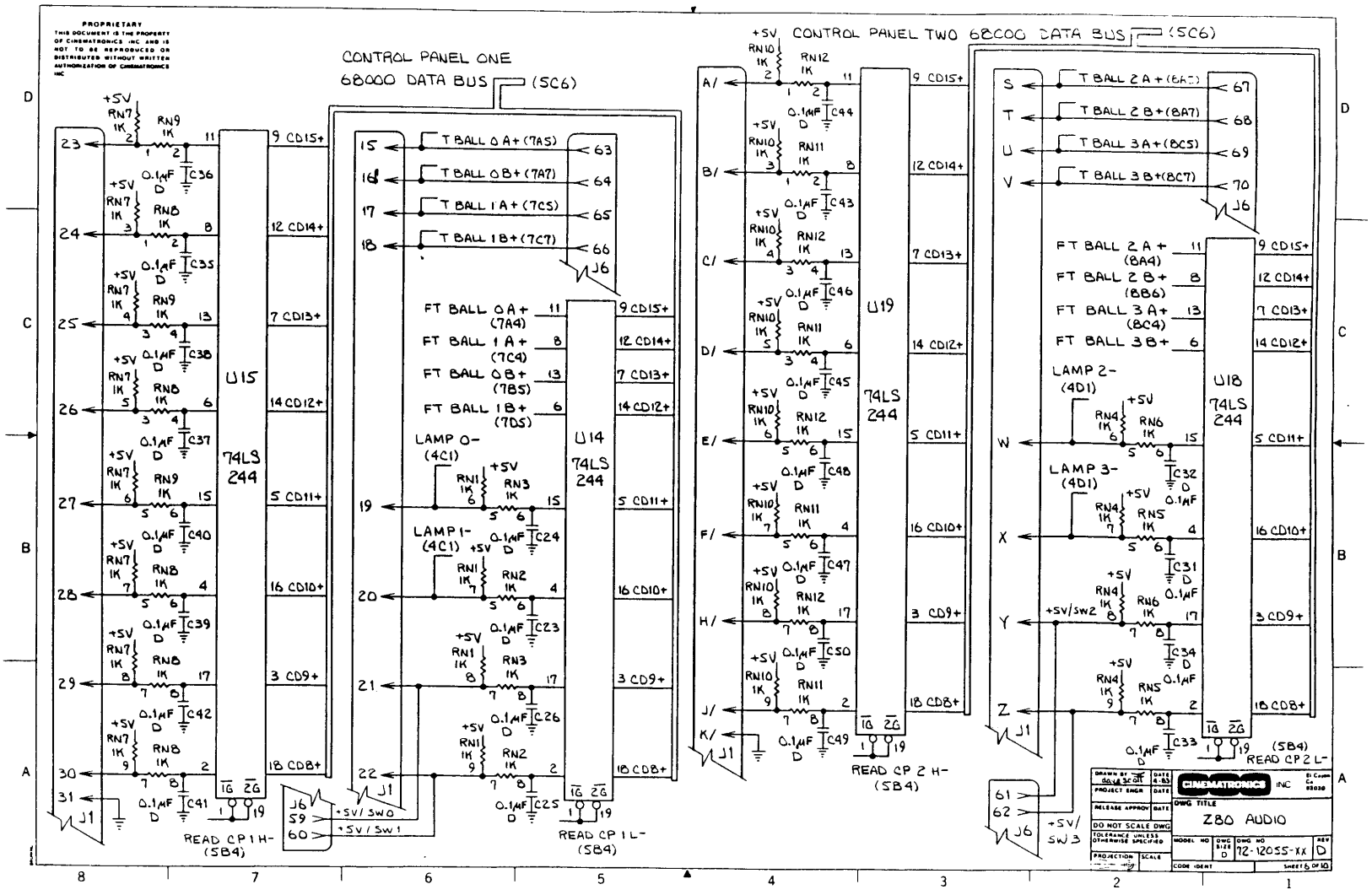
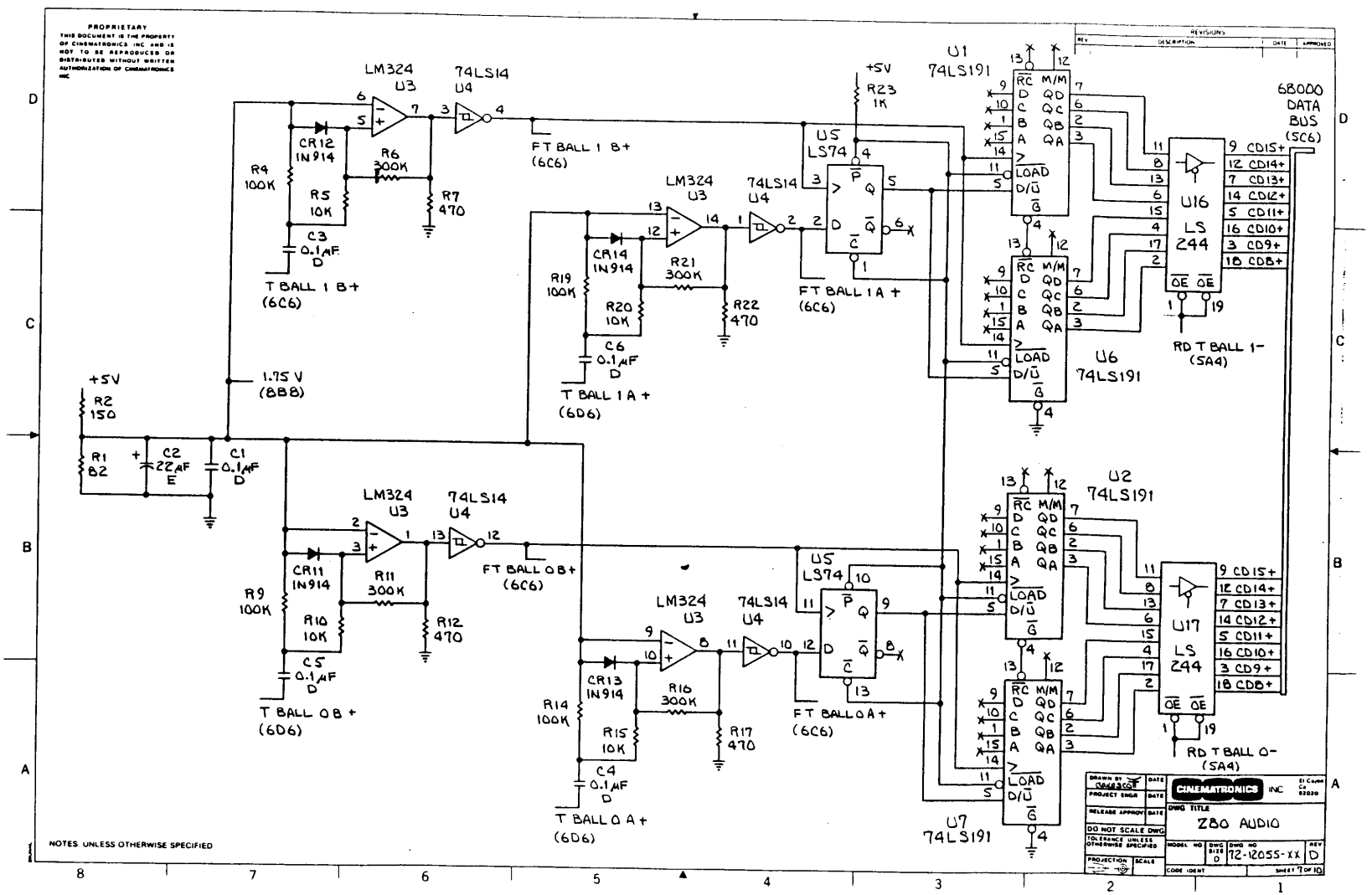
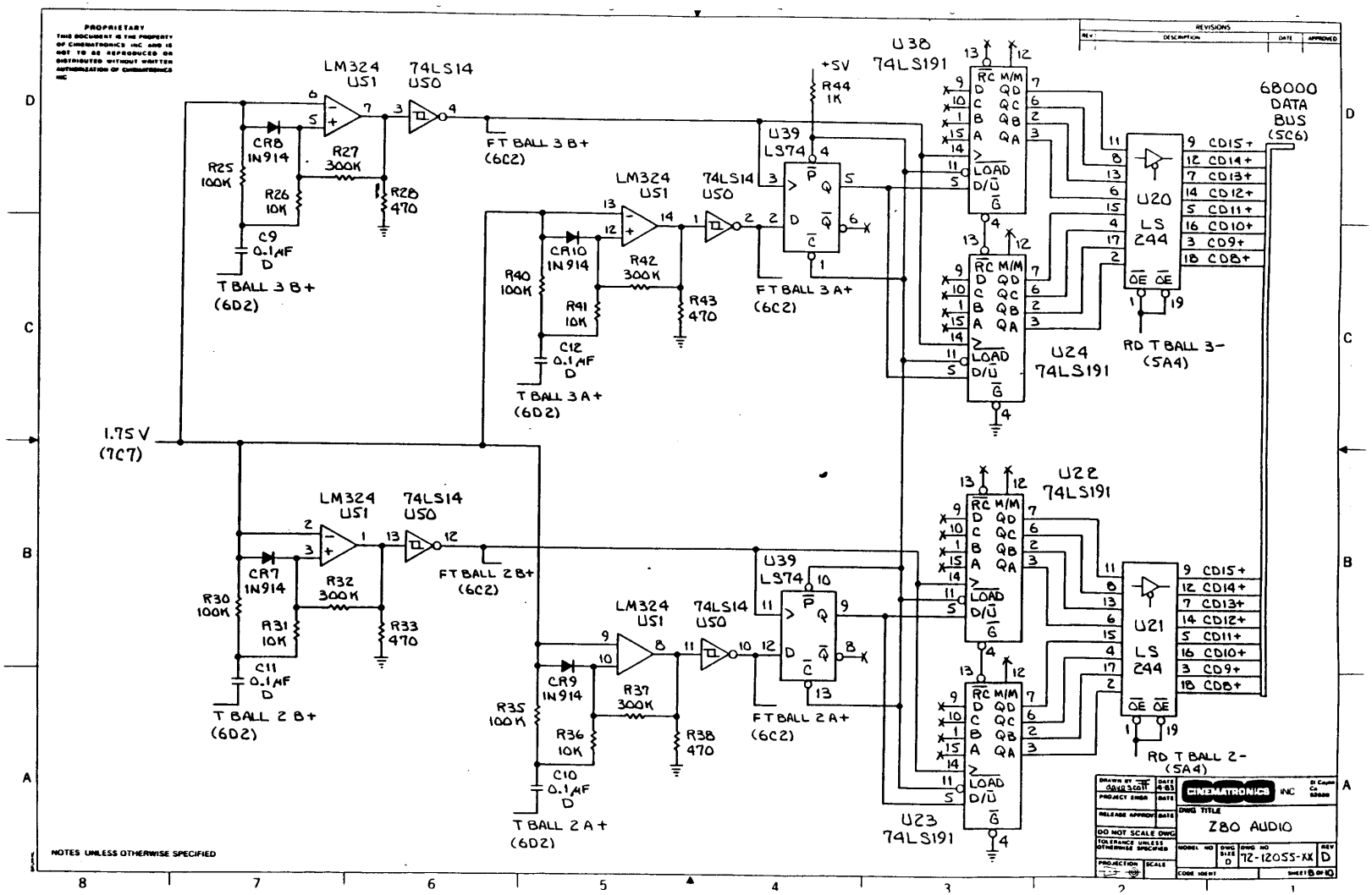
REVISIONS
REV DESCRIPTION DATE APPROVED
68000 EXPANSION
J3 40 PIN
J4 50 PIN
J6
ALL ODD PINS
U63 74LS244
U64 74LS 244
U65 74LS 245
U53 74LS138
U54 74LS138
U52 74LS138
U55 74LS138
U40 LS08
LS14 U48
68000 DATA BUS (4D3) (6D2) (6D5) (7D1) (8D1)
(SA6) CAS-
(SB7) AR/W
(SD4) RG7-
(SD4) RG6-
(SD4) RG5-
(SD4) RG4-
(SD4) RG3-
(SD4) RG2-
(SC7) AA3
(SC7) AA2
(SC7) AA1
(SC7) AD15
(SC7) AD14
(SC7) AD13
(SC7) AD12
(SC7) AD11
(SB7) AD10
(SB7) AD9
(SB7) AD8
(3B4) AUDIO CLK+
SPARE 1
SPARE 2
EXT AUDIO 0+ (3D2)
EXT AUDIO 1+ (3D2)
RG0-
LOCAL- (SB6)
LOCAL- (SC3)
W DRIVER REQ- (4B3)
W CMMD REG H- (4B8)(4C7)
W CMMD REG L- (4C7)
READ CP 2 H- (6A3)
READ CP 2 L- (6A1)
READ CP 1H- (6A7)
READ CP 1L- (6A5)
READ 68 K FLAGS- (4A4)
READ STATUS H- (4A8)(4C4)
READ STATUS L- (4C4)
RD T BALL 3- (8C2)
RD T BALL 2- (8A2)
RD T BALL 1- (7C2)
RD T BALL 0- (7A2)
CA3+ (SA5)
CA2+ (SA5)
CA1+ (SA5)
R116 4.7K
R115 7.5K
R118 4.7K
R117 7.5K
R119 470
+5V
AR/W (SD2)
A103
CAS- (SD3)
CA3+ (4B8)(4C7) (4C3)(4D7)
C 68 K RESET- (3D6)
A RESET (SD2)
STATUS FULL+ (4B6)
A11
CINEMATRONICS INC
Z80 AUDIO
DWG NO 72-12055-XX
REV D
SHEET 5 OF 10


PROPRIETARY
THIS DOCUMENT IS THE PROPERTY OF CINEMATRONICS, INC AND IS NOT TO BE REPRODUCED OR DISTRIBUTED WITHOUT WRITTEN AUTHORIZATION OF CINEMATRONICS INC
CONTROL PANEL ONE
68000 DATA BUS (SC6)
CONTROL PANEL TWO 68000 DATA BUS (SC6)
U15
74LS 244
U14
74LS 244
U19
74LS 244
U18
74LS 244
T BALL 0 A+ (7A5)
T BALL 0 B+ (7A7)
T BALL 1 A+ (7C5)
T BALL 1 B+ (7C7)
T BALL 2 A+ (8A5)
T BALL 2 B+ (8A7)
T BALL 3 A+ (8C5)
T BALL 3 B+ (8C7)
FT BALL 0 A+ (7A4)
FT BALL 1 A+ (7C4)
FT BALL 0 B+ (7B5)
FT BALL 1 B+ (7D5)
FT BALL 2 A+ (8A4)
FT BALL 2 B+ (8B6)
FT BALL 3 A+ (8C4)
FT BALL 3 B+
LAMP 0- (4C1)
LAMP 1- (4C1)
LAMP 2- (4D1)
LAMP 3- (4D1)
READ CP 1 H- (5B4)
READ CP 1 L- (5B4)
READ CP 2 H- (5B4)
READ CP 2 L- (5B4)
+SV/SW0
+SV/SW1
+SV/SW2
+SV/SW3
Z80 AUDIO
72-12055-XX
CINEMATRONICS INC


PROPRIETARY
THIS DOCUMENT IS THE PROPERTY OF CINEMATRONICS INC AND IS NOT TO BE REPRODUCED OR DISTRIBUTED WITHOUT WRITTEN AUTHORIZATION OF CINEMATRONICS INC
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
LM324 U3
74LS14 U4
+5V
R23 1K
U1 74LS191
U5 LS74
68000 DATA BUS (SC6)
U16 LS 244
U6 74LS191
U2 74LS191
U17 LS 244
U7 74LS191
R4 100K
CR12 IN914
R5 10K
R6 300K
R7 470
C3 0.1μF D
T BALL 1 B+ (6C6)
FT BALL 1 B+ (6C6)
R19 100K
CR14 IN914
R20 10K
R21 300K
R22 470
C6 0.1μF D
T BALL 1 A+ (6D6)
FT BALL 1 A+ (6C6)
RD T BALL 1- (SA4)
+5V
R2 150
R1 82
C2 22μF E
C1 0.1μF D
1.75 V (8B8)
R9 100K
CR11 IN914
R10 10K
R11 300K
R12 470
C5 0.1μF D
T BALL 0B+ (6D6)
FT BALL 0B+ (6C6)
R14 100K
CR13 IN914
R15 10K
R16 300K
R17 470
C4 0.1μF D
T BALL 0A+ (6D6)
FT BALL 0A+ (6C6)
RD T BALL 0- (SA4)
9 CD15+
12 CD14+
7 CD13+
14 CD12+
5 CD11+
16 CD10+
3 CD9+
18 CD8+
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
DO NOT SCALE DWG
MODEL NO
DWG NO
72-12055-XX
REV D
SHEET 7 OF 10


PROPRIETARY
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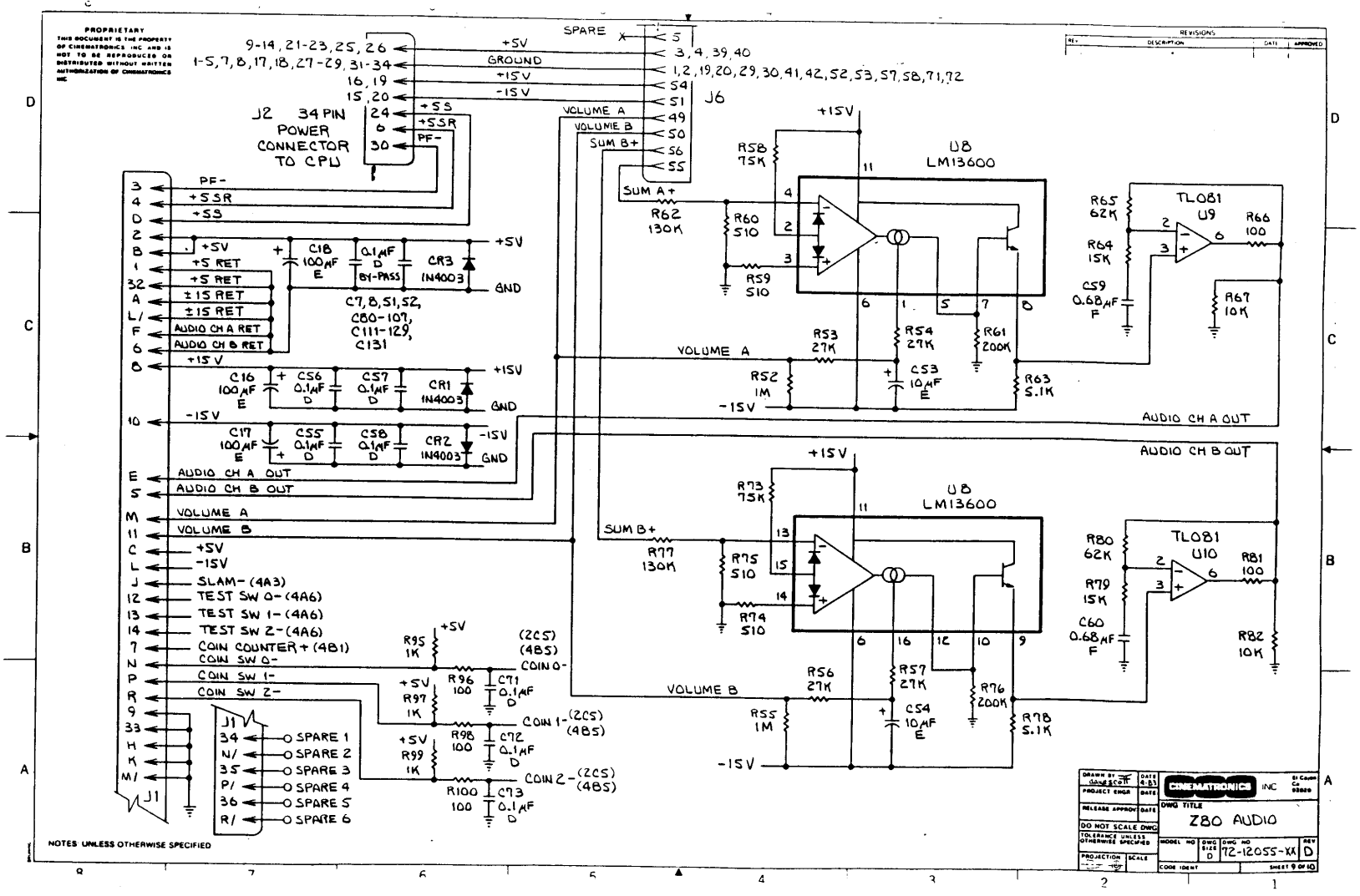
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
LM324 U51
74LS14 U50
+5V
R44 1K
U38 74LS191
U39 LS74
U20 LS 244
U24 74LS191
68000 DATA BUS (SC6)
CR8 1N914
R25 100K
R26 10K
R27 300K
R28 470
C9 0.1MF D
TBALL 3 B+ (6D2)
FT BALL 3 B+ (6C2)
CR10 1N914
R40 100K
R91 10K
R42 300K
R43 470
C12 0.1MF D
TBALL 3 A+ (6D2)
FT BALL 3 A+ (6C2)
RD T BALL 3- (5A4)
CD15+
CD14+
CD13+
CD12+
CD11+
CD10+
CD9+
CD8+
1.75 V (7C7)
CR7 1N914
R30 100K
R31 10K
R32 300K
R33 470
C11 0.1MF D
TBALL 2 B+ (6D2)
FT BALL 2 B+ (6C2)
CR9 1N914
R35 100K
R36 10K
R37 300K
R38 470
C10 0.1MF D
TBALL 2 A+ (6D2)
FT BALL 2 A+ (6C2)
U22 74LS191
U21 LS 244
U23 74LS191
RD T BALL 2- (5A4)
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
72-12055-XX
REV D
NOTES UNLESS OTHERWISE SPECIFIED


PROPRIETARY
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REVISIONS
REV DESCRIPTION DATE APPROVED
J2 34 PIN POWER CONNECTOR TO CPU
9-14, 21-23, 25, 26 +5V
1-5, 7, 8, 17, 18, 27-29, 31-34 GROUND
16, 19 +15V
15, 20 -15V
24 +5S
6 +5SR
30 PF-
SPARE
J6
5
3, 4, 39, 40
1, 2, 19, 20, 29, 30, 41, 42, 52, 53, 57, 58, 71, 72
54
51
49
50
56
55
VOLUME A
VOLUME B
SUM B+
SUM A+
PF-
+5SR
+5S
+5V
+5 RET
+5 RET
±15 RET
±15 RET
AUDIO CH A RET
AUDIO CH B RET
+15V
-15V
C18 100MF E
0.1MF D BY-PASS
CR3 IN4003
C7, 8, 51, 52, C80-107, C111-129, C131
C16 100MF E
CS6 0.1MF D
CS7 0.1MF D
CR1 IN4003
C17 100MF E
CS5 0.1MF D
CS8 0.1MF D
CR2 IN4003
GND
AUDIO CH A OUT
AUDIO CH B OUT
VOLUME A
VOLUME B
+5V
-15V
SLAM- (4A3)
TEST SW 0- (4A6)
TEST SW 1- (4A6)
TEST SW 2- (4A6)
COIN COUNTER+ (4B1)
COIN SW 0-
COIN SW 1-
COIN SW 2-
J1
SPARE 1
SPARE 2
SPARE 3
SPARE 4
SPARE 5
SPARE 6
R95 1K
R96 100
C71 0.1MF D
R97 1K
R98 100
C72 0.1MF D
R99 1K
R100 100
C73 0.1MF D
(2CS) (4BS)
COIN 0-
COIN 1-
COIN 2-
U8 LM13600
R58 75K
R60 510
R59 510
R62 130K
R53 27K
R54 27K
R61 200K
R52 1M
CS3 10MF E
R63 5.1K
U9 TL081
R65 62K
R64 15K
CS9 0.68MF F
R66 100
R67 10K
AUDIO CH A OUT
U8 LM13600
R73 75K
R75 510
R74 510
R77 130K
R56 27K
R57 27K
R76 200K
R55 1M
CS4 10MF E
R78 5.1K
U10 TL081
R80 62K
R79 15K
C60 0.68MF F
R81 100
R82 10K
AUDIO CH B OUT
NOTES UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
Z80 AUDIO
DWG NO 72-12055-XX
REV D
SHEET 9 OF 10

POWER DISTRIBUTION

IC REFERENCE	+5V	GND
U33	24	5
U13,U14,U15,U16,U17,U18,U19,U20, U21,U27,U28,U29,U30,U44,U45, U46,U47,U56,U57,U63,U64,U65, U66,U67,U68,U69,U70,U72,U73, U74,U75	20	1, 10
U58,U59	18	9
U1,U2,U6,U7,U22,U23,U24,U38, U52,U53,U54,U55,U77,U78,U79 U4,U5,U11,U12,U26,U34,U35,U36, U37,U39,U40,U41,U42,U43,U47, U48,U49,U50,U60,U61,U62,U76, U80,U81	16	8
U71	11	29
U3,U51	4	11
U31,U32	3	6
RN1,RN4,RN7,RN10	1	NONE

IC REFERENCE	+15V	-15V
U8	11	6
U9,U10	7	4

LAST REFERENCE DESIGNATORS USED:
U81, R145, C13, D14, Q6, RN12, J6

REFERENCE DESIGNATORS DELETED:
R3,8,13,18,24,29,34,39,68-72, R86-94,125,126,132,136.

C13-15,19-22,28-30,61-70,78, C79,108,109,132.

U25

LS244 IC REFERENCE	ENABLING PINS	OUTPUT PINS ENABLED
U63	1, 19	3, 5, 14, 16, 18
U73	1, 19	5, 7, 9, 12, 14

NOTES UNLESS OTHERWISE SPECIFIED

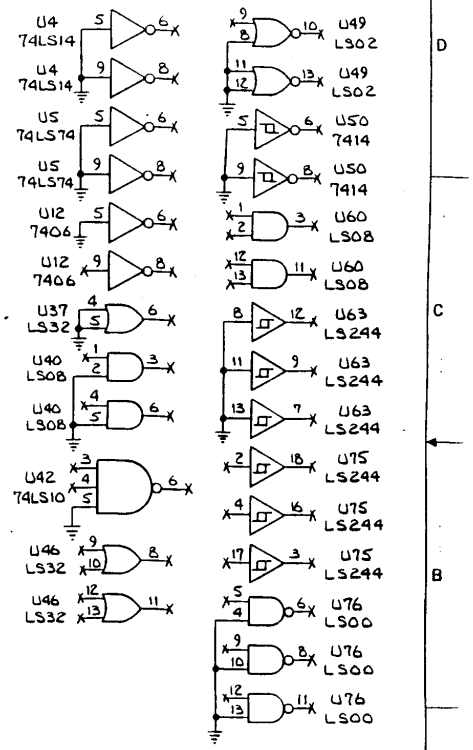
J1

PIN	FUNCTION	LOCATION
1	+5 RETURN	(9C8)
2	+5V	(9C8)
3	PF-	(9C8)
4	+SSR	(9D8)
5	AUDIO CH B OUT	(9B8)
6	AUDIO CH B RET	(9C8)
7	COIN COUNTER+	(9B8)
8	+15V	(9C8)
9	GROUND	(9A8)
10	-15V	(9C8)
11	VOLUME	(9B8)
12	TEST SW 0-	(9B8)
13	TEST SW 1-	(9B8)
14	TEST SW 2-	(9B8)
15	T BALL 0 A+	(6D6)
16	T BALL 0 B+	(6D6)
17	T BALL 1 A+	(6D6)
18	T BALL 1 B+	(6C6)
19	LAMP 0-/SWITCH INPUT	(6B6)
20	LAMP 1-/SWITCH INPUT	(6B6)
21	+5V/SW0	(6A6)
22	+5V/SW1	(6A6)
23	SWITCH INPUTS FOR CONTROL PANEL ONE	(6D8)
24		(6C8)
25		(6C8)
26		(6C8)
27		(6B8)
28		(6B8)
29		(6A8)
30		(6A8)
31	GROUND	(6A8)
32	+5 RETURN	(9C8)
33	GROUND	(9A8)
34	SPARE 1	(9A7)
35	SPARE 3	(9A7)
36	SPARE 5	(9A7)
A	-15 RETURN	(9C8)
B	+5V	(9C8)
C	+5V	(9B8)
D	+5S	(9D8)
E	AUDIO CH A OUT	(9B8)
F	AUDIO CH A RET	(9C8)
H	GROUND	(9A8)
J	SLAM-	(9B8)
K	GROUND	(9A8)
L	-15V	(9B8)
M	VOLUME A	(9B8)
N	COIN SW 0-	(9A8)
P	COIN SW 1-	(9A8)
R	COIN SW 2-	(9A8)
S	T BALL 2 A+	(6D3)
T	T BALL 2 B+	(6D3)
U	T BALL 3 A+	(6D3)
V	T BALL 3 B+	(6D3)
W	LAMP 2-/SWITCH INPUT	(6B3)
X	LAMP 3-/SWITCH INPUT	(6B3)
Y	+5V/SW2	(6B3)
Z	+5V/SW3	(6A3)
A/	SWITCH INPUTS FOR CONTROL PANEL TWO	(6D4)
B/		(6D4)
C/		(6C4)
D/		(6C4)
E/		(6C4)
F/		(6B4)
H/		(6B4)
J/		(6A4)
K/	GROUND	(6A4)
L/	-15 RETURN	(9C8)
M/	GROUND	(9A8)
N/	SPARE 2	(9A7)
P/	SPARE 4	(9A7)
R/	SPARE 6	(9A7)

J6

PIN	FUNCTION	LOCATION
1	GROUND	(9D5)
2	GROUND	(9D5)
3	+5V	(9D5)
4	+5V	(9D5)
5	SPARE	(9D5)
6	BA12+	(1D3)
7	BA11+	(1D3)
8	BA10+	(1D3)
9	BA9+	(1D3)
10	BA8+	(1D3)
11	BA7+	(1D3)
12	BA6+	(1D3)
13	BA5+	(1D3)
14	BA4+	(1C3)
15	BA3+	(1C3)
16	BA2+	(1C3)
17	BA1+	(1C3)
18	BA0+	(1C3)
19	GROUND	(9D5)
20	GROUND	(9D5)
21	BD7+	(1B1)
22	BD6+	(1B1)
23	BD5+	(1B1)
24	BD4+	(1B1)
25	BD3+	(1B1)
26	BD2+	(1B1)
27	BD1+	(1B1)
28	BD0+	(1B1)
29	GROUND	(9D5)
30	GROUND	(9D5)
31	SEL ROM 0-	(1C3)
32	SEL ROM 1-	(1C3)
33	SEL ROM 2-	(1C3)
34	SEL ROM 3-	(1C3)
35	G RAM 1-	(1A3)
36	BWT-	(1A3)
37	RPL-	(1B3)
38	WPL-	(1A3)
39	+5V	(9D5)
40	+5V	(9D5)
41	GROUND	(9D5)
42	GROUND	(9D5)
43	G1Q+	(2D1)
44	G11+	(2D1)
45	CTC 1-	(2D1)
46	CTC 2-	(2C1)
47	EXT AUDIO 0+	(5A1)
48	EXT AUDIO 1+	(5A1)
49	VOLUME A	(9D5)
50	VOLUME B	(9D5)
51	-15V	(9D5)
52	GROUND	(9D5)
53	GROUND	(9D5)
54	+15V	(9D5)
55	SUM A+	(9D5)
56	SUM B+	(9D5)
57	GROUND	(9D5)
58	GROUND	(9D5)
59	+5V/SW0	(6A7)
60	+5V/SW1	(6A7)
61	+5V/SW2	(6A3)
62	+5V/SW3	(6A3)
63	T BALL 0 A+	(6D5)
64	T BALL 0 B+	(6D5)
65	T BALL 1 A+	(6C5)
66	T BALL 1 B+	(6C5)
67	T BALL 2 A+	(6D1)
68	T BALL 2 B+	(6D1)
69	T BALL 3 A+	(6D1)
70	T BALL 3 B+	(6D1)
71	GROUND	(9D5)
72	GROUND	(9D5)

SPARE GATES



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

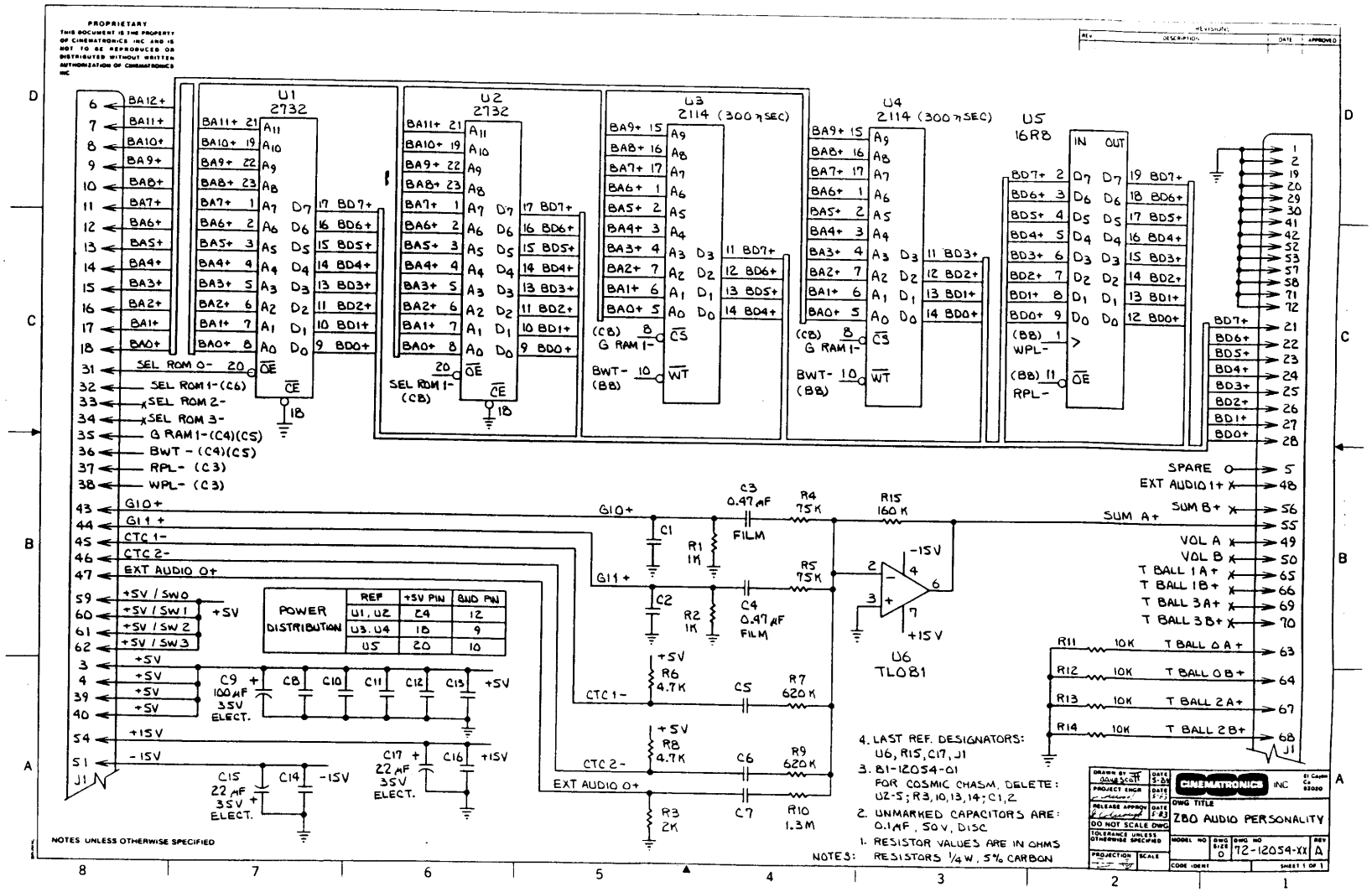
MATERIAL
FINISH
DRAWN BY DAVESCO — DATE
PROJECT ENGR — DATE
RELEASE APPROV — DATE
DO NOT SCALE DWG
TOLERANCE UNLESS OTHERWISE SPECIFIED
PROJECTION — SCALE

CINEMATRONICS INC — 81 Comm Ct — 95020

DWG TITLE: Z80 AUDIO

MODEL NO | DWG SIZE D | DWG NO 72-12055-XX | REV D

CODE IDENT | SHEET 10 OF 10


PROPRIETARY
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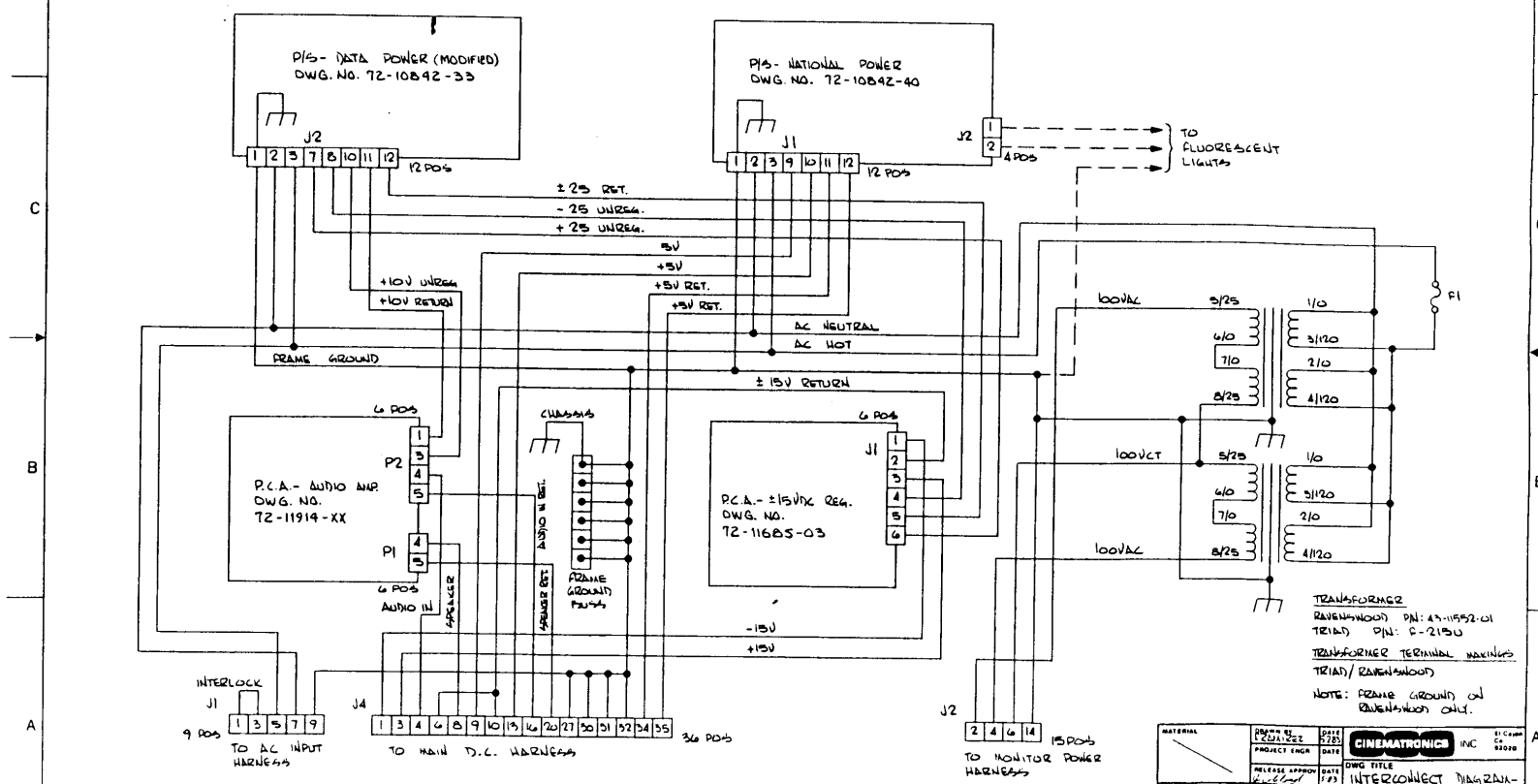
U1 2732
U2 2732
U3 2114 (300 nSEC)
U4 2114 (300 nSEC)
U5 16R8
U6 TL081
SEL ROM 0-
SEL ROM 1-(C6)
SEL ROM 2-
SEL ROM 3-
G RAM 1-(C4)(C5)
BWT - (C4)(C5)
RPL- (C3)
WPL- (C3)
SEL ROM 1-(C8)
G RAM 1-
BWT-
WPL-
RPL-
POWER DISTRIBUTION
REF
+5V PIN
GND PIN
U1, U2
U3, U4
U5
EXT AUDIO 0+
EXT AUDIO 1+
SUM A+
SUM B+
VOL A
VOL B
T BALL 1A+
T BALL 1B+
T BALL 3A+
T BALL 3B+
T BALL 0A+
T BALL 0B+
T BALL 2A+
T BALL 2B+
SPARE
4. LAST REF. DESIGNATORS: U6, R15, C17, J1
3. 81-12054-01 FOR COSMIC CHASM, DELETE: U2-5; R3, 10, 13, 14; C1, 2
2. UNMARKED CAPACITORS ARE: 0.1 MF, 50V, DISC
1. RESISTOR VALUES ARE IN OHMS
NOTE 3: RESISTORS 1/4 W, 5% CARBON
NOTES: UNLESS OTHERWISE SPECIFIED
CINEMATRONICS INC
DWG TITLE
ZBO AUDIO PERSONALITY
DO NOT SCALE DWG
DWG NO 72-12054-XX
REV A
SHEET 1 OF 1

REVISIONS

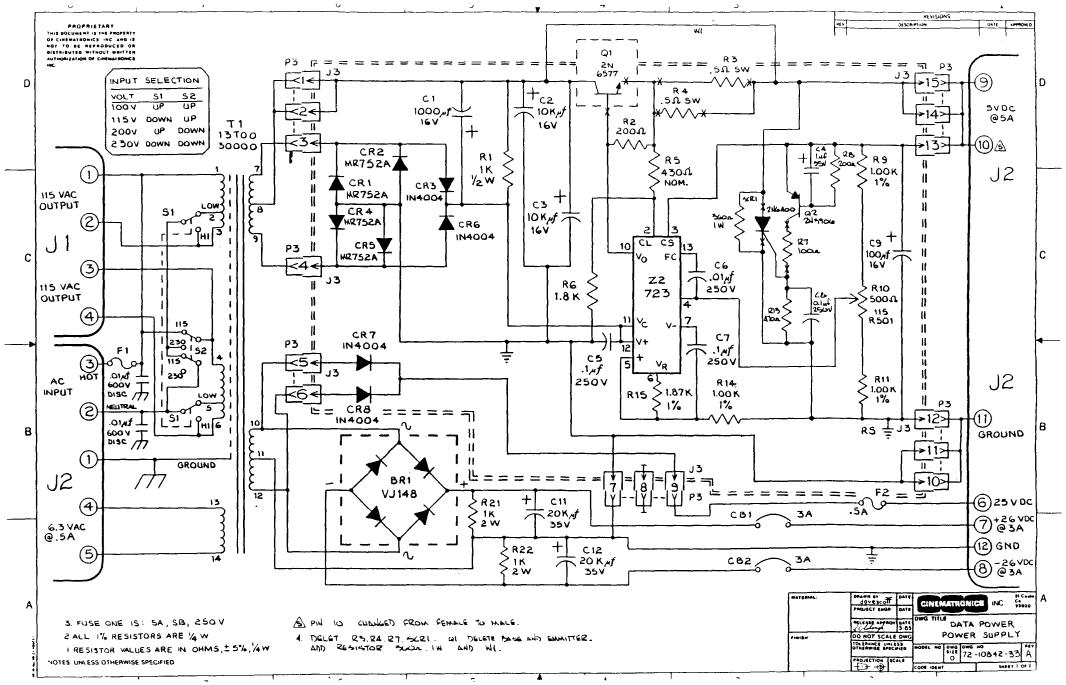
REV	DESCRIPTION	DATE	APPROVED

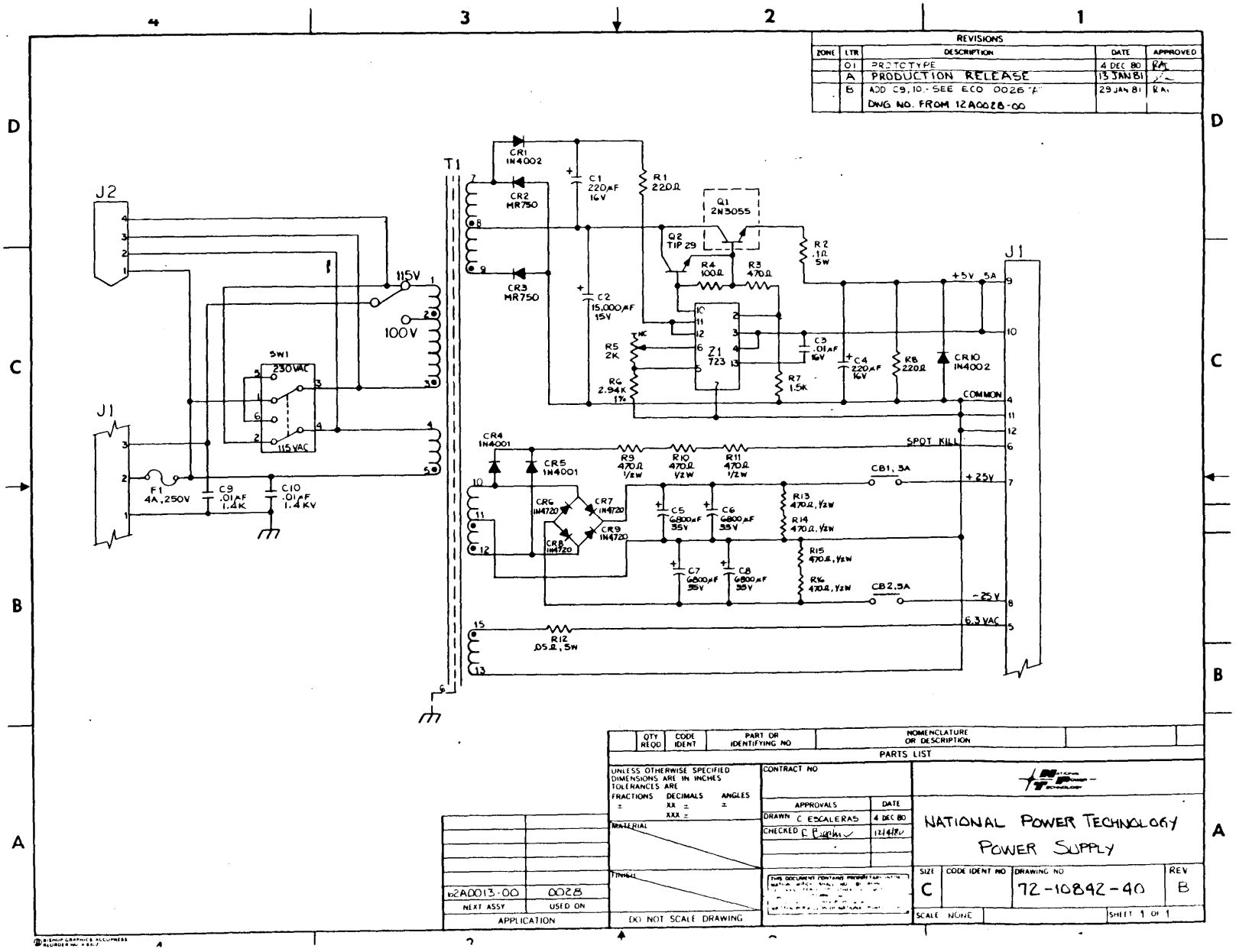


1. ALL CONNECTOR PINS NOT SHOWN ARE UNUSED.

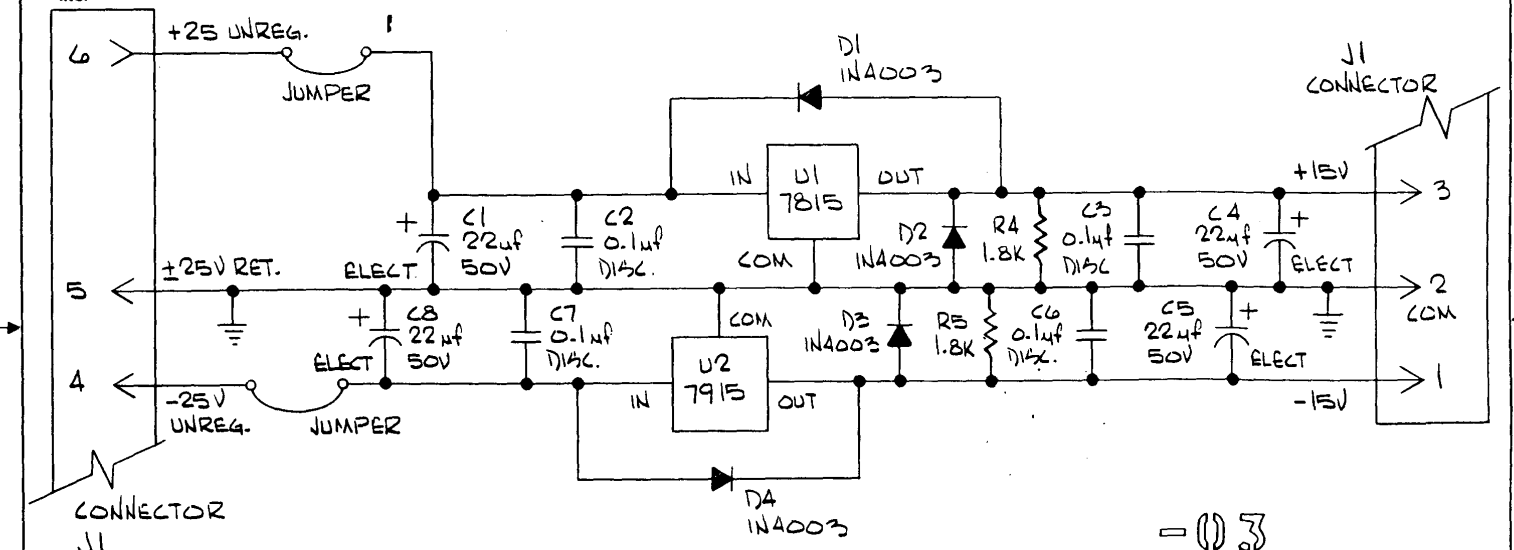
NOTES UNLESS OTHERWISE SPECIFIED

MATERIAL	DRAWN BY: L. GALINDEZ	DATE: 7-85	CINEMATRONICS INC 91 Commercial Co 92020
	PROJECT ENGR	DATE	
	RELEASE APPROV	DATE 1-87	DWG TITLE: INTERCONNECT DIAGRAM- POWER SUPPLY PLATE
FINISH	DO NOT SCALE DWG		
	TOLERANCE UNLESS OTHERWISE SPECIFIED		MODEL NO: D; DWG SIZE: D; DWG NO: 11-12110-01; REV: A
	PROJECTION	SCALE: NONE	CODE IDENT: SHEET 1 OF 1


PROPRIETARY
INPUT SELECTION
VOLT S1 S2
100V UP UP
115V DOWN UP
200V UP DOWN
230V DOWN DOWN
T1
13T00
30000
115 VAC OUTPUT
J1
115 VAC OUTPUT
AC INPUT
HOT
NEUTRAL
GROUND
J2
6.3 VAC @.5A
S1
F1
.01μf 600V DISC
.01μf 600V DISC
CR1 MR752A
CR2 MR752A
CR3 IN4004
CR4 MR752A
CR5 MR752A
CR6 IN4004
CR7 IN4004
CR8 IN4004
BR1 VJ148
C1 1000μf 16V
C2 10Kμf 16V
C3 10Kμf 16V
C5 .1μf 250V
C6 .01μf 250V
C7 .1μf 250V
C9 100μf 16V
C11 20Kμf 35V
C12 20Kμf 35V
R1 1K ½W
R2 200Ω
R3 .5Ω 5W
R4 .5Ω 5W
R5 430Ω NOM.
R6 1.8K
R9 1.00K 1%
R10 500Ω 115 R501
R11 1.00K 1%
R14 1.00K 1%
R15 1.87K 1%
R21 1K 2W
R22 1K 2W
Q1 2N 6577
Z2 723
CB1 3A
CB2 3A
F2 .5A
5VDC @5A
J2
GROUND
25 VDC
+26 VDC @3A
GND
-26 VDC @3A
3. FUSE ONE IS: 5A, SB, 250 V
2 ALL 1% RESISTORS ARE ¼ W
1 RESISTOR VALUES ARE IN OHMS, ± 5%, ¼ W
NOTES UNLESS OTHERWISE SPECIFIED
PIN 10 CLIPPED FROM FEMALE TO MALE.
DELET R9, 24, 27 & C21. W1 DELETE BASE AND EMMITTER. AND R6 & R14 FOR 1.5K 1W AND W1.
CINEMATRONICS INC
DWG TITLE
DATA POWER POWER SUPPLY
DWG NO 72-10842-33
SIZE A
SHEET 1 OF 1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
01 | PROTOTYPE | 4 DEC 80 | RAL
A | PRODUCTION RELEASE | 13 JAN 81
B | ADD C9, 10 - SEE ECO 0026 | 29 JAN 81 | RAL
DWG NO. FROM 12A0028-00
J2
J1
T1
SW1
230VAC
115VAC
115V
100V
F1 4A, 250V
C9 .01μF 1.4K
C10 .01μF 1.4 KV
CR1 IN4002
CR2 MR750
CR3 MR750
C1 220μF 16V
C2 15,000μF 15V
R1 220Ω
Q1 2N3055
Q2 TIP 29
R2 .1Ω 5W
R3 470Ω
R4 100Ω
R5 2K
R6 2.94K 1%
Z1 723
C3 .01μF 10V
C4 220μF 16V
R7 1.5K
R8 220Ω
CR10 IN4002
+5V 5A
COMMON
SPOT KILL
CR4 IN4001
CR5 IN4001
R9 470Ω 1/2W
R10 470Ω 1/2W
R11 470Ω 1/2W
CB1, 3A
+25V
CR6 IN4720
CR7 IN4720
CR8 IN4720
CR9 IN4720
C5 6800μF 35V
C6 6800μF 35V
C7 6800μF 35V
C8 6800μF 35V
R13 470Ω, 1/2W
R14 470Ω, 1/2W
R15 470Ω, 1/2W
R16 470Ω, 1/2W
CB2, 5A
-25V
6.3 VAC
R12 .05Ω, 5W
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
± XX ± ±
XXX ±
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
DRAWN C ESCALERAS | 4 DEC 80
CHECKED C P [illegible] | 12/4/80
NATIONAL POWER TECHNOLOGY
POWER SUPPLY
SIZE C | CODE IDENT NO | DRAWING NO 72-10892-40 | REV B
SCALE NONE | SHEET 1 OF 1
12A0013-00 | 0028
NEXT ASSY | USED ON
APPLICATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



-03

UNUSED DES:
R1, R2, R3

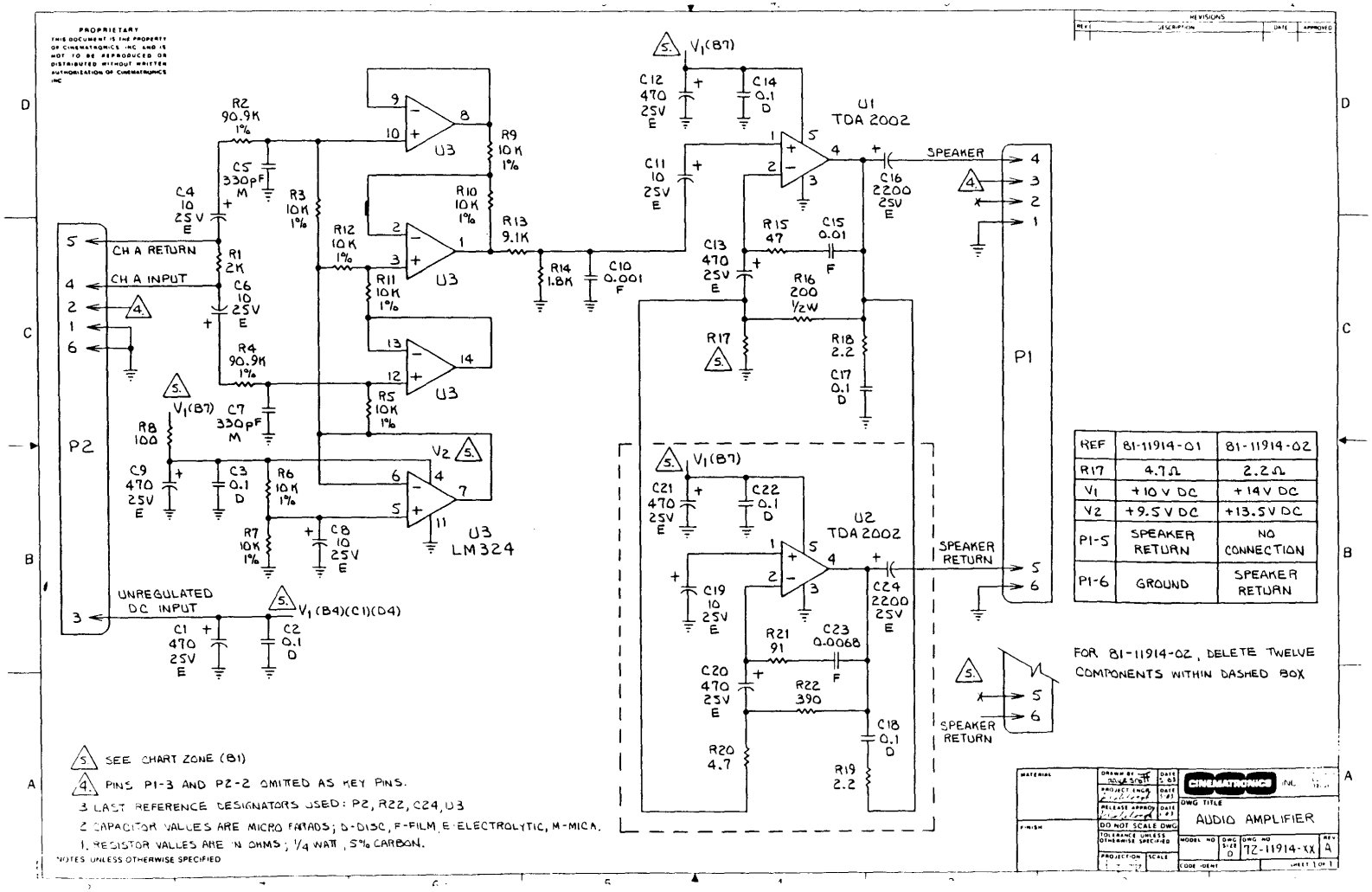
LAST DES:
C8, D4, R5

2. R4 AND R5 VALUES ARE IN OHMS.
1. R4 AND R5 ARE 1/4 WATTS, 5% CARBON.

NOTES:

MATERIAL:	DRAWN BY: F. RAMIREZ	DATE 5283	CINEMATRONICS INC. El Cajon Ca. 92020
	PROJECT ENGR:	DATE 5-83	
FINISH: BREAK ALL SHARP EDGES AND DEBURR ALL HOLES.	RELEASE APPROV:	DATE 5-93	DWG TITLE: SCHEMATIC DIAGRAM-REGULATOR +15 -15 VOLTS
	DO NOT SCALE DWG		
	TOLERANCE: UNLESS OTHERWISE SPECIFIED		MODEL NO. / DWG SIZE B / DWG NO. 72-11685-03 / REV. A
	PROJECTION:	SCALE: NONE	CODE IDENT. / SHEET 1 OF 1

BRUNING 40/21 40423



REF	81-11914-01	81-11914-02
R17	4.7Ω	2.2Ω
V1	+10 V DC	+14 V DC
V2	+9.5 V DC	+13.5 V DC
P1-5	SPEAKER RETURN	NO CONNECTION
P1-6	GROUND	SPEAKER RETURN

FOR 81-11914-02, DELETE TWELVE COMPONENTS WITHIN DASHED BOX

5. SEE CHART ZONE (B1)

4. PINS P1-3 AND P2-2 OMITTED AS KEY PINS.

3 LAST REFERENCE DESIGNATORS USED: P2, R22, C24, U3

2 CAPACITOR VALUES ARE MICRO FARADS; D-DISC, F-FILM, E-ELECTROLYTIC, M-MICA.

1. RESISTOR VALUES ARE IN OHMS; 1/4 WATT, 5% CARBON.

NOTES UNLESS OTHERWISE SPECIFIED

CINEMATRONICS INC

DWG TITLE: AUDIO AMPLIFIER

DWG NO 72-11914-XX REV A

SHEET 1 OF 1

COSMIC CHASM ONBOARD TEST

1. Push reset switch next to DIP switch on processor board

2. Push test button on panel with volume control and coin counter

3. Color test pattern should now appear on screen

4. Push test button again

5. Crosshatch test pattern should appear on screen

6. Push test button again

7. You should now be in control panel/audio test mode.

   NOTE: Audio will be heard only if attract mode audio is turned on (processor DIP switch, position 6)

   A spaceship and multicolored test pattern should appear.
   Rotating shaft encoder should rotate ship
   Pushing thrust button(s) should cause ship to move slowly with thrust sound.
   Pushing fire button(s) should cause ship to fire with fire sound.
   Pushing shield button(s) should cause shield to appear with shield sound.
   Pushing one or two player start buttons should cause "ONE PLAYER" or "TWO PLAYER" to appear at bottom of screen.

8. Push test button again.

9. You should now be in game configuration mode.

   Game setup information and a multicolored test pattern should be on the screen.
   Changing the setting of the DIP switch on the processor board should change the corresponding information on the display.

10. Push the reset button on the processor board to exit test mode and enter changes in the game setup.

NOTE: Turning position 8 of the processor DIP switch "on" has the same effect as pushing the test button.

4/6/83