ACORN

BBC Master 128

SERVICE MANUAL

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British Broadcasting Corporation
Master Series Microcomputer
Service Manual

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WARNING: THE COMPUTER MUST BE EARTHED

IMPORTANT: The wires in the mains lead for the apparatus are coloured in accordance with the following code:

Green & Yellow	Earth
Blue	Neutral
Brown	Live

The moulded plug must be used with the fuse and fuse carrier firmly in place. The fuse carrier is of the same basic colour (though not necessarily the same shade of that colour) as the coloured insert in the base of the plug. Different manufacturers' plugs and fuse carriers are not interchangeable. In the event of loss of the fuse carrier, the moulded plug MUST NOT be used. Either replace the moulded plug with another conventional plug wired as detailed below, or obtain a replacement fuse carrier from an authorised Acorn dealer. In the event of the fuse blowing it should be replaced, after clearing any faults, with a 3 amp fuse that is ASTA approved to BS1362.

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate plug fitted and wired as previously noted. The moulded plug which was cut off must be disposed of as it would be a potential shock hazard if it were to be plugged in with the cut off end of the mains cord exposed.

As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug, proceed as follows:

The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E, or by the safety earth symbol -I-, or coloured either green or green and yellow.

The wire which is coloured blue must be connected to the terminal which is marked with the letter N, or coloured black.

The wire which is coloured brown must be connected to the terminal which is marked with the letter L, or coloured red.

BBC Master Series Microcomputer Service Manual

Contents

1 Introduction

This manual is intended to provide the information required to diagnose and repair faults on the BBC Master Series Microcomputer which was designed by Acorn Computers Ltd of Cambridge, England.

The information contained in this manual is aimed at service engineers and Acorn dealers who will be servicing the BBC Master Series Microcomputer on behalf of Acorn Computers Ltd.

2 Packaging and installation

The microcomputer is supplied with three-part moulded polystyrene packing in a cardboard box. Supplied with the microcomputer is a Welcome Guide, an aerial lead, a welcome tape, a welcome disc, two reversible keyboard inserts, a VIEW reference card, a ViewSheet reference card, and a guarantee card.

The mains supply for UK models is 240V AC 50Hz. The microcomputer is supplied with a moulded 13 amp square pin plug. If this plug is unsuitable then it must be cut off and thrown away. Instructions for fitting a replacement plug are given right at the front of this manual.

The microcomputer is turned on by a switch at the back of the microcomputer next to the mains lead.

Do not use the microcomputer in conditions of extreme heat, cold, humidity or dust or in places subject to vibration. Do not block ventilation under or behind the computer. Ensure that no foreign objects are inserted through any openings in the microcomputer.

3 Disassembly and assembly

To service the BBC Master Series Microcomputer, first disconnect the power supply plug from the mains and remove all peripheral connections from the computer.

To disassemble

The lid of the microcomputer case may be removed after undoing the four fixing screws underneath the case. DO NOT remove the lid with the mains power connected.

Inside the microcomputer are four main sub-assemblies:
keyboard
speaker and battery unit (the cartridge nest)
power supply unit
main printed circuit board

To remove the keyboard, first unplug the 2 keyboard connectors from the main printed circuit board. Undo the 3 screws holding the keyboard to the case bottom, and the 1 screw which holds it to the power supply unit.

To remove the speaker and battery unit, simply lift the casing upwards and then unplug the two connectors joining it to the board.

The power supply unit is connected to the main circuit board by seven push-on connectors which must be unplugged. Three screws on the underside of the case are undone allowing the unit to be removed. On reassembly, ensure that the same type of screw is used (M3x6mm).

The main printed circuit board is removed complete with the metal back-plate. To remove the main printed circuit board, undo the 4 fixing screws which pass through the cartridge connectors into the case bottom, and the 1 screw which holds the metal back-plate to the power supply unit. Remove the circuit board from the case by lifting it slightly at the rear and then sliding it backwards.

To reassemble

Replace the main printed circuit board by putting the front edge (with connector headers) in first and pulling it forwards until the metal back-plate drops in. Make sure that all the lugs on the lower case locate with all the correct points on the PCB and back-plate. Replace the 4 PCB fixing screws which pass through the cartridge connectors, and the single screw which joins the back-plate to the power supply unit.

Reconnect the power supply, being careful to route the wires neatly, and connect the wires (seven) to the push-on connectors on the PCB, being very careful to get the polarity right.

PCB connectors marked +5V must have a red wire attached (three)
PCB connectors marked OV must have a black wire attached (three).
The connector marked -5V has the purple wire attached (one).

Replace the speaker and battery unit, first plugging the two connectors into their correct positions on the board, the battery connector to PL8 either way round, and the speaker connector to PL9 either way round. Note that although the battery connector can be plugged either way round, it must locate on all three pins or the polarity will be wrong. Check carefully.

Replace the keyboard. Replace the 4 screws, 3 to the lower case and 1 to the power supply unit. Be careful to reconnect the keyboard ribbon sockets so that all the pins are engaged; it is easy to displace the connectors one pin to right or left.

Make one final check that all reconnections have been made correctly, especially the power supplies which will short circuit if any two are reversed.

Replace the lid, and insert and tighten the four fixing screws.

4 Selection links

LK1 PCB track, made A: 1MHz Bus Audio Input/Output

2 position link.

In the-A position the 1MHz Bus signal is an input to the computer's audio mixer.
In the B position the 1MHz Bus signal is an output from the computer's audio circuit (Minimum load 1k ohm).

This link is a permanent track in the A position. The track must be cut before a wire link is used to make the B position.

LK2 PCB track, made: Cartridge -5V
decoupler. One position link.
In some instances, particular cartridge hardware may need a -5V supply that is decoupled from the main computer -5V load. To do this R9 needs to be fitted and LK2 which is a track on the circuit board should be cut.

LK3 : Not present.

LK4 plug, made: Clock chip IRQ.

One position link.

The 6818 clock/RAM chip has a daily alarm function built in. When the alarm is triggered, the CPU is interrupted via its IRQ line. Removing the shunt from LK4 disconnects the CPU IRQ line to the clock line. This function is not supported by the operating system as this feature may not be present in future versions of the circuit board. Consequently the clock chip must be directly operated by the application software.

LK5 PCB track, made East: CSYNC
polarity. Two position link.
The polarity of the composite synchronisation signal is determined by this link. It is supplied as a track on the PCB causing negative synchronisation polarity. This track must be broken and a piece of wire used to make the other side of the link for positive synchronisation.

LK6(0) and LK6(1) plug, made A B: Main Clock Select.

Multi-function link.

This group of 4 pins can take either one or two shorting plugs as follows:

Link between A and B - The computer main 16MHz reference is provided by on-board circuitry. This is normally how computers are shipped.

Link between B and D - The computer main 16 MHz reference must be provided from pin A17 on either of the cartridge connectors. Note that in this case a clock source MUST be provided or the dynamic memories could be destroyed.

Link between C and D - The cartridges are clocked by the 8 MHz signal from the computer. This is a synchronous signal with the 2 MHz (phi2) signal, also supplied to the cartridges. Note that the link between A and B must also be fitted.

LK7 PCB track, made East: Video
polarity. Two position link.
The polarity of the video RGB signals is determined by this link. It is supplied as a track on the bottom of the PCB causing true polarity. This track must be broken and a piece of wire used to make the link West for negative polarity.

LK8 : Not present.

LK9 : Not present.

LK10 fitted for NTSC only: Channel Select.

Two position link.

When used with NTSC VHF televisions, the modulator enables one of two channels to be selected. Note that the computer as supplied for use in the UK is fitted with a UHF modulator so LK10 is not fitted.

LK11 : Not present.

LK12 Plug, made B (East): CSYNC/Cartridge Machine
Detect. Two position link.
Position A - This connection to the computer CSYNC line is provided for GENLOCK purposes.

Position B - Certain hardware cartridges may need to detect whether they are plugged into a Master Series computer or an Acorn Electron. Master computers are shipped with this link in the B position, causing a logic LOW to appear on pin A10 of the cartidges. The Electron has no connection to this pin.

LK13 PCB track, made West: A to D converter reference select.

Two position link.

As shipped, this link is a track on the bottom of the PCB causing the A to D converter reference voltage input to be 1.8V.

If the LK13 track is cut then the voltage reference must be applied between analogue ground and Vref on the external connector.

If the LK13 track is cut and LK13 made East with a wire link, a precision reference can be fitted in the position PR1 shown on the circuit diagram.

LK14 PCB track, made: Serial data clock reference. One position link.
As shipped, this link is a track on the PCB connecting the CHROMA chip 1.23MHz output to the Serial Processor. This link is provided for production purposes and should not be modified.

LK15 PCB track, made West: PAL/NTSC select. Two position link.
As shipped in the UK, this link is a track on the bottom of the PCB causing the CHROMA chip to encode colour information on to the television output in PAL format. If the track is cut and a wire link used to make the other side of the link, then colour information will be encoded in NTSC. In general, televisions within the UK can only accept the PAL format.

LK16 wire link, not fitted: Chrominance information luma trap bypass. One position link.
This link is not normally fitted. It is provided for those applications where filtering of the luminance information from the chrominance part of the television signal is not required.

LK17 : Not present.

LK18 plug, made West: Paged ROM/RAM Select. Two position link.
When fitted in the West position, this link causes 16Kbyte of RAM to appear in each of the "sideways" memory "slots" 6 and 7.

When fitted in the East position, a 32Kbyte ROM occupying slots 6 and 7 may be plugged into socket labelled 1C41.

LK19 plug, made West: Paged ROM/RAM Select.

Two position link.

When fitted in the West position, this link causes 16Kbyte of RAM to appear in each of the "sideways" memory "slots" 4 and 5.

When fitted in the East position, a 32Kbyte ROM occupying slots 4 and 5 may be plugged into socket labelled IC37.

LK20 : Not present.

LK21 plug, not made: Light Pen Strobe to cartridge.

This link is not normally made, so position B10 on the cartridges is merely a connection from one to the other. When the shunt is fitted, the CRTC Light Pen Strobe input is connected to B10. This is to facilitate GENLOCK and an alternative LPSTB connection to the rear analogue connector.

5 Hardware description

5.1 Introduction

The Master Series Microcomputer consists of a central processing unit with associated memory and various input/output devices for communication with external equipment. Only a fully configured system will be described here although reference to sub-systems will be made where relevant.

The Core Machine

All input/output (I/O) computing is performed by a 65C12 CPU with its principal ancillary components:-

128 Kbyte of Dynamic Random Access memory:- Special expansion options allow a further expansion of 64 Kbyte. Dedicated hardware can be used to expand this almost indefinitely.

262 Kbyte of Read Only Memory:- Special expansion options allow a further expansion of approximately 1/2 Mbyte of ROM. Plug in cartridges are available which accept up to 256 Kbyte of ROM.

Internal I/O

Various I/O devices operate solely within the confines of the system to either improve facilities or increase throughput. These are as follows:-

6522 VIA devices - Two of these are provided and interface to:-

1) A 93 contact keyboard with 2 key rollover.

3-Channel sound generator with additional noise channel. Battery backed up Real-Time Clock and fifty bytes of RAM.
2) The Printer Port and User Port

Co-processors

These consist of an additional CPU with associated memory. They have no I/O capability of their own and depend entirely on the main processor to supply such information. They do all the computation not associated with I/O operations.

When a co-processor is not fitted, the main processor has to perform both I/O and non I/O computation.

External I/O

Video display:- A 6845 CRT controller is provided to format the output from ROB, composite video and PAL/NTSC connectors.

Analogue to Digital Converter:- A four channel A-D converter provides 10 bit binary conversions in 5ms. The absolute accuracy will depend on the conditions of use.

Tape Interface:- Facilities to both save and retrieve data from audio cassettes is provided.

Disc Interface:- Facilities to both save and retrieve data from standard Shugart connected media. Filing systems are provided to support data encoded in FM or MFM.

Network Interface:- Connection to the ECONET is provided by a 68B54 advanced data link controller. This is fitted on a daughter board and may as such be fitted as an optional extra (standard on the ET machine).

1MHz Bus:- The standard BBC computer 1MHz bus is provided.

External Second Processor:- An external second processor may be connected. Selection of either internal co-processor or external second processor is performed by software. Only one second or co-processor can be active at a time.

Centronics Printer Port:- Connection is provided for the standard parallel printer port configuration.

User Port:- The user port is an eight bit bidirectional bus with two extra handshaking/serial lines. These are unbuffered.

RS423:- A serial RS423 port is provided.

Audio Output:- The output from the sound generator is amplified to a speaker and provided at a phono style connector. Sound transfer to and from the modem is provided.

Modem:- Connection for a modem with both dial pulse and dual tone multi-frequency dialling is provided. This facility is provided to support third party hardware.

5.2 Core machine

Operation of the RAM and ROM is controlled by the Memory Controller integrated circuit. The principal function of this device is to control the memory paging structure.

Memory Map

The 65C12 can directly address 64K locations. As over 1/2 Mbyte may be resident (depending on the users configuration), a paging scheme is implemented to allow access to it.

The basic memory assignment is as follows:

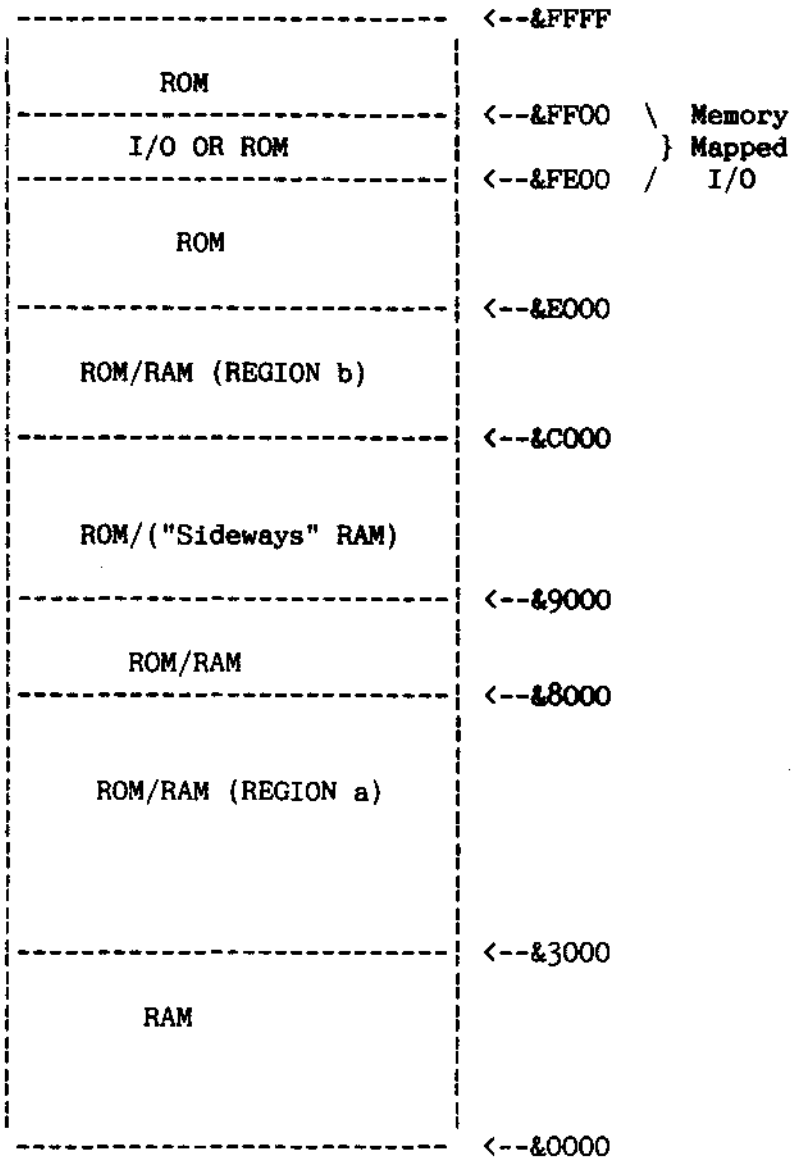


Figure 1

The current memory map is dictated by the contents of the two latches, ROM SELect and ACCess CONtrol located at &FE30 and &FE34 respectively.

The contents of these two latches are as follows:-

	d7	d6	d5	d4	d3	d2	dl	d0
(&FE30)	RAM	0	0	0	PM3	PM2	PM1	PM0
(&FE34)	IRR	TST	IFJ	ITU	Y	X	E	D

The contents of ROMSEL dictate the selection of memory which resides from &8000 to &BFFF.

ACCCON

The contents of ACCCON principally dictate the activity of two regions of memory:

(a) &3000 to &7FFF
(b) &C000 to &DFFF

128 Kbyte RAM

The RAM is functionally split up into two regions: The main region supports the language workspaces, buffers etc. and provides the bit mapped screen. The second region provides four, 16K "Sideways" RAM segments. These are link selected into ROM locations 4,5,6 and 7. They may be deselected, reinstating the ROM sockets in "chunks" of 32 Kbyte.

Within the main 64 Kbyte region, the lower 32K is used within the &0000 to &7FFF region of the CPU memory map, as shown in figure 1.

The upper 32K is split up into three, self-contiguous regions. The largest portion of this is a 20 Kbyte region designated LYNNE. This can be overlayed on the region (a) of main memory.

* When bit D in ACCCON is set, the CRT controller will display the contents of LYNNE. When bit D is cleared, the region (a) of main memory will be displayed.

* When bit E in ACCCON is set, if the address range is &3000 to &7FFF the CPU will read/write Lynne according to the flow shown in figure 2.

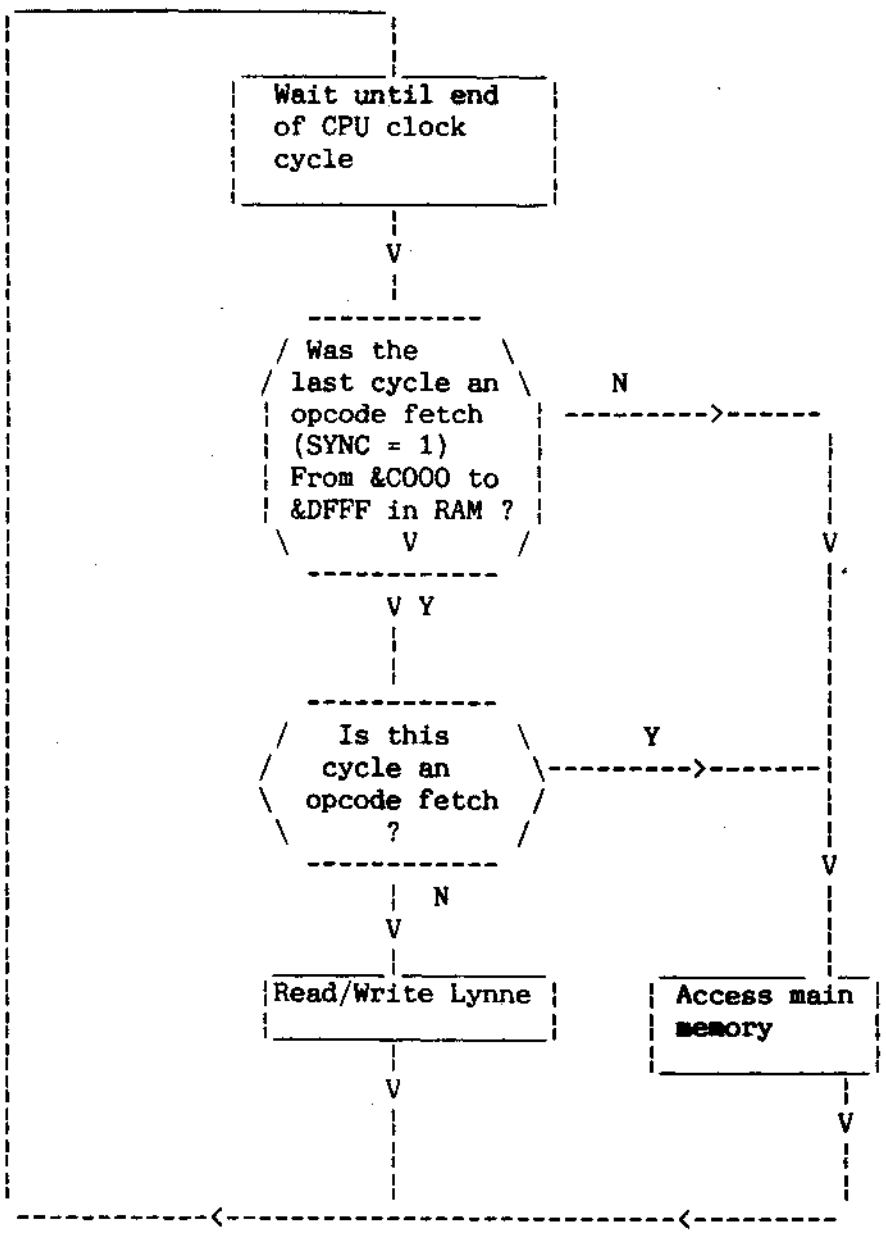


Figure 2

This system allows for the screen bit map to be removed from the main CPU memory map, of which it occupies a significant proportion. It will, however, only work if the screen is being accessed by opcodes from a known region - i.e. the MOS VDU drivers. A mechanism is also provided to permit 'illegal' screen access:

* Bit X in ACCCON, when set, causes all accesses to region (a) to be re-directed to LYNNE. This occurs irrespective of the opcode address, hence considerable care will have to be exercised in its use. When cleared, the memory map returns to its usual format.

In the same way that the BASIC variable HIMEM will always have the value &8000 when LYNNE is used, it is desirable for the variable PAGE to have the value &E00, irrespective of the current filing system.

This is achieved by providing a filing system workspace as follows:-
* Bit Y in ACCCON when set, causes 8 Kbyte of RAM referred to as HAZEL to be overlayed on the MOS VDU drivers, i.e. from &C000 to &DFFF.

Clearly, when this bit has been set, no calls may be made to the MOS for VDU operation. The code which performs this paging operation is responsible for resetting the Y bit, as no hardware is provided for this purpose.

The remaining bits in ACCCON are used to control various peripheral systems:-

* The bit ITU in ACCCON when set enables the CPU to access the internal second processor rather than the external one.

* The bit IRR in ACCCON is InterRupt Request. When set, this bit causes an open drain output to pull the CPU NIRQ pin down to Vss.

ROMSEL

The contents of ROMSEL determine the paging of memory in the 16K region &8000 to &BFFF. One of sixteen, unique 16 Kbyte ROM memory segments may be selected. One additional 4 Kbyte RAM segment may be selected from &8000 to &8FFF.

Eight of the segments are assumed to be in four, 32 Kbyte ROMs where the least significant bit of ROMSEL selects between the upper and lower segments. Seven of the segments exist together with a ROM which is active from &C000 to &FFFF, within a 128 Kbyte ROM. This ROM is connected via a separate data bus. The four, 32 Kbyte devices and one, 16 Kbyte device are connected in a matrixing scheme as shown in figure 3.

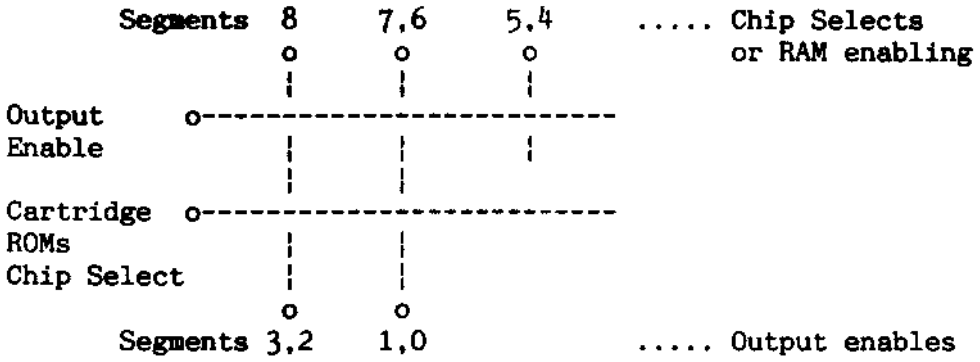


Figure 3

In this way, fewer connections to the controller logic are required to select agiven ROM, although the power dissipation will be increased if all the ROMs in one column are inserted.

A chip select will be driven low if an access to one of the segments (4 to 8) is required. If a cartridge ROM is required, then the Cartridge ROM chip select will be driven high. All chip selects are a decode of the CPU address most significant nibble.

An output enable is turned active low during the CPU phi2 period depending on which segment is required.

The segment to be selected is determined by the binary number held within the least significant nibble of ROMSEL.

Overlaid RAM in ROM area

When the bit RAM is set in ROMSEL, accesses to the region &8000 to &8FFF are redirected from the currently selected ROM to a region of RAM referred to as ANDY. It is the responsibility of the code which set RAM to clear it after accessing ANDY. This is necessary to ensure correct operation of software in ROM.

Summary of RAM memory map

The 64K of DRAM is distributed as follows:-

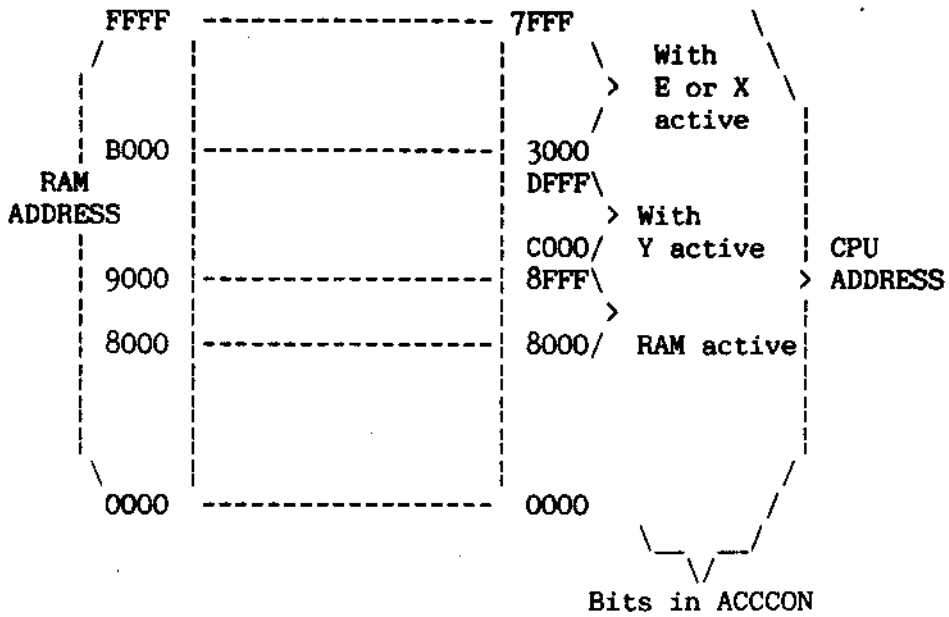


Figure 4

A further 64 Kbyte of RAM is available as four pages of 16 Kbyte from &8000 to &BFFF. The ROM slots 4,5,6 and 7 are not active when this RAM is link selected to be active.

5.3 Internal I/O

Slow peripherals:- These are subsystems which are provided with data from port A of the system VIA. This data is stable until next programmed by the CPU.

Keyboard

General description:- 93 keys are provided. 92 of these are in a modified 8 x 13 matrix as shown in figure 5. A keyboard encoder, IC16 is used to scan the keyboard. During idle (free run) mode, pressing any key will cause an IRQ to be generated via the system 6522. A connection is provided from IC16 to a 6522 'CA' type connection. Hence the interrupts thus generated are controlled by the 6522 control register. Depression of either of the shift keys, or the control key does not cause an interrupt to occur.

Keys are arranged as a QWERTY style keyboard with extra keys for a numeric keypad. Ten additional 'function keys' together with cursor control buttons, etc., are provided.

The "BREAK" key will reset the CPU and abort any access to the clock/RAM chip. To prevent accidental operation, a mechanical lock is provided. This is a plastic cam which is rotated through 90 degrees to stop the keytop from being depressed.

Keyboard Operation:- During free run mode, the keyboard column lines are continually scanned by incrementing a counter, decoding its outputs and pulling low a column line. Any key depressed will cause the interrupt to be generated. A signal, KeyBoard ENable is generated to stop free running mode. The counter contents are now loaded by CPU operation to determine on which row the key was pressed. The rows are then individually selected to determine which key was pressed.

IC16 is supplied with data from the slow data bus:-

PAO to PA6:- These are the slow bus connections. PAO to PA3 are the column select inputs and PA4 to PA6 are the row select inputs. PA7 is a three state connection which is driven active low when a row/column combination describes a depressed key.

RO to R7:- The keyboard row input connections are normally held high by internal pull-up resistors. If a key is depressed it will cause the appropriate row connection to be pulled low when its column is selected.

CO to C14:- These open collector column driving outputs are sequentially taken active low in auto scan mode at a rate of 1MHz. In polled mode (nKBEN active low) the slow bus inputs PAO to PA3 determine which output will be low. The selected column output is a direct decode of these inputs.

CA2:- Connected to the system VIA, this output will cause the VIA to generate an nIRQ. The line will be active low when an active key is detected.

nKBEN:- Generated by the system VIA, this line is taken active low to enable the row and column addresses to be determined by the Operating System.

MHz1:- This is the timing reference.

SWT1, RST0:- These connections are not used. The Keyboard Matrix
The keys are physically arranged as a QERTY type keyboard with 10 function keys, 4 cursor control keys and a 19 key numeric keypad.

The matrix is as follows:-

	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12
R0	ESC	f1	f2	f3	f5	f6	f8	f9	¦	@	4'	5'	2'
R1	TAB	Z	sp	V	B	M	< ,	> .	? /	copy	0'	1'	3'
R2	SHIFT LOCK	S	C	G	H	N	L	+ ;	}]	del	#'	*'	,'
R3	CAPS LOCK	A	X	F	Y	J	K	@	* :	ret	/'	del'	.'
R4	! 1	" 2	D	R	& 6	U	0	P	{ [	@	+'	-'	ret'
R5	f0	W	E	T	' 7	I	) 9	0	£ _	@	8'	9'	
R6	Q	# 3	$ 4	% 5	f4	(8	f7	= -	~ ^	@	6'	7'	
R7	SHIFT	CTRL											

Figure 5

Sound Generator

The sound generator is an SN7694A device. Three sound channels plus one pseudo random noise channel are provided. The full description of it is found in the manufacturers data sheet. It is provided with a reference clock of 4MHz from central timing. The output is filtered as described in the section 'Audio Circuitry'.

The output can also be connected by screened cable to the optional modem. This output is mixed on the modem board to generate dialling tones for DTMF exchanges where the modem hardware does not provide such tones itself.

Real time clock with RAN

Battery back-up

A 146818 RTC and RAM chip is provided with battery backed supply. The chip operation is described in the manufacturers data sheet. In its fully charged state, the internal lithium manganese dioxide battery will provide over one year of back up power. Alternatively, components may be fitted to the circuit board which provide for the fitting of a rechargeable battery on the keyboard. This battery, like its support components are not fitted as standard. If these are fitted by the user, the warranty may be invalidated.

The keyboard mounted battery is charged whilst the computer is running from the mains supply. The proportion of charge accummulated during operation is shown in figure 6 for an initially flat battery. This is an approximation dependent on conditions of use, as the actual charge accumulated will vary with temperature and duty cycle (i.e. ratio of time on charge, to time on discharge).

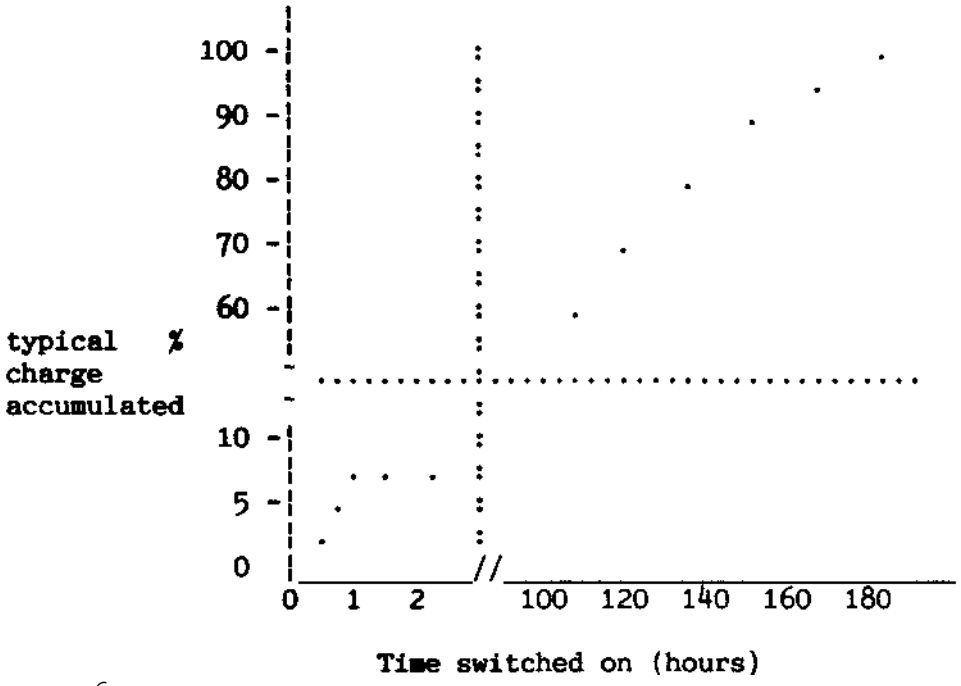


Figure 6

An over-charge prevention circuit is provided with the following action:

a) Upon switch on, charging current of about 30mA is applied.

b) After approximately 15 minutes the charging current falls to 1mA.

c) "Trickle" charging continues at 1mA for as long as mains power is applied.

The minimum charge burst is designed to provide battery back-up over a weekend after just a few minutes operation.

A 10uf capacitor is connected across the clock chip supply connections. This is to prevent loss of data in the event of accidental battery disconnection.

Configuration Status:- Fifty bytes of CMOS RAM are available within the chip. Twenty of these are used by the operating and filing systems for initial configuration of the hardware. Of the remainder, ten are reserved for future use by ACORN, ten are for 'Third Party' use and the remainder are for the user.

Clock:- The clock operates from a 32.768KHz crystal oscillator. A trimming capacitor is provided as is a test point with the buffered clock output. Year, month, day, hour, minute and second information is provided with automatic leap year (but not automatic leap century) correction. An alarm is also included within the chip, but operating system support to this facility is not provided. An optional nIRQ connection can be made to the CPU from the clock chip, enabling the alarm to change program flow. Operation of the clock chip in this manner involves direct manipulation of the chip control signals and should only be attempted by competent programmers. Acorn Computers are not responsible for incorrect programming by the user/software supplier.

If power is removed during an access to this chip, the chip select will become invalid. This cannot however remove the possibility of write accesses being corrupted. This is done by inverting the chip select with a transistor whose collector resistor is connected to the battery backed supply. As power fails to the main circuitry, the transistor base current reduces and the transistor switches off deselecting the chip.

1 MHz Internal I0:- Various devices operate at a 1MHz bus rate. Only one internal I/O component works at this speed - the system VIA.

System VIA:- A 6522 allows several sources to create maskable interrupts. The sources are:-

a) CRTC vertical synchronisation.
b) A-D converter; end of conversion signal.
c) CRTC light pen strobe.
d) Keyboard key detect.

It also provides the previously mentioned slow data bus.

Port B on this device generates and reads a number of internal hardware strobes. These are as follows:-

Port B Data Strobe Active Level

Port B Data D7 D0	Strobe	Active Level
D X X X X X X X	Clock Address	H
X D X X X X X X	Clock chip enable	H
X X D X X X X X	'Fire' button 1	Input
X X X D X X X X	'Fire' button 2	Input
X X X X D 0 0 0	Sound chip select	L
X X X X D 0 0 1	Clock R/W	L
X X X X D 0 1 0	Clock Data	Q
X X X X D 0 1 1	Keyboard enable	Q
X X X X D 1 0 0	C0 } Screen control	L
X X X X D 1 0 1	C1 } Signals	H
X X X X D 1 1 0	Caps Lock indicator	L
X X X X D 1 1 1	Shift Lock indicator	L

Note: Q is the value of D after the port write operation is completed

2MHz Internal I/0:- Only one internal I/O component operates at this speed, the internal second processor TUBE. Its data bus is connected directly to the CPU data bus.

The second processor interface will only be specified as a hardware data transfer definition. In this way, the actual second processor used will not be constrained by this specification.

This is a parallel port providing the following data access signals:-

i) DO to D7 .... A bi-directional bus to TTL levels. ii) AO to A2 .... A uni-directional bus to CMOS levels.

The following control and timing signals are provided:-

i) Host CPU phi2 .... CMOS levels
ii) System Reset .... TTL levels
iii) Host CPU nIRQ .... This must be an 'open collector' node with an active low TTL level
iv) 8MHz timing reference.... TTL levels
v) TUBE chip select .... CMOS levels
vi) Read/Write .... TTL levels

5.4 External I/O

1MHz External I/O:-

Screen Output:- There are two chips primarily responsible for providing the screen output:-

a) 6845
b) Acorn proprietary VIDPROC (IC42)

High Resolution Modes:- The 6845 generates a linear memory address sequence which increments every 0.5 us or lus, depending on the video bandwidth selected and video data format.

The amount of memory reserved for screen use is also varied. The available options are shown in figure 7

Video Data Formats

"Mode"	Format Pixels/Byte	Reserved Memory Bytes	
0	8	20K	
1	4	20K	
2	2	20K	
3	8	16K	
4	8	10K	
5	4	10K	
6	8	8K	
7	Teletext	1K	
128	8	20K \	
129	4	20K ¦	
130	2	20K ¦	Reserved
131	8	20K >	in
132	8	20K ¦	LYNNE
133	4	20K ¦	
134	8	20K ¦	
135	Teletext	20K /	

Figure 7

All modes except 7 and 135 display a bit mapped image of the reserved memory. The 6845 may be re-programmed to display any arbitrary section of memory. If this is done, however, the hardware scrolling will not work correctly, as it assumes that the screen memory is in its usual location.
The screen always ends at &7FFF and starts 1,8,10 or 20K further down than that, depending on the selected mode.

The selection of video bandwidth and data format is performed by programming the VIDPROC. The cursor size and position is also controllable by VIDPROC. Special measures have been taken to ensure correct cursor operation in the Teletext modes.

Teletext

The Teletext modes do not generate a bit mapped display, but a character cell one. The character/graphics ROM within a SAA5050 device generates RGB signals according to the desired character/graphics information within the reserved memory space. Each byte of memory is therefore just a definition of the character/graphics symbol required.

Other SAA505X devices may be used when different languages are required. Only 1 Kbyte of memory is needed for either of the Teletext modes, although 20K is reserved for it in mode 135. The MOS uses the spare 19K to speed up inter-filing system file transfers but the user may use this memory if no such transfers are to be done.

The VIDPROC has to be re-programmed to use the SAA5050 RGB outputs.

The 6845 is still used to generate the cursor. As a delay of 2.75 us will occur after a character is read from RAM, before outputting the appropriate RGB signals, the 6845 has to be programmed accordingly. The "start" of screen signal is given a 1.5 byte-time offset, and the SAA5050 has a further 1 byte-time offset to restore the correct cursor/data phase.

The VIDPROC has further adjustment which allows for the cursor to be adjusted to pixel accuracy.

Hardware Scroll:- Scrolling may be achieved in any mode by re-programming the 6845 start of screen address to an integral number of video lines further down the memory map than the nominal start of screen.

This of course causes the linear address generator to attempt to display an end of screen which is out of the reserved video area. To overcome this effect, hardware scrolling is provided with a variable address wrap-around.

In effect, when the address generator would otherwise attempt to access out-of-screen RAM, its addresses are modified to point to the gap between the original start of screen and scrolled start of screen. When this is done, only the end of screen needs to be written over in RAM. (If this is not done, the entire screen appears to "roll-over"). The amount of modification to be used is controlled by two nodes; C0 and C1.

Video Output:- Three outputs are provided for displaying video data. These are:
a) PAL/NTSC encoded, UHF carrier. On channel 36 with 1.5mV into 75 ohm.

b) Composite video. This is a iv peak to peak signal.

c) Digital Red, Green, Blue outputs. These are approximately 75 ohm outputs.

For use with NTSC, the modulator has to be changed from UM1233/E36 to a VHF equivalent. Provision is made for selection of either one of two channels with V.H.F. A Molex type link has to be inserted for this.

Analogue Port:- This 15 way D-type connector provides access to an NEC uPD7002, 4 channel, 10 bit analogue to digital converter. The sampled input is compared to a 1.8V reference derived from three small signal diodes in series.

A tracked link may be cut to deselect this reference. The user may then solder in a two pin precision reference in the holes provided or supply an external reference. Any user supplied reference should have a maximum voltage of 2.5V.

Conversion:- An input voltage on any one of the 4 channels wil be digitised when the A/D control register is so instructed. Conversions are in the range 0 to 1.8V.

The voltage reference is made available at the connector. Provision is made on the board for an additional high stability reference, if required.

A link will have to be made for the additionl reference to be used. Conversions take place in 5mS and the "end of conversion" pulse causes an IRQ to be generated by the system VIA.

Auxiliary Connections:- Two "fire buttons" are provided for with the connections IO, These are connected to the system VIA and cause interrupts (as IRQ) to be generated.

A light pen may be connected to the signal LPSTB. This also causes the system VIA to generate an IRQ (if enabled). It also causes the 6845 CRTC to latch the address of the currently selected video data byte. This may not be the same as the displayed byte, and some software correction may be necessary. Factors such as phosphor characteristics, light pen response and the angle at which the pen is used, may all affect the correction needed.

Serial Ports - Cassette and RS423:- Much circuitry used to provide the RS423 port also generates cassette interface signals. For this reason, these will be described together, with the differences where appropriate.

U.A.R.T.:- The device responsible for providing most of the serial port functions is the 6850 UART. This has all the receive/transmit and data formatting/error checking that is neccessary for both systems.It is fully described in the March 1983 edition of the Hitachi Microcomputer Databook.

SERPROC:- The ACORN proprietary part, the SERPROC is effectively a multiplexer and baud rate generator for the 6850. It also generates the phase-continuous transmission circuitry for use with the cassette interface.

Buffer Components:- The RS423 transmit data and CTS lines are buffered by an AM26LS30, or equivalent. This provides a single ended transmission with slew rate limited output.

RS423 receive data and RTS is buffered by a uA9637AC or equivalent. Both buffers are connected with single ended input configurations.

Cassette data output from the SERPROC is buffered by a single, non-inverting operational amplifier with a simple, single pole filter; a. c. coupling capacitor and current limiting output resistor.

2MHz External I/O

Two peripheral devices operate at 2MHz. These are the external second processor connection and the ECONET connection.

ECONET Module:- Connection is made to the ECONET by a five way DIN connector mounted on the main circuit board. The interface electronics including the 681354. line drivers, receivers and chatter disconnect components are mounted on a separate circuit board. This board has two connectors:-

a) A 5 way connector which has a one-to-one connection with the DIN connector.

b) A 15 way connector provides the CPU data bus together with address, timing reference, chip select and interrupt signals. The main pcb has two further address connections for future expansion.

External Second Processor:- This interface has a buffered data bus via the Peripheral Bus Controller (PBC). The EXbus on this component provides for good data set up and hold times. Together with a limited degree of line matching, this ensures reliable high speed data transfer with unspecified cable lengths. A maximum cable length of one metre is suggested to prevent noise problems.

The interface operates at 2Mhz. This means that if a 1Mhz bus peripheral is also connected, then the address and data buses on this connector will appear to perform both 1 and 2MHz cycles.

The connections are:-

DO to D7	Data Bus	CMOS levels
AO to A7	Address Bus	TTL levels
IRQ	Interrupt Request	Open collector TTL levels
nTUBE	Parasite chip select	TTL levels
Supply		+5V
Ground		OV

6 Test equipment

A PORT tester is available for the microcomputer. It will check the DRAMs (including siueways RAM), CMOS RAM, and all the I/O ports on the microcomputer: disc, printer, user, 1MHz bus, TUBE, UHF, video, ROB, RS423, cassette, A to D, and sound output. To use this tester, the microcomputer must at least have the CPU running and the MOS/BASIC ROM working and some of the RAM working.

The PORT test software is contained in a cartridge ROM and on disc. Full operating instructions are supplied with the equipment.

7 Fault finding

This section goes step by step through fault finding in each section of hardware. It should be studied in conjunction with the circuit diagram and component location tables in the Appendix.

If any part of the machine is suspected of being faulty, the following points should always be checked first:

1 no loose connectors and broken cables

2 no broken or shorting tracks

3 ICs plugged into their sockets correctly

4 power supply working and reaching the components concerned

5 all digital signals are either at clean TTL logic levels (greater than 2.4V for 1, less than .5V for 0), or clean CMOS logic levels (greater than 3V for 1, less than 1V for 0). On timed signals this must be true for the period 150ns before phi2 on read cycles and 300ns before phi2 on write cycles.

Hints for repair:

1 Never solder to a computer which is switched on.

2 Remove all user ROMs before starting (Remember to put them back afterwards !)

3 Use sharp pointed meter probes to push through solder resist. This will make finding short/open circuits more reliable.

4 Always suspect connectors.

5 If you find a recurrent fault (e.g. more than 10 machines), let us know at ACORN so that we can include it in this manual if appropriate.

The following items of test equipment are required for fault finding:
A set of screwdrivers Pliers
Cutters

10A Multimeter

RGB monitor

logic probe
5 ohm 5W resistor

The repair will be quicker with:

100MHz dual beam oscilloscope

Good quality scope probes

TV, composite monitor, colour monitor

cassette player

disc drive
PORT tester

frequency counter

A known good computer to use as a signal model

Note: the Peripheral Bus Controller IC21 is used to buffer the data bus around the system. It also isolates may parts of the system from each other to help improve reliability. It may disguise data bus failures or open circuits. Be sure not to assume that any node is connected to any other unless you have checked it. This particularly applies to the SAA5050 and all 1MHz operating components. E.g. the User VIA going down could stop the System VIA.

7.1 Switch on

If the suspect microcomputer has a second or co-processor fitted then disconnect it. Connect the suspect microcomputer to a UHF TV and an RGB monitor (connecting both a TV and a monitor will show up any fault in the connecting leads, or the polarity of CSYNC). Connect the mains supply and switch on both the monitors and the computer. One of the following will happen.

7.1.1 There is noise on the monitor screens (no signal from computer). There is no power-on beep sound and the keyboard power indicator does not light.

Results: the power supply is dead.

Follow the sequence of checks shown below.

1 Check the power supply (see 7.2). Try replacing the power supply anyway as the fuse may have blown.

7.1.2 The power supply is working (the keyboard indicator is lit), but nothing else happens.

Results: There is a board fault.

Follow the sequence of checks shown below.

1 Check that all ICs have power and ground on the correct pins at the correct voltage. Make good any dry joints.

2 Feel whether any of the ICs are hot. Check for shorted PCB tracks. Watch for shorts from -5V to the IO controller causing it to latch-up. Clear shorted tracks and then replace any affected ICs.

Note: ICs which get abnormally hot due to a fault, but which work after the fault has been cured, should still be replaced. Their long term reliablility may well be impaired.

3 Check the 16MHz oscillator output IC43 pin 2, and check that it is reaching the VIDPROC IC42 pin 8. The signal should be reasonably clean, 4V peak to peak. If not then check the crystal controlled oscillator circuit formed by half of IC43 and X2.

Warning: if the system 16MHz clock does not work, the DRAM RAS and CAS lines could be held low. This can make the ICs heat up causing permanent damage. If the oscillator is not working, or the clock is not reaching the VIDPROC, try to find the fault and repair it as quickly as possible. Do not leave the computer switched on for more than 30 seconds at a time.

4 Check the 1 2 4 and 8 MHz signals from the VIDPROC, IC42 pins 4 5 6 and 7 respectively. If any is missing, or is not a clean square wave with MI logic levels then replace the VIDPROC 1C42.

5 Check that there is a clean 2 MHz signal on the CPU clock input, IC14 pin 37. If it is missing or incorrect then check for broken or shorting track.

6 Check that all data and address bus lines are clear of shorts between themselves, +5V and ground.

7 Check that the system ROM is plugged in.

8 Check the RAS and CAS signals to the main DRAMs, ICs 17 and 23, pin 5 (RAS) and pin 16 (CAS).

The main DRAM timing is shown in figure 8.

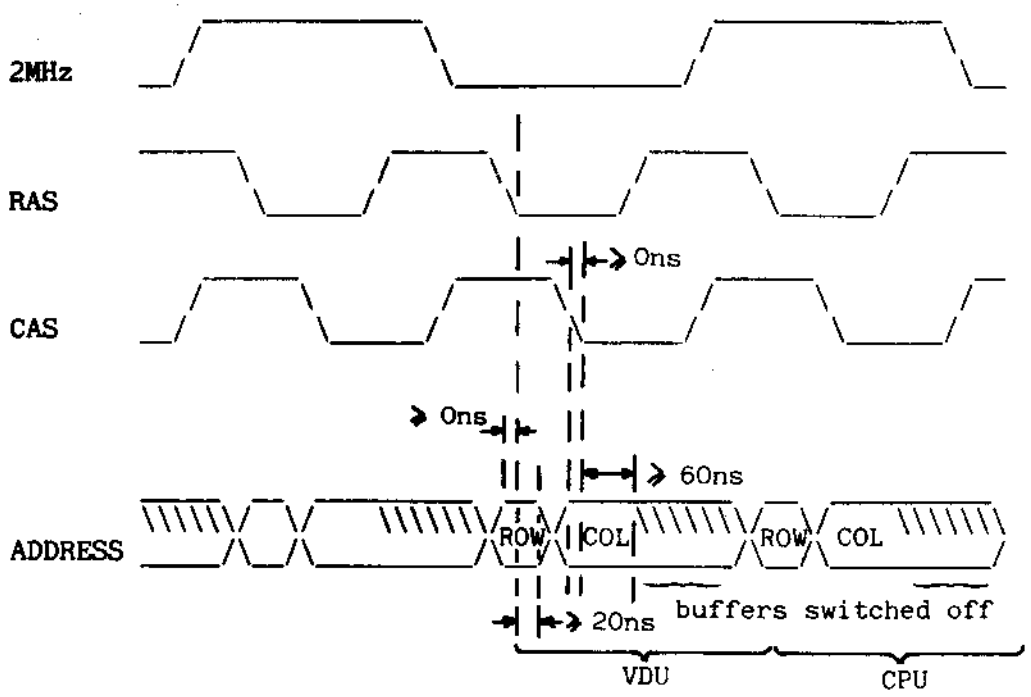


Figure 8 DRAM timing

RAS and CAS should be good 4MHz square waves. If one or both is missing then check for shorted tracks. Remember the DRAMs can be destroyed if RAS is stuck low.

RAS is generated from 4M and 8M by the D-type IC28 pin 9.

CAS for the main DRAMs is generated from 2M, inverted by a NAND in IC34 to give phi2 IN, gated with DRAMEN which enables the main RAM, and finally gated with 4M through another NAND in IC34.

9 Check that the auxiliary DRAM CAS line, when inverted at IC36 pin 8 is low. If it is high at this point then it will suppress the main DRAMs.

10 Check the multiplexed address lines into the main DRAMs, ICs 17 and 23 pins 6 7 8 10 11 12 13 and 14. The address lines should switch after RAS, with an approximate 20ns hold time as shown in figure 8.

Also check that the address lines are correctly switching after phi2, as shown in figure 8.

If any of the DRAM timing is found to be out of specification then check that C26 is fitted and is the correct value.

7.1.3 There is a sort of display with rolling lines and/or diagonal stripes.

1 Check the MA and RA lines from the 6845 CRTC IC22. There are 14 MA lines from MA0 (pin 4) to MA13 (pin 17) inclusive. There are 4 RA lines from RA0 (pin 38) to RA3 (pin 35) inclusive (RA4 is not connected).

These lines form the video RAM addresses in the various screen modes. Check that they are not stuck, and that they oscillate between good logic 0 and logic 1 voltage levels. If not then first replace the 6845, then look for shorted tracks.

Check that all are getting through to the CRTC/MUX IC31.

2 Check VSYNC pin 40 IC22. This line should pulse low every 20ms.

3 Check HSYNC pin 39 IC22. This line should pulse low every 64us.

4 Check that CSYNC (both HSYNC and VSYNC superimposed) is available at IC25 pin 8 and also at pin 4 of SK9, the RGB connector.

5 If the RGB display alone is not working then the CSYNC polarity for that particular monitor is probably incorrect. Alter LK5.

6 Check all video connections.

7.1.4 There is a cursor stuck at the top left corner of the screen, but nothing else.

1 Disconnect any second or co-processor which may be fitted.

2 Check all connections to and from the keyboard and keyboard encoder IC16. Replace IC16.

7.1.5 The screen says

AC0RN MOS

ACORN ADFS

but nothing else.

1 Disconnect any second or co-processor which may be fitted.

2 Try typing CTRL F BREAK. If this works then either connect up a disc drive and put an ADFS disc in it or type

*configure nodir RETURN

Turn the power on and off. The machine should now work.

3 The configuration memory may have been set incorrectly or is faulty. Turn the power off and on again whilst holding down the R key. Then press CTRL F BREAK. All previous configuration commands will be reset to zero.

7.1.6 BASIC is printed on the screen, but no > prompt appears.

1 Disconnect any second or co-processor which may be fitted.

2 Check that the IRQ line on the CPU IC14 pin 4 is not stuck in one logic state. If it is then check the address and chip select lines of the system VIA IC8.

7.1.7 The BASIC prompt > appears, but the keyboard does not respond.

1 Check the address and ship select lines of the system VIA IC8.

2 Check all connections to the keyboard encoder IC16.

3 If all else fails then try a different keyboard. If this works, look for broken leads and tracks on the original one.

4 Check that the IRQ line IC14 pin 4 is not stuck low or high. The memory controller IC20 and CMOS clock/RAM IC11 both have direct connections to the IRQ line. The latter part has a link LK4 which can be used to isolate it from IRQ.

Note: the system VIA IC8 generates an interrupt every 100th of a second. If this interrupt is not cleared by the operating system each time it occurs the IRQ line will appear to be stuck low. This could occur if some other installed software is faulty or if an address or data line to the VIA is faulty.

7.1.8 Not all keys work on the keyboard.

One of two possible keyboard circuits may be fitted:

a) A 40 pin keyboard encoder IC16 on the main circuit board and two 15 way connectors (possibly with an intermediate buffer board) joined to the keyboard with ribbon cables.

1 If more than one key is affected, check for a faulty connection from the keyboard encoder IC16 to the keyboard.

2 If more than one key is affected, check for a broken track in the middle of a row or column of the keyboard matrix.

3 If one key only is affected, check for a broken track at the end of a row or column in the keyboard matrix.

4 If one key only is affected then check the keyswitch itself.

Note: the beginning of a row or column is the end of a PCB track which is immediately connected to the encoder circuitry. The end of a row or column is the other end of the PCB track. Because of the layout, the beginning and end of a track are not necessarily the parts of the track which are visually nearer or farther from the encoder circuitry.

b) A 17 way connector rising to a keyboard with the encoder circuitry on it.

1 All of 1 to 4 in the previous section.

2 Check for a faulty connection from the main board to the keyboard which may cause the entire keyboard to be affected.

7.1.9 All the keys are working, but CTRL BREAK behaves as BREAK. (CTRL BREAK should invoke the configuration settings.)

1 Check that all power-down components around the CM0S clock/RAM chip IC11 are present and have the correct value.

On some early computers, C11 needs to be 100uF instead of 10uF, D8 should be changed to IN4001, and Q3 should have a 1k8 resistor between its base and emitter.

2 Check that the chip enable pin 13 of IC11 is normally high with just occasional excursions low. If not then check the system VIA IC8 for the RTC chip select pulses which should be on pin 16.

3 Real time clock chip control lines should be in the following state at all times when not being accessed by the user.

CE IC11 pin 13 high
AS IC11 pin 14 low
DS IC11 pin 17 low

4 Check that R/W IC11 pin 15 wiggles when alternate reads and writes are performed.

7.1.10 The computer powers up in terminal mode, and *configure will not change it.

1 Check 1 and 2 in the section above.

2 Check all connections to the clock/RAM chip IC11 for open circuits or short circuits.

7.1.11 The computer works, but random dots or characters appear on the screen.

1 Type a short program or piece of text into the machine - about two lines in any screen mode are adequate. Leave it for a few minutes and then see if the screen has been corrupted. If it has then there is a memory system fault. If it hasn't then enter a longer piece of program or text - enough to fill a screen and repeat the test.

Any fault showing itself will be due to a memory system failure. These are rarely due to the RAM chips themselves as these are usually very reliable. Check the following very carefully.

2 Check all connections from the CPU address bus (IC14 pins 9 to 20 and pins 22 to 25 inclusive) to the DRAM address multiplexers (ICs 29 30 and 33, see circuit diagram for pin numbers). Then check the voltage levels of these signals at the multiplexer input pins. All signals should have good CMOS levels (less than 1V for 0, greater than 3V for 1). A constant 0 or 5V level implies a short to the relevant power rail. Poor logic levels imply shorting to another logic signal.

3 Check that the address at the DRAM inputs is stable for at least 15ns after RAS goes low and changes no later than 50ns after that edge, see figure 8. This should occur once for every active high period of the system 2MHz clock out of the VIDPROC and once for every active low period.

4 Check that the noise around logic LOW signals is generally less than 500mV. If it is not, then some signals may be shorting or a decoupling capacitor may be missing.

5 Check that the data bus is properly connected between the CPU and the DRAMs.

7.1.12 You can type but get two or more copies around the screen.

1 Check Test Points TP7 to TP20 (the CRTC scanning outputs, shown on circuit diagram to the left of the CRTC IC22) to make sure that the correct addresses are being generated. Any line stuck high or low or shorting to another pin will give strange screen effects.
Note: MA13 IC22 pin 17 is used to switch the address multiplexing circuits between modes 7/135 and any other modes. This line should be static in any given mode.

2 Check that all of the lines from the CRTC IC22 to the CRTC Multiplexer IC31 actually get there.

3 Check that the lines CO and Cl from the 74LS259 (IC10 pins 4 and 5) to the CRTC Multiplexer (IC31 pins 38 and 39) are properly connected and change at least once if you switch between modes.

4 Check that the lines from the CRTC/MUX IC31 to the DRAMs are correct with no short or open circuits.

7.2 Sideways RAM

1 Check all connections to the memory address multiplexers.

2 Check RAS and CAS at the DRAMs, see figure 8.

3 Check that the two links LK18 and LK19 are in the correct position for your use.

7.3 Video

To debug the video, all three different types of monitor should be connected: TV, ROB and composite.

7.3.1 The display scrolls vertically round the screen. Does it occur on RGB, UHF and Composite video?

1 If so, check VSYNC is correct on the CRTC IC22 pin 40.

2 Then follow the signal through the exclusive-OR gates IC25 where it is combined with HSYNC. If the signal does not make good logic levels at any node, then there is probably a short in that area.
Note: when VSYNC (period 20ms) is EXORed with HSYNC (period 64us), the former will be difficult to spot within the latter. A way of getting round this is to synchronise the oscilloscope from the VYSNC output of the CRTC IC22 pin 40 and then examine the EXOR gate output.

Does it only occur on one of the video outputs?

1 Is the CSYNC polarity link LK5 correct for your monitor?

2 If it only occurs on composite video, check that all the resistors (R147 to R150 inclusive) to the output transistors are correct in accordance with the circuit diagram. Do they all have good signals going into them?

3 If it only occurs on UHF, check the signal as it passes through the resistor network, IC40 pins 12 to 19 inclusive through resistors R69 75 77 78 84 85 87 and 89.

4 If it only occurs on RGB, check all the signals going to the back of the connector.

7.3.2 The display is correct vertically, but is broken into moving diagonal lines.

Does it occur on RGB, UHF and Composite video?

1 If so, check HSYNC is correct on the CRTC IC22 pin 39.

2 Then follow the signal through the exclusive-OR gates IC25 where it is combined with VSYNC. If the signal does not make good logic levels at any node, then there is probably a short in that area.
Note: when HSYNC (period 64us) is EXORed with VSYNC (period 20ms), the former will have the latter superimposed upon it. This will make the former appear to have glitches. This should be ignored in the measurement of HSYNC period.

Does it only occur on one of the video outputs?
1 Is the CSYNC polarity link LK5 correct for your monitor?

2 If it only occurs on composite video, check that all the resistors (R147 to R150 inclusive) to the output transistors are correct in accordance with the circuit diagram. Do they all have good signals going into them?

3) If it only occurs on UHF, check the signal as it passes through the resistor network, IC40 pins 12 to 19 inclusive through resistors R69 75 77 78 84 85 87 and 89.

7.3.3 There is no colour on UHF.

1 Is the variable capacitor VC2 set to give the correct frequency of 17.7345MHz at IC43 pin 12?

2 Check connection to IC40 pin 11, and resistor summing node through Li and C81 Q12 c88 and R140.

3 Check +5V supply on IC40 pin 20.

4 Try replacing IC40 as a last resort.

7.3.4 There is only one colour.

On RGB

1 Check the RGB connections out of the VIDPROC IC42 pins 14 12 and 10.

2 If the fault is only in mode 7 or 135 then check RGB connections from SAA5050 IC32 pins 24 23 and 22 to the VIDPROC IC42 pins 13 11 and 9.

On UHF

1 Check RGB inputs to IC40 pins 6 7 and 8. If there are any faults, check the connections from the VIDPROC IC42 pins 14 12 and 10. If any nodes are stuck at +5V or ground then check for shorts. As a last resort, try changing chips.

2 Check resistors R69 75 77 78 84 85 87 89 90 for the correct values and that they have good signal levels at their IC40 ends.

7.3.5 The screen displays the wrong colours.

1 Check 1 and 2 above.

7.3.6 The display works in all modes except 7 and 135.

These modes work very differently from the others, using the SAA5050. There are a number of faults which only exhibit themselves in these modes.

1 There is a cursor which can be moved, but no text. Check the 6MHz input to the SAA5050. It will have a slightly variable duty cycle, certainly not 50%, but no part of the waveform should be narrower than about 40ns. If so, check all components and signals around the 6MHz generator IC39 and 1C25.

2 The text is at all fragmented. Check as above.

3 Not all colours are present. Check all connections to the VIDPR0C 1C42. Are the pull-up resistors R51 R54 and R56 present and the correct values?

4 Not all characters can be obtained. Check all data bus connections the the PBC IC21 pins 21 to 28.

5 Lines of normal size text appear cut in half. Check VSYNC at the CRTC IC22 pin 40.

6 Rounded characters appear unstable. Check the components and signals around the 6MHz generator 1C39 and 1C25.

7) Lines are broken up. Check all connections to the PBC
IC21. 7.4 Real time clock
7.4.1 Gives strange characters.

1 Type in the correct time and try again.

7.4.2 Does not increment.

1 Check that the variable capacitor VC1 is in the circuit. Check that 32.768 KHz is at IC11 pin 2. If it is not, check all the values in the oscillator circuit X1 VC1 C6 C7 R17 and R24.

2 Are all connections to the system VIA correct?

3 Are all the components in the chip select/power-down circuit fitted correctly ? See 7.1.9.

7.4.3 Loses a lot of time.

1 Is the battery connector PL8 securely fitted with all three pins engaged? Are the battery leads properly soldered to the battery clips?

2 Is the battery flat? If it is then replace it in its holder next to the speaker inside the computer, being careful to insert the new battery with the same polarity as the old one.

3 Is there at least 2.6V at the clock chip with mains power switched off?

If not the battery may still be flat, but check the FET Q4 and surrounding components first.

7.5 Analogue port

7.5.1 Gives completely erroneous results on all channels.

1 Are all the connections on the external plug correct?

2 Has it got an incorrect or faulty integration capacitor C49?

3 Check that the reference voltage is approximately 1.8V across pins 8 and 9 of IC49 and has very little noise on it.

4 Are all the address and data bus connections to IC49 correct?

5 Are the input voltages within the range 0 to 2.5V? If not, the converter will not work correctly.

6 Have any of the terminals in the connector been connected to voltages greater than 5.5V or less than 0.5V? If so the A/D converter is likely to be damaged. Replace IC49.

7 Is the chip select from the 10 controller IC15 pin 35 correctly connected to IC49 pin 23?

8 Does IC49 have a 1MHz timing reference on pin 2?

7.5.2 Gives erroneous results on just one channel.

1 The plug and cable connections are the most likely sources of problems.

Point 6 above may also apply.

7.6 RS423 port

7.6.1 Does not work at all.

1 Are the data format and baud rate settings the same as the remote computer?

Note: these will be set to the configuration values after power on or CTRL BREAK. Make sure that these are correct as well.

2 Is the cable properly connected?

Note: this connector CAN be inserted the wrong way up!

3 Are all the cable connections correct, i.e. no open/short circuits?

4 Are the device select connections to the SERPR0C and ACIA from the I0 controller correct (IC15 pin 34 and pin 36 respectively), with no short circuits to either power supply rail?

5 Is the SERPR0C getting a 1.23MHz timing reference, IC48

pin25? This signal could come from either one of two

sources -

a) A 74LS169 counter.
b) The chroma chip.

Whichever it SH0ULD come from is dependent on the build standard of the computer. In any case, the SERPROC should get this signal from some source. Check that it is the correct frequency.

6 Is the -5V supply correctly connected (and working) to the RS423 transmitter chip IC50 pin 8?

7 Are either CTS (IC48 pin 20) or RTS (IC48 pin 23) stuck high or low?

8 If all else fails, check all remaining connections to the ACIA and SERPROC.

7.6.2 Will only receive data.

1 Does the remote computer use different transmit and receive rates? If so check that your computer has the equivalent receive and transmit respectively.

2 Check 3 6 and 7 as above.

3 Check that data going into the line driver IC50 comes out of it. The driver could be faulty otherwise.

4 Check that the Tx CLK going into the ACIA is correct, IC45

pin 4. 7.6.3 Will only transmit data.

1 Does the remote computer use different transmit and receive rates? If so check that your computer has the equivalent receive and transmit respectively.

2 Check 3 6 and 7 as above.

3 Check that data going into the line receiver IC51 comes out of it.

4 Check that the Rx CLK going into the ACIA is correct, 1C45

pin 3. 7.7 Cassette interface

7.7.1 Will not load or save data.

1 Check the cable and data recorder (with another computer if possible).

2 Check that the ACIA and SERPR0C have correct (i.e. no open or short circuit) connections on all pins.

3 Check that the back panel connector has no dry joints or short circuits between it and the interface circuitry.

4 Are the connector pins in good condition? If not, the fault could show itself as intermittent operation.

5 Check the 1.23MHz connection to the ACIA.

7.7.2 Will not load data.

1 Check 1 3 and 4 above.

2 Check that the ACIA is receiving an Rx CLK, IC45 pin 3.

2 Check the connections between the SERPR0C IC48 and ACIA IC45.

3 Check that incoming data is appearing at the pin at the back of the connector.

4 Follow the signal path through the high and low pass filters. It should finish up as a 1.2V peak to peak signal at the CASIN input to the SERPROC, IC48 pin 12. If it disappears at any point there is probably a dry joint.

5 The cassette data input has a static protection network on it. Check that all the components in this are fitted and have the correct values. A faulty component could mean that the LM324 has been subsequently damaged.

6 Check that the ACIA and SERPR0C have correct (i.e. no open or short circuit) connections on all pins.

7 Check the 1.23MHz connection to the ACIA.

8 As a last resort, change the SERPR0C and try again, then try the ACIA. This should not be necessary as both of these components are very reliable.

7.7.3 Will not save data.

1 Check the cable and data recorder (with another computer if possible).

2 Check that the ACIA is getting a Tx CLK, IC45 pin 4.

3 Check the connections between the SERPR0C and ACIA.

4 Check that the back panel connector has no dry joints or short circuits between it and the interface circuitry.

5 Are the connector pins in good condition? If not, the fault could show itself as intermittent operation.

6 Check that data is coming out of the CAS0UT output from the SERPROC, IC48 pin 27. If not, check all the data and address connections to the SERPR0C and ACIA.

7 Follow the signal (if it exists) from the SERPR0C to the connector. If it disappears then a dry joint or short to power or ground is likely.

7.8 Disc drive interface

7.8.1 Refuses to work at all.

1 Check that both the signal connector and power connector are securely pushed home.

2 Try another disc drive if possible, to eliminate the chance of a fault in this.

3 Try the disc drive with another computer, if possible.

4 Check that the 1770/1772 and 74LS174 have valid logic 0 levels at their device select inputs (IC3 pin 1 and IC4 pin 1) and that all data and address bus connections are present, with no open or short circuits. If either IC is not being selected then check the outputs on the IO controller, IC15 pin 1 (FDCON) and pin 4 (FDC). If these signals are not available then check that the disc software is fitted and is selected.

7.8.2 The drive select light comes on. You cannot read a catalogue.

1 Has the correct filing system for the disc been selected (i.e. ADFS or DFS)?

2 Is the disc formatted?

3 Is the disc in the right way round?

4 Is the Read Data input to the 1770/1772 (IC3 pin 19) wiggling when you attempt to read the disc? If not then check the signal cable and if necessary check that data is getting onto it from the disc drive.

5 Are the pull-up resistors (R1 R3 R5 and R6) on the 1770/1772 disc inputs fitted and correct?

6 Is the 8MHz input to the 1770/1772 correct? Check that it is available at IC3 pin 18. If not then trace it back to IC19 pin 4 and IC42 pin 7.

7 Is the 1770/1772 DRQ line (IC3 pin 27) normally low but going high once every 32us (when then disc interface has been asked to read, say, a catalogue)? If not then check that this line is not shorted to power or ground and is connected to the IO Controller (IC15 pin 5).

8 Check that the DRQ transitions (IC3 pin 27) appear logically inverted at the NMI pin on the CPU (IC14 pin 6).

9 Check that the 1770/1772 INTRQ output (IC3 pin 28) produces a high going pulse at the end of every command issued to the 1770/1772. If the INTRQ line is shorted high it will cause the IO Controller to hold the CPU NMI line low, thus masking DRQ transitions.

7.8.3 The catalogue can be read, but the entries are corrupted.

1 Some computers have 220 pF capacitor C27 fitted from the DRQ line to ground. Is this fitted? Is its value correct? There will be no place on the PCB for computers that do not need this capacitor.

2 Are one or two disc drives present? If two, make sure that only one of them has line termination resistors in.

7.8.4 The catalogue can be read, but not the data (or the directory cannot be changed in ADFS).

1 (Issue 1 boards only). There should be a small capacitor from the DRQ line to ground. Is this fitted? Is its value correct?

2 Are one or two disc drives present? If two, make sure that only one of them has line termination resistors in.

7.8.5 Data can be read but it is wrong (or you get Bad FS map in ADFS).

1 Try the disc drive in another computer. If the fault persists, then the disc drive is at fault.

2 (Issue 1 boards only). There should be a small capacitor from the DRQ line to ground. Is this fitted? Is its value correct?

3 There may be a fault in the memory system. Check that the address inputs to the Memory Controller (IC20 pins 21 to 28 inclusive) are switching with good logic levels. Check that the outputs: the AA and AT lines are switching. A good test here is to press BREAK repeatedly and look at each line in turn.

4 Check that the AA and AT lines are correctly connected to the address multiplexers, IC29 and IC33.

5 Use a memory test program to validate memory. This is rarely necessary as the memory chips are highly reliable.

7.8.6 Data can be read correcty but cannot be written reliably.

1 Is the disc formatted for DFS but being used with ADFS or vice versa? The built in formatter is only for use with DFS.

2 Check the disc drive on another computer if possible.

3 Check that data transitions are appearing on the 1770 WD and WG pins, IC3 pins 22 and 21. If not then check all connections to the 1770 (IC3) and the 74LS174 (1C4).

4 Follow the signal path of WD to the connector.
Note: a disc drive must be connected at this stage as pull-up resistors for the line driver outputs are within the disc drive. The output should be normally high with low going transitions.

5 Follow the signal path of WG to the connector.
Note: a disc drive must be connected at this stage as pull-up resistors for the line driver outputs are within the disc drive. The output should be normally high with low going transitions.

7.8.7 Data can be read and written correctly, but only one disc drive can be selected out of two.

1 Check all connections to the 74LS174 (IC4).

2 Check that only one drive select output is a logic LOW from the 7438, IC2 pins 3 and 6.

7.9 Parallel printer port

1 Check that the configuration system is set up correctly (i.e. *CONFIGURE PRINT 1). Use the default printer driver to conduct the tests.

2 If the fault only shows up with a custom printer driver, test the software carefully first.

3 Check the printer with another computer if possible.

4 Check the computer with another printer if possible.

5 Check that pin 40 on the User VIA (IC6) has a pull up to +5V (R11) but is not short circuited to +5V.

6 Check that data appearing on Port A of the VIA (IC6 pins 2 to 9) appears on the outputs of the 74LS244 buffer (IC5).

7 Check that a strobe pulse appears on IC6 pin 39 for every character transmitted. If not then check all address, data and control pins on the User VIA.

8 Check that a strobe pulse is found inverted at pin 11 of the 7438 (IC2) and true at pin 8 of the 7438 (IC2).

7.10 User port

1 Is the software illegal, for example, using peek and poke type commands from a second or co-processor? If so, this is the cause of the problem. It would work on the I/O processor alone but this is not recommended.

2 Is the shift register being used to transfer data on the CA lines? There is a fault in some manufacturers' 6522's and for this reason the use of this feature of the 6522 is not specified for the computer.

3 Check the software very carefully.

4 Check all address, data and control lines to the User VIA 106.

5 Have voltages outside the supply range been applied to any of the pins? If so, the VIA may have been damaged.
Note: this could arise if a cable is left connected the the User Port and the other end is, for instance, left trailing across a carpet.

7.11 1MHz bus

1 Is there anything in the configuration system that would cause the 1MHz bus to be deselected? For example, this would happen if the computer were configured to power up with a floppy disc drive as the default rather than a hard disc, therefore making the hard disc seem not to work.

2 Ensure that the software has not selected the internal pages &FC and &FD.

3 As with any straightforward parallel data bus, any faults with this have to be found by methodical checking of all connections.

a) Ensure the remote equipment is not at fault (if possible).

b) Ensure the cables and connectors are in good condition and are correctly assembled, i.e. cable clamps are fitted and effective.

c) Ensure that any non-polarised connectors are correctly inserted.

d) Cables longer than 1m should in general not be used.

e) Check that each and every connection is correct as per the circuit diagram.

f) Check that the READY signal from the I0 Controller (IC15 pin 17) goes to both the CPU (IC14 pin 2) and the Peripheral Bus Controller (IC21 pin 11).

g) Check that the FIT connection from the I0 controller (IC15 pin 38) goes to the PBC (IC21 pin 5).

h) Check that all address connections to the Memory Controller (IC20) are correct.

i) Check that the two data bus connections to the I0 Controller are correct (IC15 pins 18 and 19).

7.12 The Tube

1 Check 3 a) b) c) d) e) f) g) h) and i) as for 1MHz bus above.

7.13 Internal co-processor

7.13.1 Not being recognised.

1 Is the configuration status correct?

2 Are the two connectors correctly mated?

3 Are two bits of the data bus correctly connected to the I0 Controller (IC15 pins 18 and 19)?

4 Are all connections to the two connectors correct?

7.13.2 Recognised, but just a cursor in the top left hand corner of the screen.

1 Is the co-processor working? Try it in another computer.

2 Are the two connectors correctly mated?

3 Are the boot ROM(s) correctly inserted in the co-processor?

7.14 Sound output

7.14.1 Will not work at all.

1 Is the speaker connected?

2 Is there an external speaker (to the sound phono connector at the rear of the machine) which is short circuited or of very low impedance (less than 4 ohms)? If so, remove it.

7.14.2 Will not work with all envelopes.

1 Has your software requested too many channels? The envelopes use memory shared with serial data buffer space.

7.14.3 Produces strange sounds whenever a key is pressed.

1 Are all the connections to the sound chip correct as shown in the circuit diagram?

2 Try pressing BREAK. If the sound goes away then it may be mains noise affecting the computer. This could happen in places with poor mains supplies.

3 On some early computers, pin 15 of IC10 was connected to PRST. It should now be connected to +5V.

7.15 Modem connector

1 Check the controlling software VERY carefully

2 Check all connections to the connector.

3 Check that a signal arriving at the connector goes through it, i.e. there are no dry joints or faulty connector sockets.

7.16 Cartridge port

7.16.1 Causes the sound output to be noisy.

1 Check the cartridge for shorts and general layout.

7.16.2 Will not recognise some cartridges.

1 Is the cartridge for the Electron? Not all of these are compatible.

2 Are all the links assocciated with the cartridge in the correct position.

3 Is the cartridge edge connector excessively worn, e.g. gold plating worn through?

4 Are all connections to the edge connectors correct without shorts to each other?

5 Are any of the edge connector blades bent or worn? If so, the connector must be replaced.

7.17 Econet

Econet can only be serviced properly by Econet service centres, who will have the necessary test equipment to check the system thoroughly. However, there are a few simple things which can be checked without the test equipment. Follow the Econet board circuit diagram in the Appendix.

1 Check that the two connectors on the Econet module are correctly inserted. The longer connector has two spare pins on the left of the PCB socket. If the module is displaced and is plugged into one or both of these spare pins, it will not work.

2 Check that the Econet module is installed and fitted correctly.

3 Check that NMI on the CPU pin 6 IC14 (TP 3) is not being held low.

Appendix

Connector pinouts

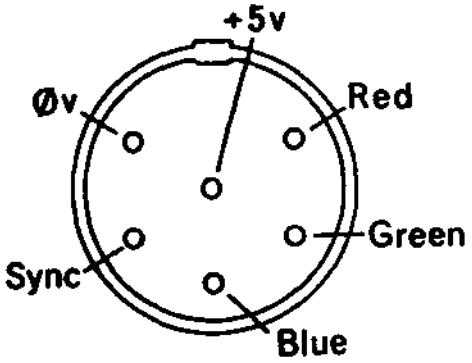
TV UHF out
phono

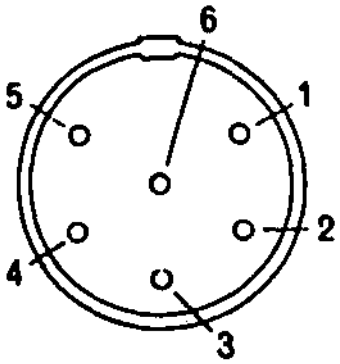
outer: ground
inner: UHF

SK8 video out
BNC

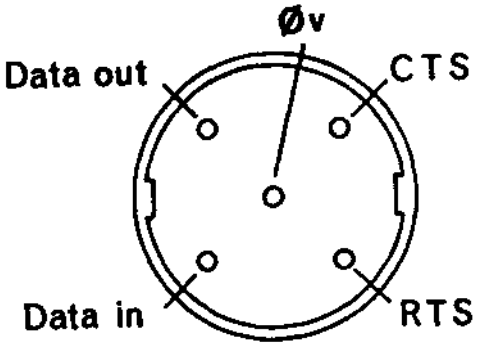
outer: ground
inner: video

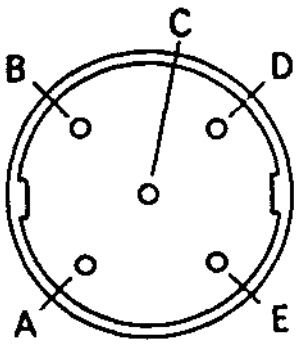
SK9 RGB
6-pin DIN



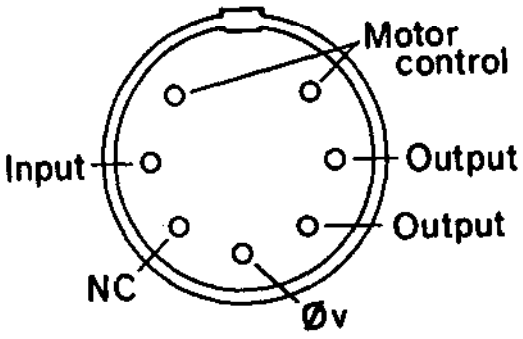


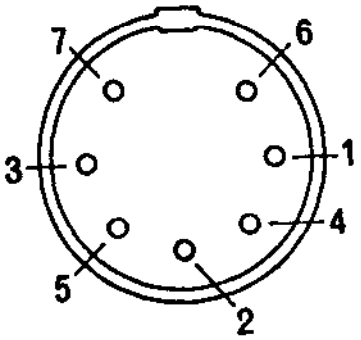
SK10 RS423
5-pin DIN



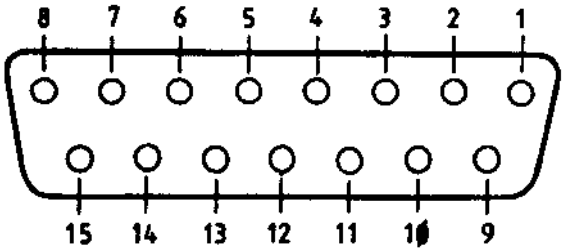


SK11 cassette
7-pin DIN



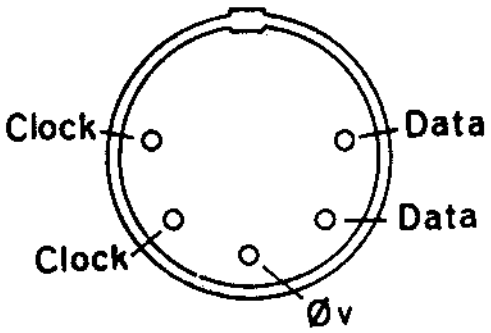


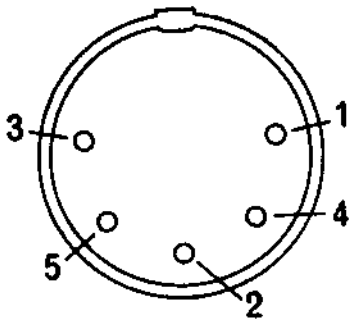
SK12 analogue in
15-way D-type



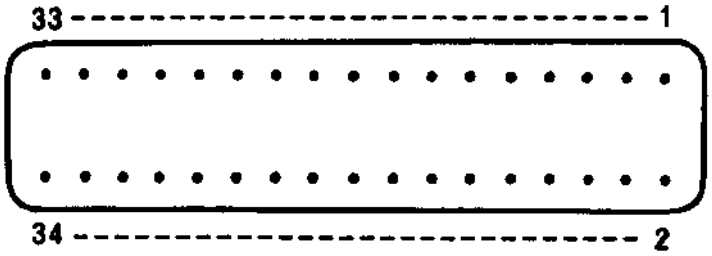
1 +5V	9 light pen strobe (notLPSTB)
2 0V	10 digital switch input (I1)
3 0V	11 voltage reference (VREF)
4 CH3	12 CH2
5 analogue ground	13 digital switch input (I0)
6 0V	14 voltage reference (VREF)
7 CH1	15 CH0
8 analogue ground	

SKI ECONET
5-pin DIN



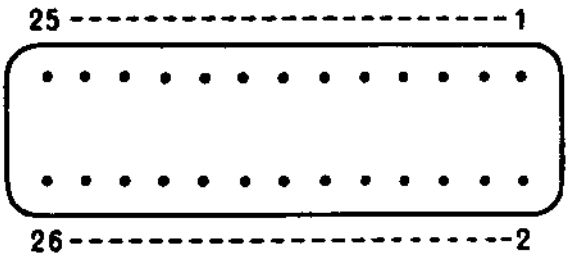


PL1 disc drive
34-way IDC



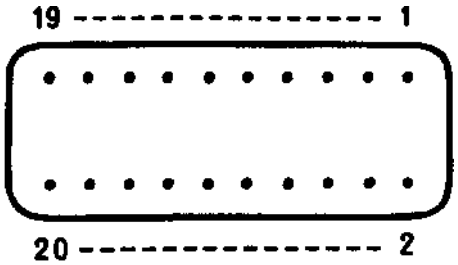
1	0V	2	(notS/SEL 8")
3	0V	4	(notINX 8")
5	0V	6	NC
7	0V	8	notINX 5 1/4"
9	0V	10	notS0
11	0V	12	notS1
13	0V	14	NC
15	0V	16	notMOTOR
17	0V	18	notDIR
19	0V	20	notSTEP
21	0V	22	notW/DATA
23	0V	24	notWR/EN
25	0V	26	notTK0
27	0V	28	notWR PCT
29	0V	30	notR/DATA
31	0V	32	notS/SEL 5 1/4"
33	0V	34	(notRDY 8")

PL3 printer
26-way IDC



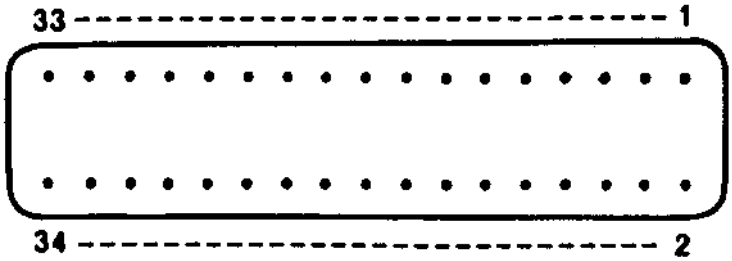
1	STB	2	0V
3	PA0	4	0V
5	PA1	6	0V
7	PA2	8	0V
9	PA3	10	0V
11	PA4	12	0V
13	PA5	14	0V
15	PA6	16	0V
17	PA7	18	0V
19	ACK	20	0V
21	NC	22	0V
23	NC	24	0V
25	NC	26	NC

PL4 user port
20-way IDC



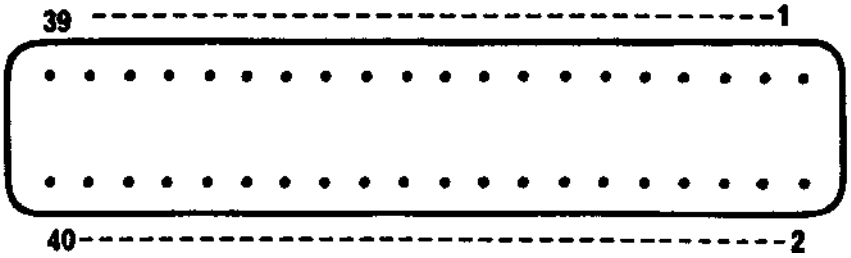
1	+5V	2	CB1
3	+5V	4	CB2
5	0V	6	PB0
7	0V	8	PB1
9	0V	10	PB2
11	0V	12	PB3
13	0V	14	PB4
15	0V	16	PB5
17	0V	18	PB6
19	0V	20	PB7

PL5 1MHz bus
34-way IDC



1	0V	2	R/notW
3	0V	4	1E
5	0V	6	notNMI
7	0V	8	notIRQ
9	0V	10	notPGFC
11	0V	12	notPGFD
13	0V	14	notRS
15	0V	16	audio in/out (see LK1)
17	0V	18	D0
19	D1	20	D2
21	D3	22	D4
23	D5	24	D6
25	D7	26	0V
27	A0	28	A1
29	A2	30	A3
31	A4	32	A5
33	A6	34	A7

PL6 TUBE
40-way IDC



1	0V	2	R/notW
3	0V	4	2E
5	0V	6	notIRQ
7	0V	8	notTUBE
9	0V	10	notRS
11	0V	12	DO
13	0V	14	D1
15	0V	16	D2
17	0V	18	D3
19	0V	20	D4
21	0V	22	D5
23	0V	24	D6
25	0V	26	D7
27	0V	28	AO
29	0V	30	A1
31	+5V	32	A2
33	+5V	34	A3
35	+5V	36	A4
37	+5V	38	NC
39	+5V	40	NC

PL11 and PL24 keyboard
2x15-pin molex

PL11

1	C6
2	BAT
3	R0
4	R6
5	R7
6	R2
7	R1
8	C11
9	C10
10	C12
11	C0
12	C2
13	c9
14	c4
15	C5

PL24

1	C8
2	C7
3	C3
4	C1
5	R5
6	R4
7	R3
8	C
9	SHIFT LOCK
10	CAPS LOCK
11	POWER
12	S
13	KBD SW
14	0VB
15	+5VB

Parts list

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
1	0243,000	BARE BOARD ISS. 1	1	
2	0143,000	ASSEMBLY DRAWING	1	PER BATCH
3				
4	0201,647	IC VIDEO PROCESSOR	1	1C42
5	0201,648	IC SERIAL PROCESSOR	1	IC48
6				
7	0201,796	PCB REAR PANEL	1	
9				
10	0201,843	IC EROS 1MB ROM	1	IC24
11	0201,844	IC MSI KEYBD ENC (CF30047)	1	1C16
12	0201,845	IC MSI P.B.C. (CF30049)	1	IC21
13	0201,846	IC MSI CRTC MUX (CF30048)	1	IC31
14	0201,847	IC MSI I/O CTRL (CF30050)	1	IC15
15				
16	2201,211	IC MSI CHROMA (CF30060)	1	1C40
17	2201,213	IC MSI MEM SW (CF30058)	1	IC20
18				
19				
20				
21				
22				
23	0502,100	RES 10R C/MF 5% 0W25	4	R27,37,38,113
24	0502,101	RES 100R C/MF 5% 0W25	4	R48,49,57,58
25	0502,102	RES 1K0 C/MF 5% 0W25	17	R13,33,34,43,47, 51, 54,56,75,117, 122, 133,137,145, 148,150, 151
26				
27				
28	0502,103	RES 10K C/MF 5% 0W25	18	R8,14,18-21,23, 28, 29,32,53,71, 81,83, 102,109, 114,120
29				
30				
31	0502,104	RES 100K C/MF 5% 0W25	5	R10,22,24,30,80
32	0502,105	RES 1MO C/MF 5% 0W25	2	R46,155
33	0502,122	RES 1K2 C/MF 5% 0W25	3	R77,78,89
34	0502,151	RES 150R C/MF 5% 0W25	5	R1,3,5,6,59
35	0502,152	RES 1K5 C/MF 5% 0W25	3	R65,108,140
36				
37	0502,154	RES 150K C/MF 5% 0W25	2	R110,111
38				
39	0502,182	RES 1K8 C/MF 5% 0W25	1	R69
40				
41				
42	0502,221	RES 220R C/MF 5% 0W25	3	R44,50,121
43	0502,222	RES 2K2 C/MF 5% 0W25	8	R4,11,76,90,105, 107, 134,149
44				

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
45	0502,223	RES 22K C/MF 5% 0W25	1	R36
46	0502,224	RES 220K C/MF 5% 0W25	2	R35,104
47	0502,272	RES 2K7 C/MF 5% 0W25	3	R88,103,131
48	0502,273	RES 27K C/MF 5% W25	1	R52
49	0502,274	RES 270K C/MF 5% 0W25	1	R70
50				
51	0502,330	RES 33R C/MF 5% W25	3	R62,64,127
52	0502,331	RES 330R C/MF 5% 0W25	7	R40,41,42,96, 97, 98,100
53	0502,332	RES 3K3 C/MF 5% W25	5	R66,67,87,118,130
54	0502,333	RES 33K C/MF 5% 0W25	1	8119
55	0502,391	RES 390R C/MF 5% W25	1	R136
56	0502,392	RES 3K9 C/MF 5% 0W25	3	R132,146,147
57	0502,393	RES 39K C/MF 5% W25	3	R31,39,91
58				
59	0502,471	RES 470R C/MF 5% 0W25	2	R153,154
60	0502,472	RES 4K7 C/MF 5% 0W25	9	R7,26,72,73,84, 125 ,126,128,129
61				
62	0502,473	RES 47K C/MF 5% 0W25	1	R115
63				
64	0502,562	RES 5K6 C/MF 5% 0W25	1	R74
65	0502,563	RES 56K C/MF 5% 0W25	1	R82
66	0502,565	RES 5M6 C/MF 5% W25	1	R17
67				
68	0502,680	RES 68R C/MF 5% 0W25	8	855,138,139, 141-144,152
69	0502,681	RES 680R C/MF 5% W25	1	R85
70	0502,682	RES 6K8 C/MF 5% W25	1	8116
71				
72	0502,820	RES 82R C/MF 5% 0W25	3	R68,94,95
73	0502,822	RES 8K2 C/MF 5% W25	2	R92,101
74	0502,824	RES 820K C/MF 5% 0W25	1	R112
75				
76				
77	0590,222	RES NET 2K2 TF 10% 9P	2	RP1,2
78				
79				
80				
81				
82	0611,047	CPCTR TANT 4u7 16V 20%	1.	C14
83	0611,100	CPCTR TANT 10u 16V 20%	3	C15,17,60
84	0611,470	CPCTR TANT 47u 16V 20%	1	C21
85				
86				
87	0613,100	CPCTR TANT lu0 35V 20%	2	032,49
88	0613,101	CPCTR TANT 10u 35V 20%	1	C11
89				
90	0629,002	CPCTR CPLT 2n2 30V 80%	3	C9,12,35
91	0629,004	CPCTR CPLT 4n7 30V 80%	2	C40,43
92	0629,010	CPCTR CPLT 10n 3V 80%	1	C47
93				
94	0630,082	CPCTR CPLT 820p 3V 10%	2	C55,56
95				
96				

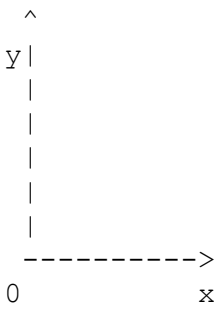
ITEM	PART NO	DESCRIPTION	QTY	REMARKS
97	0631,010	CPCTR CPLT 10p 3V 2%	1	C19
98	0631,022	CPCTR CPLT 22p 3V 2%	1	C26
99	0631,027	CPCTR CPLT 27p 3V 2%	1	C80
100	0631,033	CPCTR CPLT 33p 3V 2%	4	C6,7,83,84
101	0631,039	CPCTR CPLT 39p 3V 2%	1	C81
102	0631,047	CPCTR CPLT 47p 3V 2%	5	C23,44,45,88,92
103	0631,100	CPCTR CPLT 100p 3V 2%	3	03,85,86
104	0631,150	CPCTR CPLT 150p 3V 2%	1	C87
105	0631,220	CPCTR CPLT 220p 3V 2%	2	C24,27
106	0631,270	CPCTR CPLT 270p 3V 2%	4	C62,63,64,69
107	0634,010	CPCTR CPLT 10n 5V 80%	1	C91
108	0635,470	CPCTR ALEC 47u 16v RAD	4	C18,71-73
109	0637,104	CPCTR CML 100n 5V 80%	3	C2,10,22
110	0637,473	CPCTR CML 47n 5V 80%	1	C16
111				
112	0650,333	CPCTR MPSTR 33n 5V 20%	1	C36
113	0650,334	CPCTR MPSTR 330n 5V 20%	2	04,79
114	0651,224	CPCTR CER 220n 12V 80%	2	C34,46
115				
116	0680,002	CPCTR DCPLR 33/47n 0.2"	45	A
117	0680,005	CPCTR DCPLR 33/47n 5Px6H	1	Cl
118				
119	0699,001	CPCTR TRMR 2/22p 5V	1	VC1
120	0699,004	CPCTR TRMR 5.5/40p 25V	1	VC2
121	0701,770	IC WD1770 FDC 5.25"	1	IC3
122	0704,105	IC 4464 DRAM 120nS 64Kx4	4	IC17,18,23,26
123	0705,050	IC SAA5050 CHTR GEN	1	IC32
124	0706,489	IC 76489 SOUND GEN	1	IC12
125	0706,512	IC 65C12 CPU CMOS 2MHZ	1	IC14
126	0706,522	IC 6522 VIA NMOS 1MHZ	2	IC6,8
	0706,524	IC 6522 VIA CMOS 1MHZ		OPTION
128	0706,818	IC 6818 RTC CMOS	1	IC11
129	0706,845	IC 6845 CRTC NMOS 1MHZ	1	IC22
130	0706,850	IC 6850 ACIA NMOS 1MHZ	1	IC45
131	0707,002	IC 7002 ADC 12 BIT	1	IC49
132	0709,637	IC 9637A RS422/423 RCVR	1	IC51
133	0733,691	IC 3691 RS422/423 DRVR	1	IC50
134				
135	0740,006	IC 7406 TTL 14/0.3"	1	IC1
	0740,016	IC 7416 TTL 14/0.3"		OPTION
137	0740,038	IC 7438 TTL 14/0.3"	1	IC2
138				
139	0741,000	IC 74S00 TTL 14/0.3"	1	IC34
140	0741,004	IC 74S04 TTL 14/0.3"	1	IC43
141				
142				
143	0742,000	IC 74LS00 TTL 14/0.3"	1	IC38
	0744,000	IC 74ALS00 TTL 14/0.3"		OPTION
145				
146	0742,002	IC 74LS02 TTL 14/0.3"	1	IC39
147	0742,014	IC 74LS14 TTL 14/0.3"	1	IC19
148	0742,086	IC 74LS86 TTL 14/0.3"	1	IC25
	0744,086	IC 74ALS86 TTL 14/0.3"		OPTION
150				

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
151	0742,174	IC 74LS174 TTL 16/0.3"	1	IC4
152	0742,244	IC 74LS244 TTL 20/0.3"	1	IC5
153	0742,257	IC 74LS257 TTL 16/0.3"	1	IC30
	0744,257	IC 74ALS257 TTL 16/0.3"		OPTION
155				
156	0742,259	IC 74LS259 TTL 16/0.3"	1	IC10
	0744,259	IC 74ALS259 TTL 16/0.3"		OPTION
158				
159	0742,373	IC 74LS373 TTL 20/0.3"	1	IC7
	0744,373	IC 74ALS373 TTL 20/0.3"		OPTION
161	0748,000	IC 74F00 TTL 14/0.3"	1	IC36
162	0748,074	IC 74F74 TTL 14/0.3"	1	IC28
163				
164				
165	0749,253	IC 74HCT253 CMOS 16/0.3"	2	IC29,33
166				
167	0770,324	IC LM324 QUAD OP AMP	2	IC9,46
168	0770,386	IC LM386 AUDIO AMP	1	1C13
169				
170	0780,177	FEAT J177 T092 30V P-CHAN	1	Q4
171				
172	0780,239	TRANS BC239 NPN	8	Q3,5,6,8,9,10,12,14
173	0780,309	TRANS BC309 PNP	2	Q11,13
174				
175	0794,148	DIODE SI 1N4148	14	D7-10,12,13,17-24
176				
177	0800,001	CONR 5W SKT DIN RA DOM	1	SK10
178	0800,002	CONR 6W SKT DIN RA PCB	1	SK9
179	0800,003	CONR 7W SKT DIN RA PCB	1	SK11
180	0800,004	CONR 5W SKT DIN RA PCB	1	SK7
181	0800,006	CONR 34W HDR IDC RA 4 WALL	2	PL1,5
182	0800,007	CONR 40W HDR IDC RA 4 WALL	1	PL6
183	0800,008	CONR 26W HDC IDC RA 4 WALL	1	PL3
184	0800,009	CONR 20W HDC IDC RA 4 WALL	1	PL4
185				
186	0800,043	CONR 44W EDGE DS ST FLNG	2	SK3,4
187	0800,050	CONR 2W WAFR 0.1" ST PCB	4	LK4,21,60,61
188	0800,051	CONR 3W WAFR 0.1" ST PCB	4	PL8,LK12,18,19
189	0800,067	CONR 5W WAFR 0.1" RA 4PIN	1	PL10
190	0800,070	CONR 2W SHUNT 0.1"	5	LK4,12,18,19,60
191	0800,091	CONR 2W WAFR .1" RA PCB	1	PL9
192				
193				
194				
195				
196				
197	0800,128	SKT IC 28/0.6" NORM	3	IC27,37,41
198				
199	0800,203	FSTN TAB 6.3mm ST PCB	7	PL17-23
200				
201				
202	0800,304	CONR 15W SKT "D" RA E2.84	1	SK12
203				

ITEM	PART NO	DESCRIPTION	QTY	REMARKS
204	0800,455	CONR 15W WAFR .1" ST PCB	2	PL11,PL24
205				
206				
207	0800,481	CONR 5W SKT HSNG 0.1" PCB	1	SK6
208	0800,482	CONR 12W SKT HSNG 0.1" PCB	2	SK1,2
209	0800,483	CONR 19W SKT HSNG 0.1" PCB	1	SK5
210				
211				
212				
213				
214				
215				
216				
217	0800,600	CONR BNC SKT 75R PNL	1	SK8
218	0800,611	CONR PHONO SKT RA PCB	1	SK13
219	0801,200	CONR 20W 0.1" SR ZIF 4WR	1	PL12
220				
221	0810,001	RLY 1P CO 5V 50R PCB	1	RL1
222				
223				
224				
225				
226				
227	0820,160	XTAL 16.000MHz HC18/U	1	X2
228	0820,177	XTAL 17.7345MHz HC18/U	1	X3
229	0821,327	XTAL 32.768KHz CC 0.05"	1	X1
230				
231				
232	0825,000	MODUL UHF PAL WB E36	1	MD1
233				
234				
235	0860,005	COIL RF 33uH AX Q=45	1	Li
236				
237	0870,420	WIRE 22SWG CPR TIN	A/R	L4-10
238				
239	0884,042	RIVET POP DOME HD 3.2mmD	4	
240				

Component Locations

The following tables show the positions of ICs, resistors, capacitors, diodes, and transistors on the circuit diagram given later in the Appendix. The circuit diagram is split into 2 sheets, and the sheet on which the component appears is given in the Sheet column. The Position column gives the x,y coordinate of each component with respect to a 10 by 10 grid drawn on each sheet of the circuit diagram.



IC nos	Location	Sheet
1	1,8/1,9	2
2	2,5/1,7	2
3	2,8	2
4	2,7	2
5	2,6	2
6	2,5/2,6	2
7	2,2	2
8	2,8	2
9	4,2/5,4/5,5/6,5	2
10	4,8	2
11	6,7	2
12	6,6	2
13	4,3	2
14	2,8	1
15	2,6	1
16	6,3	2
17	6,0	1
18	4,0	1
19	9,4/3,5/6,6/0,8/0,9	1
20	3,8	1
21	9,3/9,4	1
22	7,1	2
23	5,o	1
24	3,8/4,8	1
25	6,5/7,9	1
26	3,0	1
27	4,8	1
28	4,2/5,6	1
29	4,7	1
3o	4,5	1
31	4,4	1
32	7,3	1
33	4,6	1
34	2,1/6,2/7,9	1
35	9,5/9,6	1
36	2,0/2,1/3,1	1
37	5,8	1
38	5,1/5,7/6,7	1
39	5,5/0,8/1,8/0,9/1,9	1
40	7,7	1
41	6,8	1
42	6,3/6,4	1
43	8,5/8,6	1
44		
45	7,7/7,8	2
46	8,6/7,6/8,7	2
47		
48	7,8	2
49	7,5	2
50	8,8	2
51	8,7	2

R nos	Location	Sheet
1	7,2/1,9	2
2	7,2/1,7	2
3	1,9	2
4	2,4	2
5	1,9	2
6	1,9	2
7	2,4	2
8	1,3	2
9	8,5	1
10	1.3	2
11	3,7	2
12	5,8	2
13	4,4	2
14	3,9	2
15	5,7	2
16		
17	5,7	2
18	5,6	2
19	5,5	2
20	4,4	2
21	3,9	2
22	2,4	2
23	6,9	2
24	5,7	2
25	5,6	2
26	4,4	2
27	4,5	2
28	4,4	2
29	6,8	2
30	5,6	2
31	5,4	2
32	6,5	2
33	3,3	1
34	3,3	1
35	6,5	2
36	5,4	2
37	5,4	2
38	5,3	2
39	6,5	2
40	5,9	2
41	5,9	2
42	5,9	2
43	1,9	1
44	3,7	1
45	9,4	1
46	9,4	1
47	8,4	1
48	0,8	1
49		

R nos	Location	Sheet
50	5,5	1
51	7,4	1
52	0.9	1
53	0,8	1
54	7,5	1
55	5,2	1
56	7,5	1
57	5,2	1
58	6,6	1
59	6,5	
60	6,4/6,5	1
61		
62	6,7	1
63		
64	6,2	1
65	3,8	1
66	7,5	2
67	3,3	1
68	7,8	1
69	7,6	2
70	4,3	2
71	7,6	2
72	7,6	2
73	7,6	2
74	7,5	2
75	7,8	1
76	7,7	2
77	7,7	1
78	7,7	1
79		
80	8,7	2
81	8,6	2
82	9,9	2
83	8,6	2
84	7,7	1
85	7,7	1
86		
87	7,7	1
88	8,5	2
89	7,7	1
90	7,7	1
91	8,6	2
92	8,6	2
93		
94	7,8	1
95	8,8	1
96	8,6	1
97		
98	8,6	1
99		

R nos	Location	Sheet
100	8,5	1
101	8,6	1
102	8,7	2
103	8,7	2
104	8,5	2
105	9,5	2
106		
107	2,5	1
108	1,8	1
109	8,7	2
110	9,6	2
111	9,6	2
112	9,5	2
113	8,8	1
114	9,6	2
115	5,2	2
116	5,2	2
117	5,2	2
118	8,8	1
119		
120	6,4	2
121	5,3	1
122	1,0	1
123		
124		
125	3,0	1
126	2,0	1
127	3,1	1
128	5.8	1
129	6,8	1
130	8,7	1
131	8,7	1
132	8,7	1
133	8,7	1
134	8,7	1
135		
136	8,7	1
137	8,7	1
138		
139	9,7	1
140	8,8	1
141	9.9	1
142	9,9	1
143	9,9	1
144	8,8	1
145	8,7	1
146	9,7	1
147		
148	9,6	1
149	9,6	1
150	9,6	1
151	9,7	1
152	9,7	1
153	9,6	1
154	6,9	2
155	6,8	2

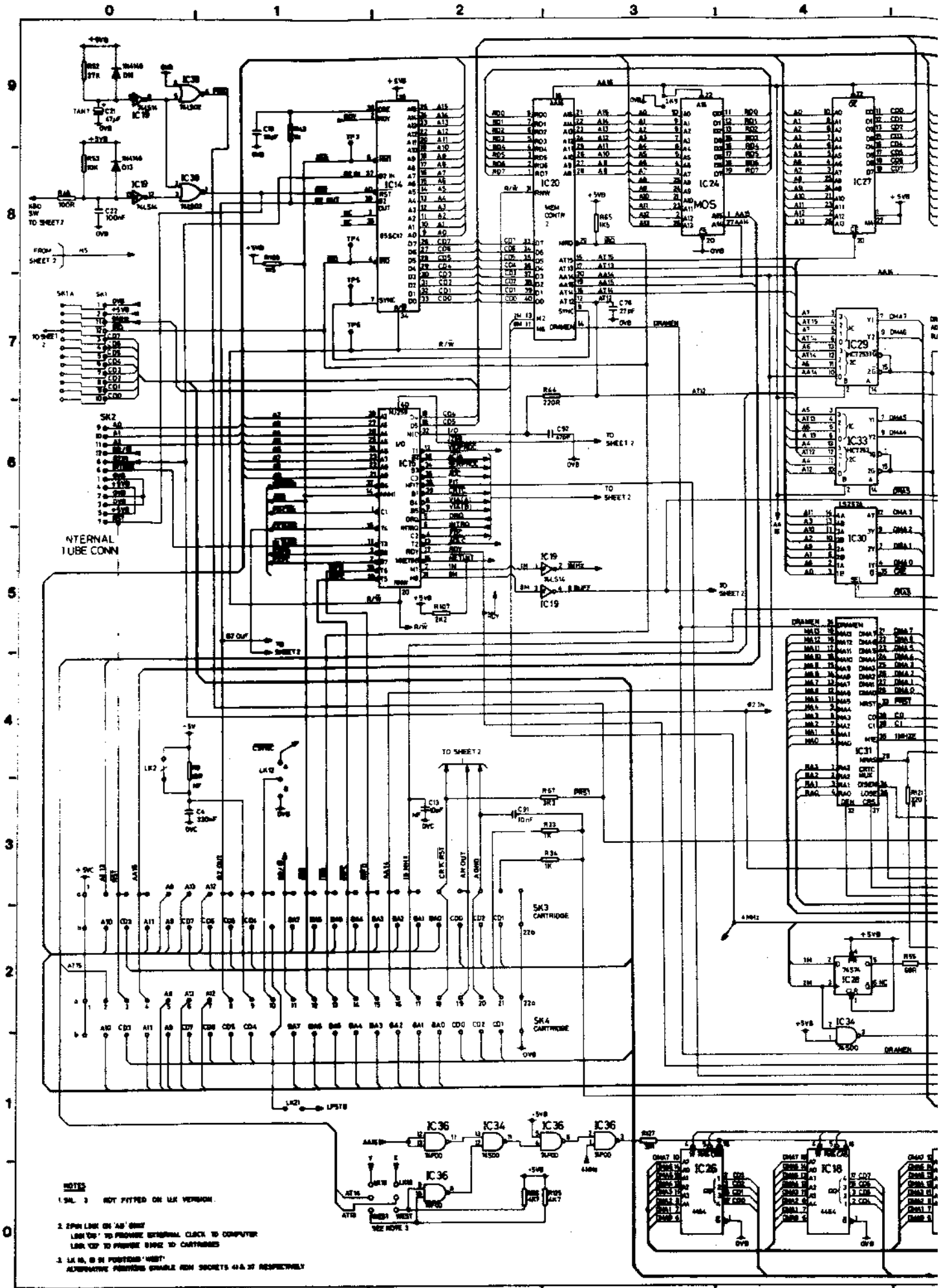
C nos	Location	Sheet
1	1,7	2
2	5,2	2
3	1,3	2
4	1,3	1
5	4,7	2
6	5,6	2
7	5,6	2
8	5,6	2
9	5,4	2
10	4,3	2
11	5,7	2
12	5,5	2
13	2,3	1
14	6,5	2
15	5,4	2
16	5,3	2
17	5,5	2
18	5.3	2
19	1,9	1
20	9,4	1
21	0,4	1
22	0,8	1
23	5,5	1
24	5,5	1
25	5,4	1
26	6,6	1
27		
28		
29		
30	6.5	1
31		
32	7,7	2
33		
34	7,6	2
35	8,6	2
36	8,5	2
37		
38		
39	8,9	2
40	8,5	2
41		
42		
43	8,5	2
44		
45		
46	8,7	2
47	8,5	2
48	9,7	1
49	9,5	2
50		

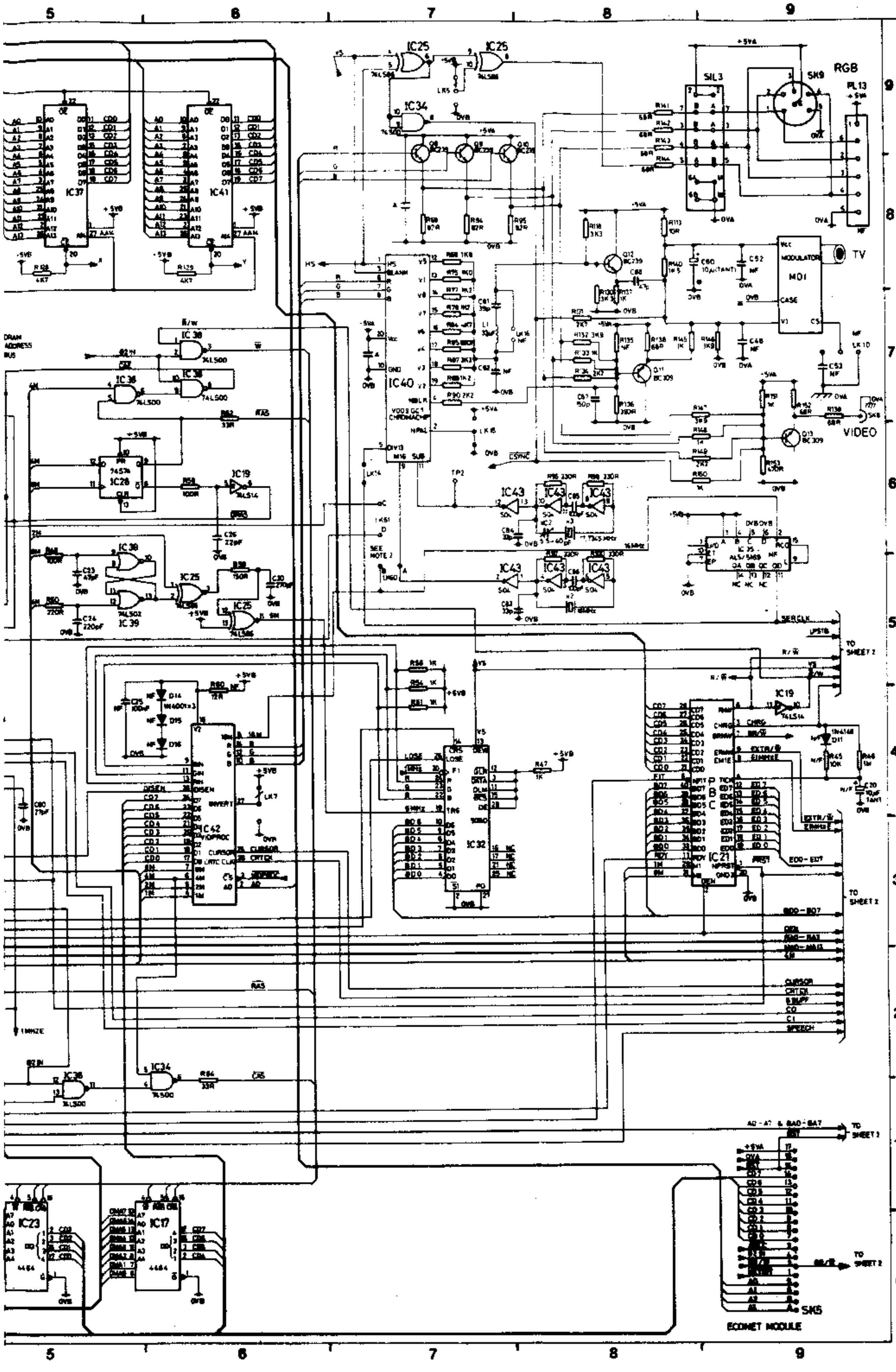
C nos	Location	Sheet
51	9,5	2
52	9,8	1
53	9,7	1
54	9,7	2
55	9,6	2
56	9,6	2
57		
58		
59	9,6	2
60	9,8	1
61	8,2	2
62	8,1	2
63	8,1	2
64	8,0	2
65	9,2	2
66	9,1	2
67	9,1	2
68	9,0	2
69	9,0	2
70	9,2	2
71	9,1	2
72	9,1	2
73	9,0	2
74		
75	9,4	2
76	9,4	2
77	5,3	2
78	3,7	1
79	6,4	2
80	5,4	1
81	7,7	1
82	7,7	1
83	8,5	1
84	8,6	1
85		
86	8,5	1
87	8,7	1
88	8,8	1
89		
90		
91	2,3	1
92	2,6	1

D nos	Location	Sheet
1	1,7	2
2	1,8	2
3	1,7	2
4		
5	5,7	2
6	6,4	2
7	5,5	2
8	6,8	2
9	7,2	2
10	7,2	2
11	9,4	1
12		
13		
14	6,4	1
15	6,4	1
16	6,4	1
17	8,5	2
18	8,5	2
19	8,5	2
20	8,6	2
21	9,6	2
22	9,6	2
23	6,4	2
24	6,4	2

Q nos	Location	Sheet
1	1,7	2
2	5,8	2
3	6,8	2
5	7,6	2
6	7,6	2
7		
8	8,9	1
9	8,9	1
10	9,9	1
11	8,7	1
12	8,8	1
13		
14	8,6	2

PCB circuit diagram
Sheet 1

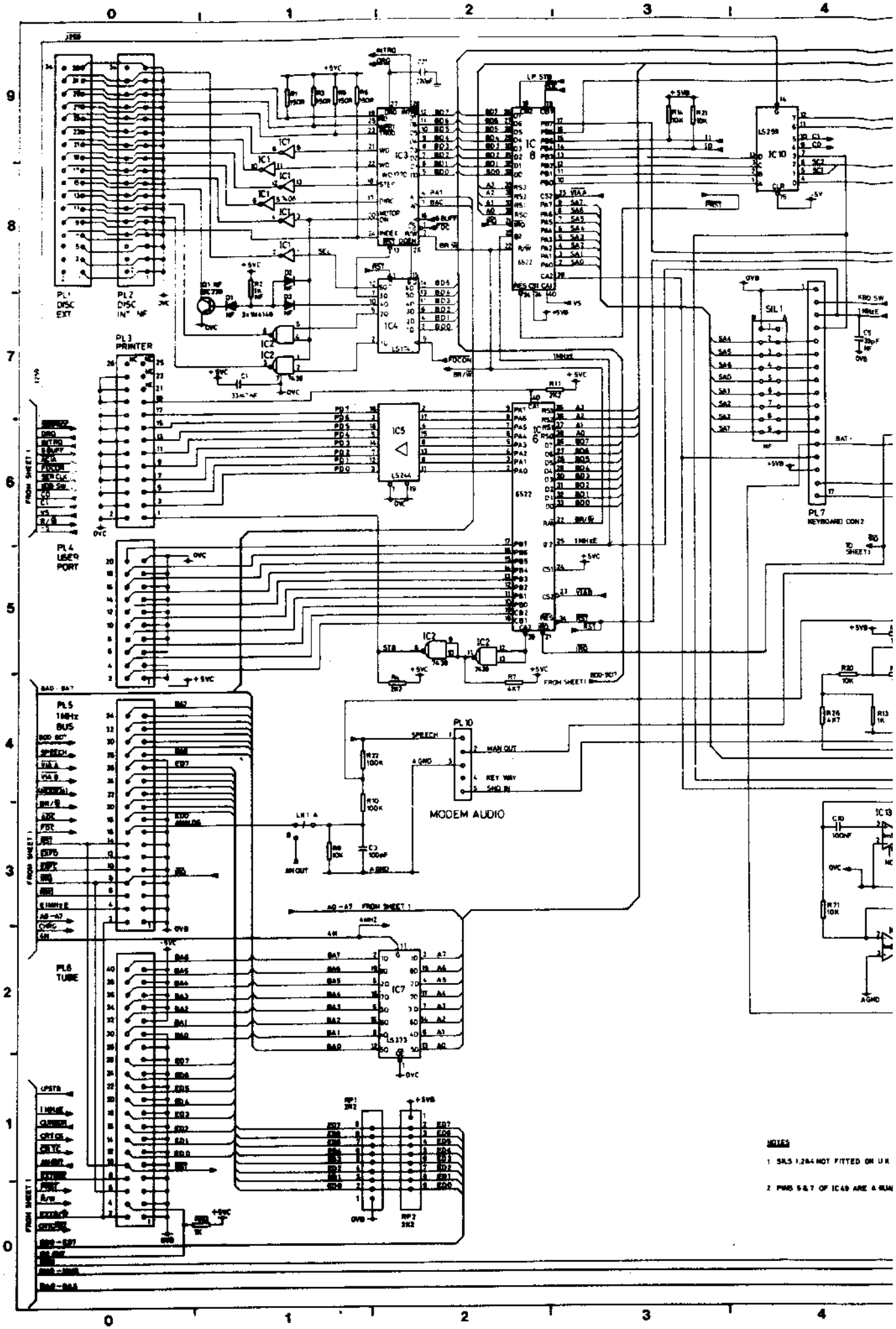


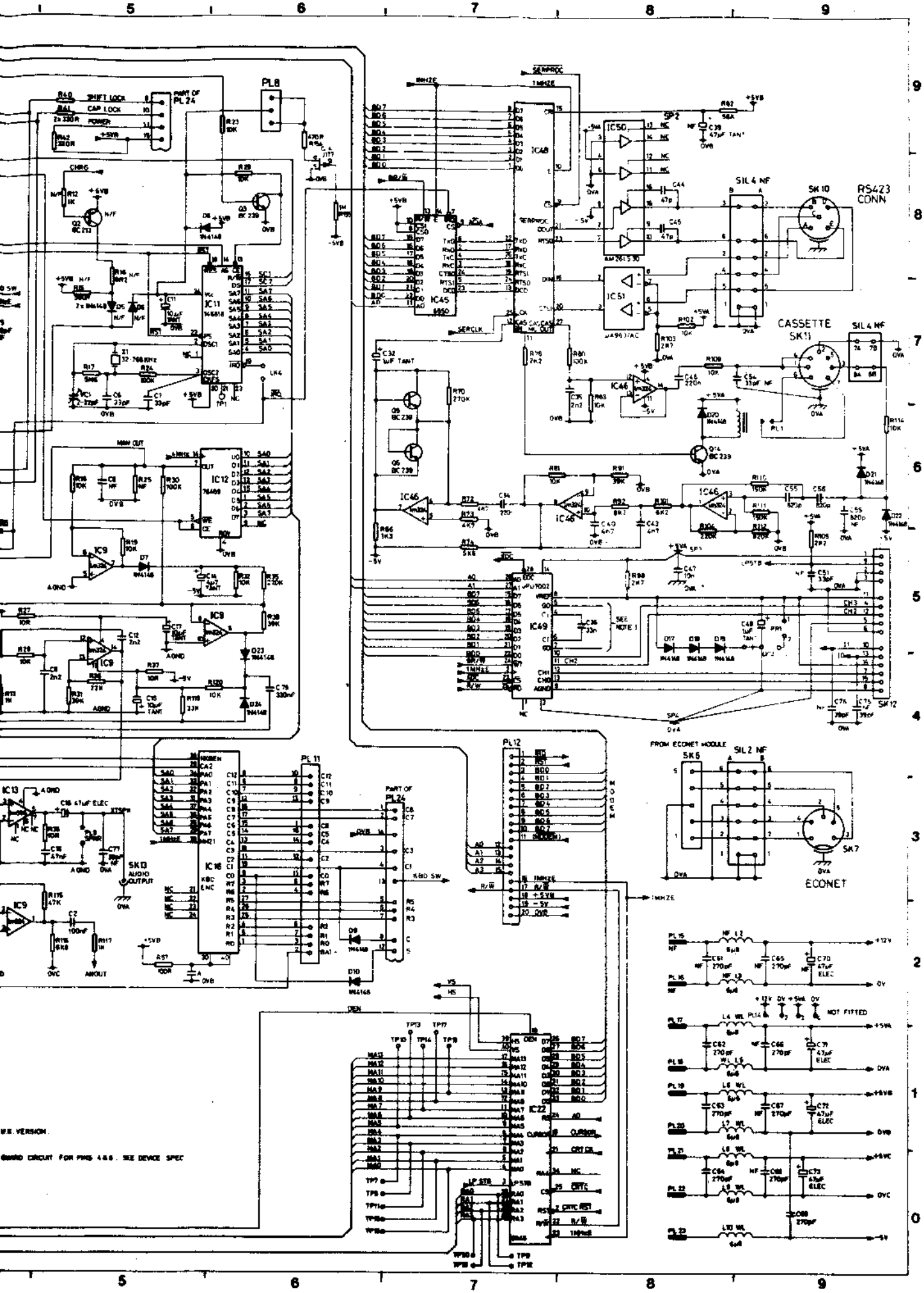


SUPPY	IC Nº	0V	+5V	TYPE Nº
C	1	7	14	7406
C	2	7	14	7438
C	3	14	28	WD1770
C	4	8	16	74LS174
C	5	10	20	74LS244
C	6	1	20	6522
C	7	10	20	74LS373
B	8	1	20	6522
B	9	*	*	LM386
B	10	8	16	74LS259
B	11	12	*	146818
B	12	8	16	76489
B	13	*	8	LM386
B	14	1,5,21	8	[illegible]
B	15	10	20	I/O CONT CF30060
B	16	10,20	*	KEYBOARD CF30047
B	17	16	8	4464
B	18	16	8	4464
B	19	7	14	74LS14
B	20	10,32	30	MEMCONT 2 CF3006[illegible]
B	21	10,32	30	PBC CF30048
D	22	1	20	6845
D	23	16	8	4464
D	24	14	28	EPROM
D	25	7	14	74LS86
D	26	16	8	4464
B	27	14	28	ROM/EPROM
B	28	7	14	74S74
B	29	8	16	74HCT153
B	30	8	16	74LS257A
B	31	10,20	20,40	CRTC MUX CF30048
B	32	1	28	SAA 5050
B	33	8	16	74HCT153
B	34	7	14	74S00
B	35	8	16	74ALS[illegible]
B	36	7	14	74F00
B	37	14	28	ROM/EPROM
B	38	7	14	74LS00
B	39	7	14	74LS02
B	40	10	20	CHROMA CF3[illegible]
B	41	14	28	ROM/EPROM
B	42	1	18	VID PROC
B	43	7	14	74S04
	44	NOT USED		
B	45	1	12	6850
B	46	*	*	LM 324
	47	NOT USED		
B	48	14	28	SERPROC
A	49	*	*	µPD7002
A	50	5	1	26LS30
A	51	4	1	µA9637AC

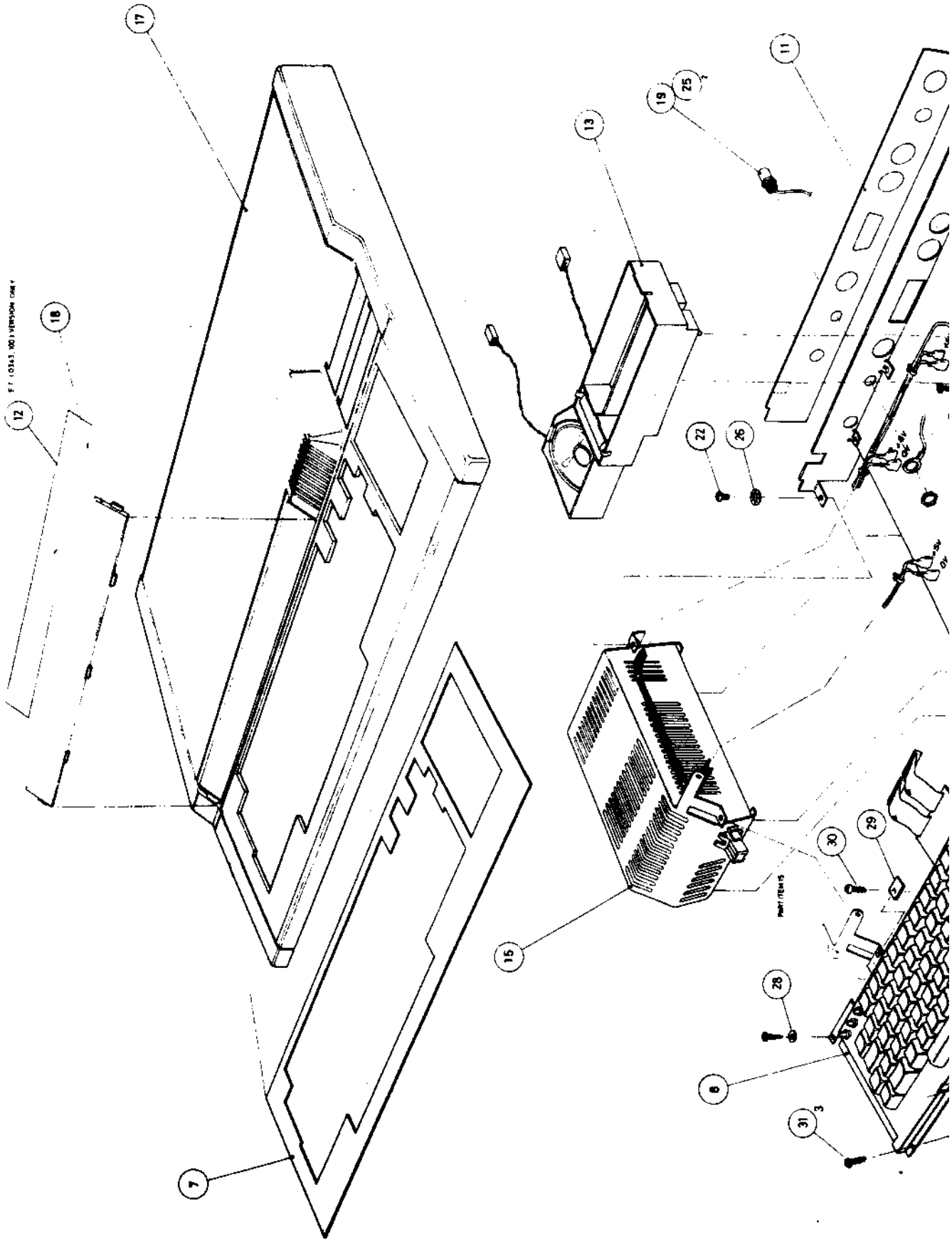
* SEE CIRCUIT

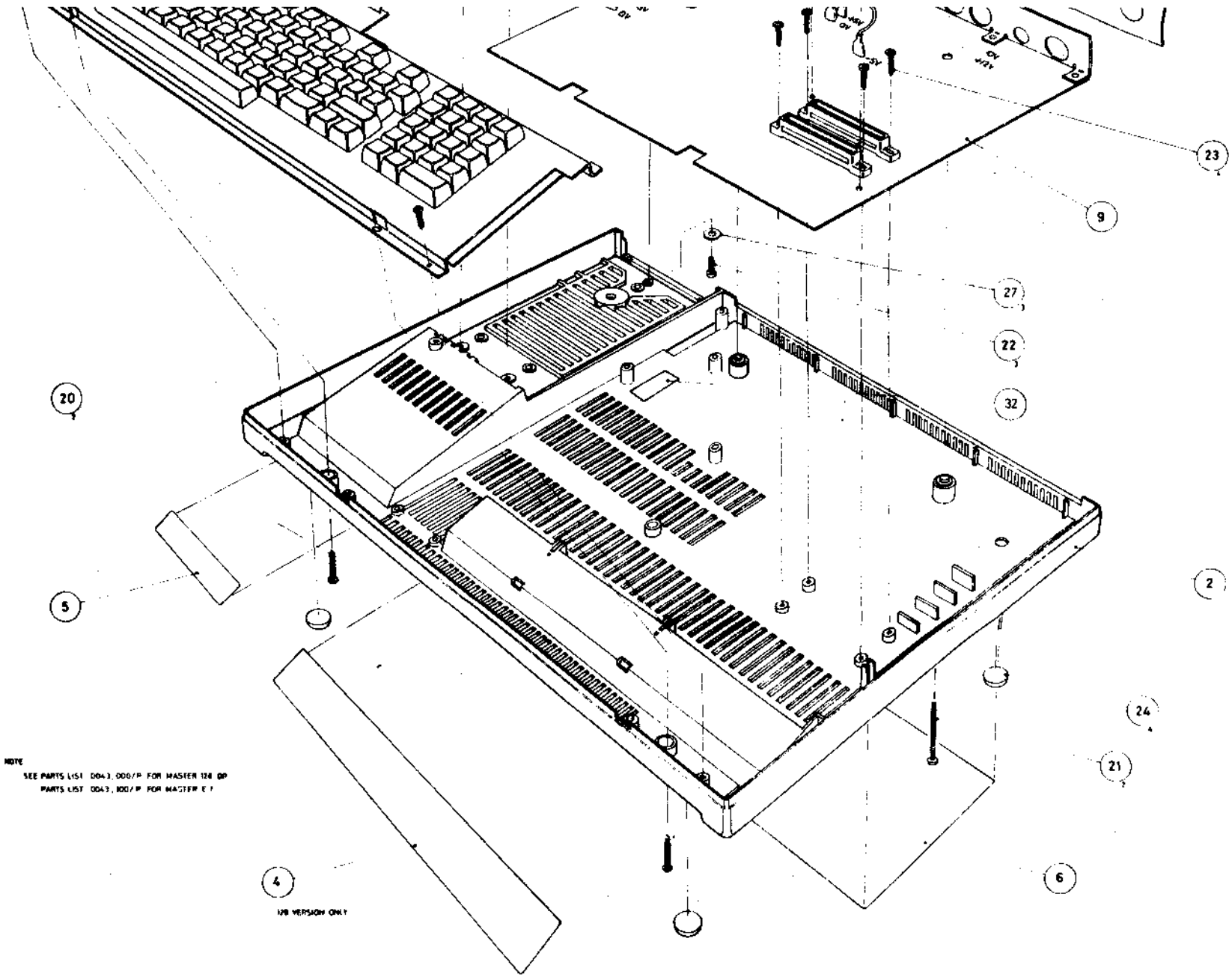
PCB circuit diagram
Sheet 2




PL8
PART OF PL24
SHIFT LOCK
CAP LOCK
POWER
CHRG
IC11
IC12
IC9
IC45
IC48
IC50
IC51
IC46
IC69
IC22
IC16
IC13
SERPROC
SERCLK
SIL 4 NF
SK10
RS423 CONN
CASSETTE
SK11
SIL 2 NF
SK6
FROM ECONET MODULE
SK7
ECONET
PL12
PL11
SK13
AUDIO OUTPUT
SK12
NOT FITTED
+12V
+5VA
+5VB
0V
0VA
0VB
0VC
-5V
1MHZE

Final assembly





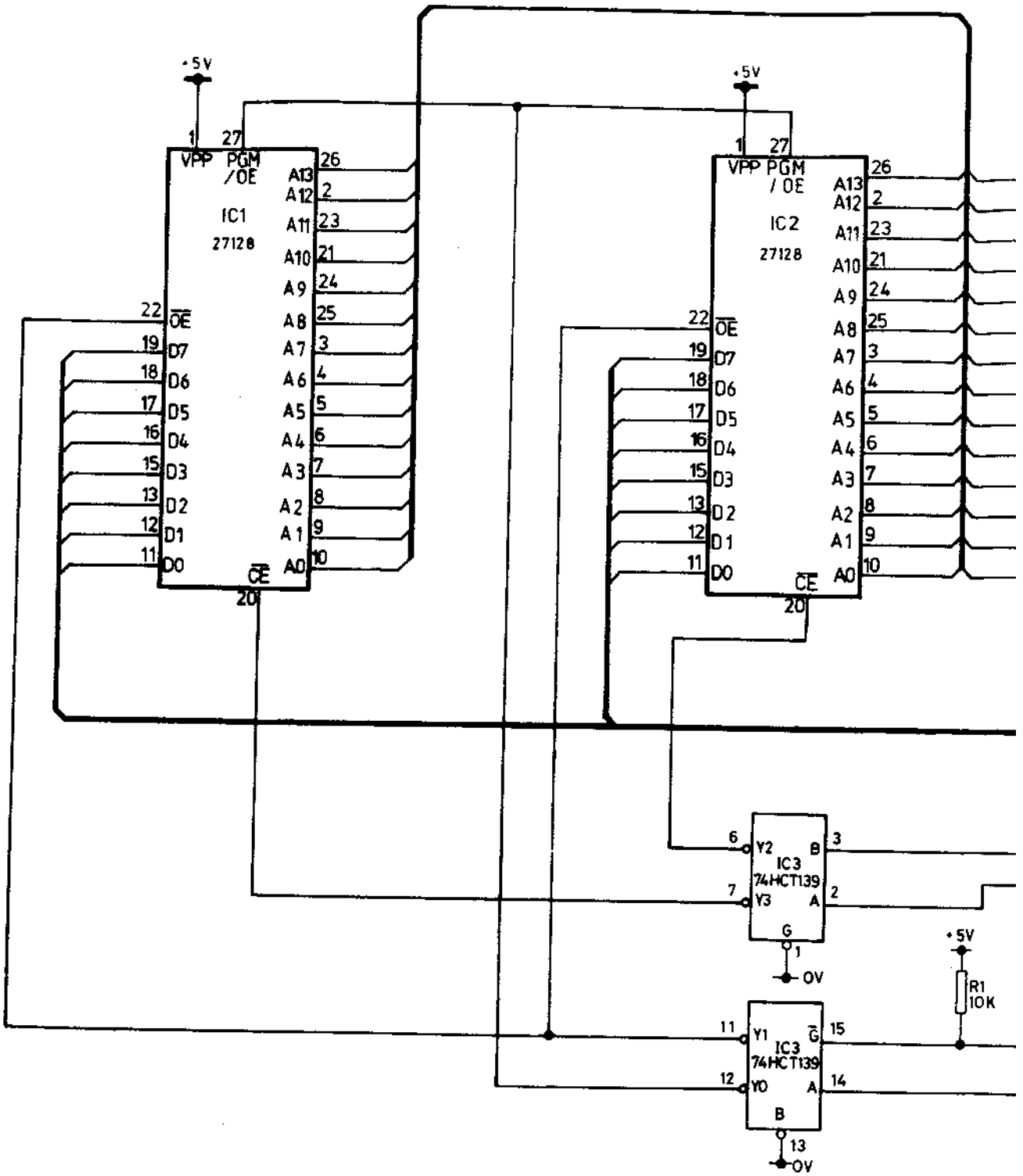
NOTE

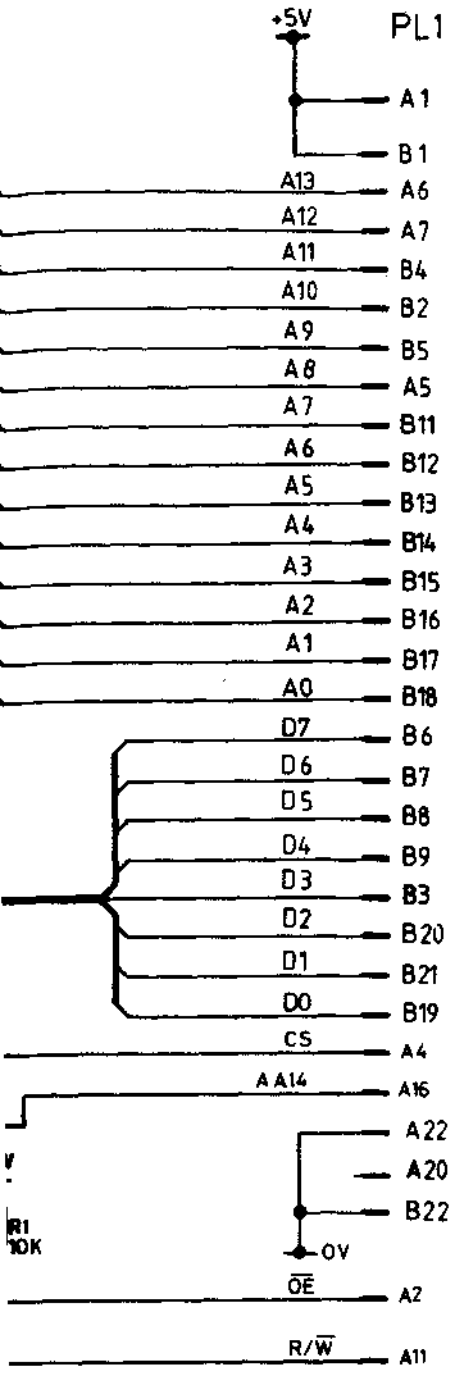
SEE PARTS LIST 0043,000/P FOR MASTER 128 OP

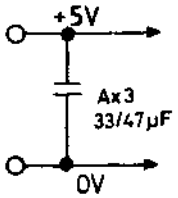
PARTS LIST 0043,100/P FOR MASTER E.T

128 VERSION ONLY

EPROM cartridge circuit diagram

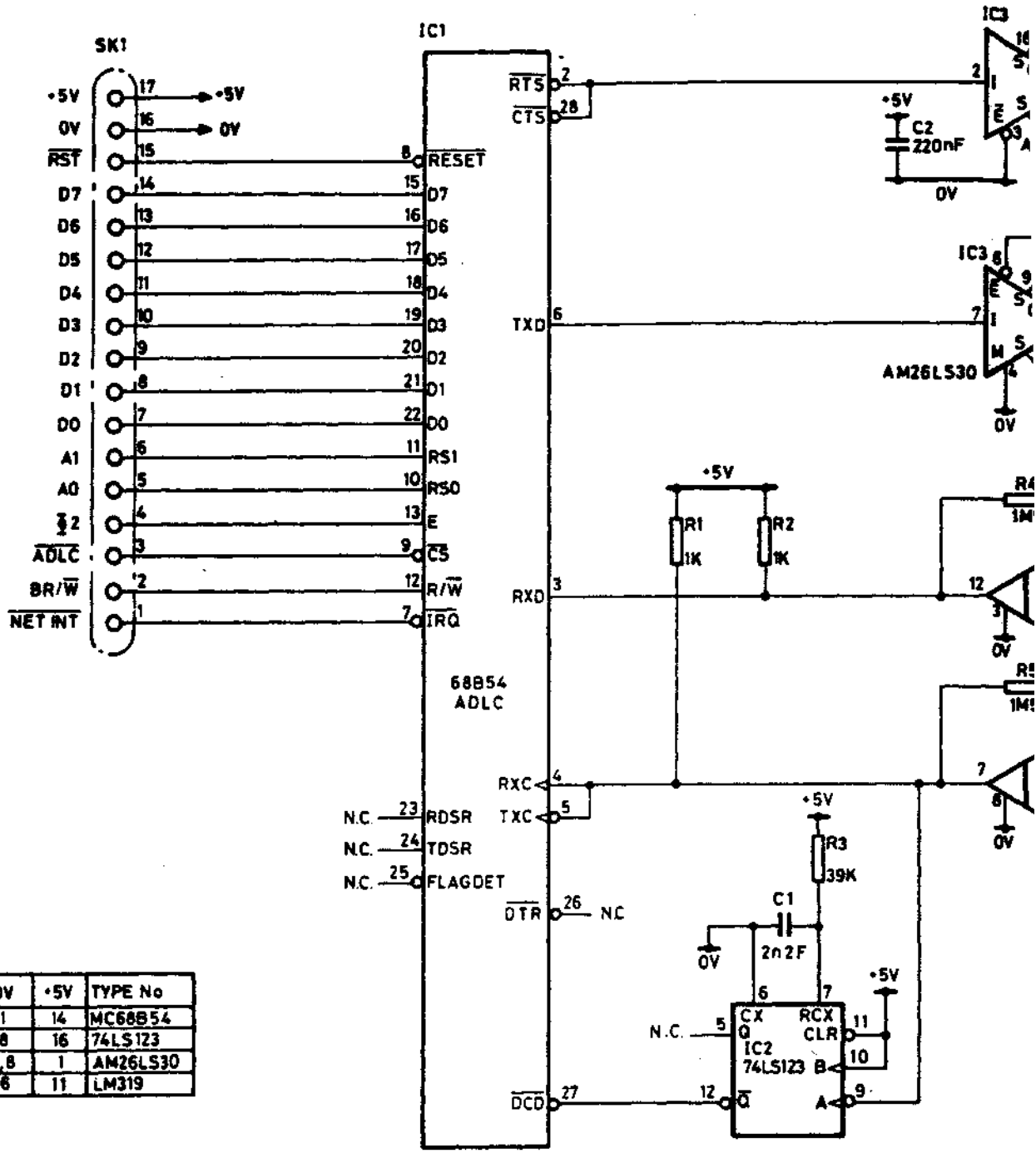




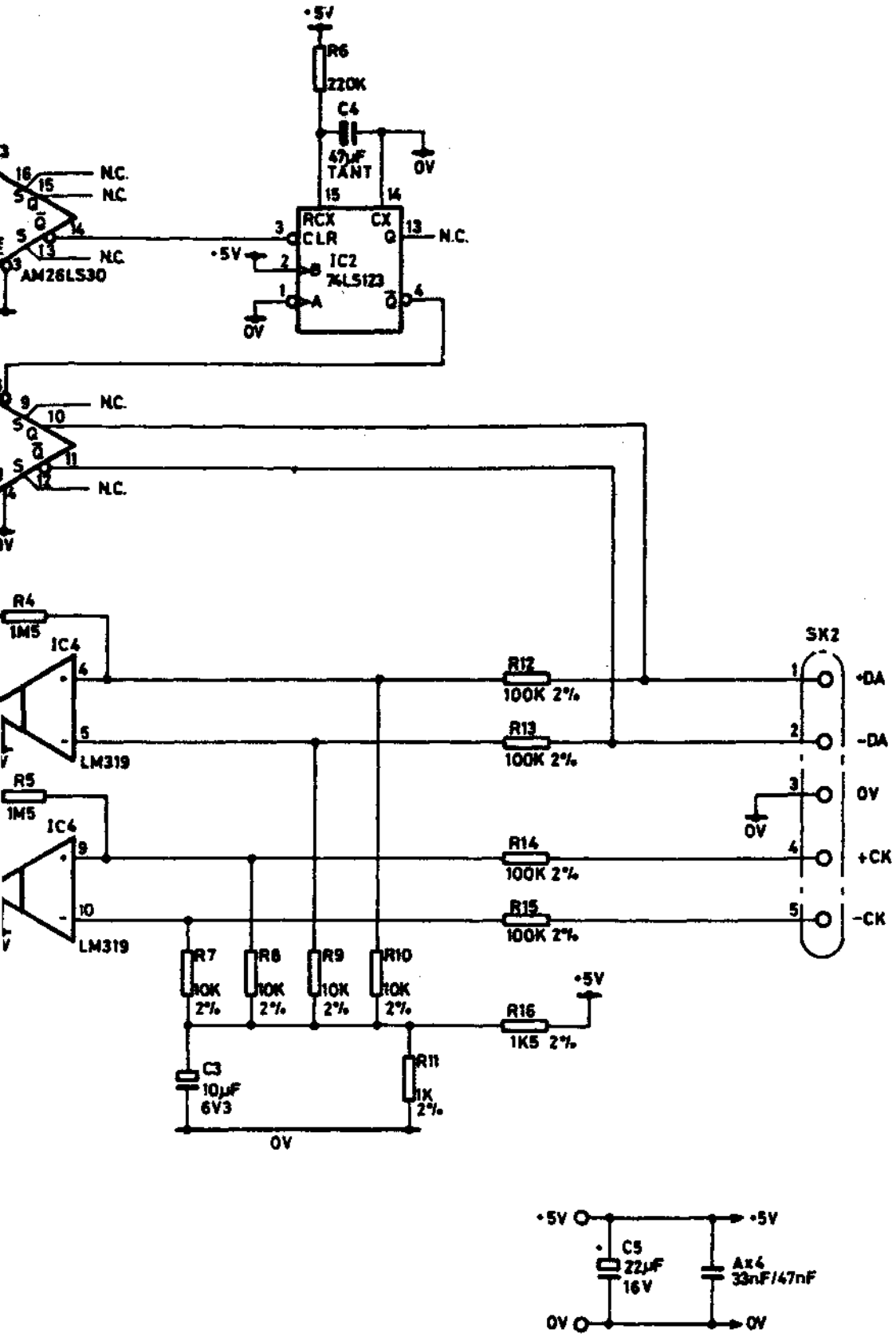


IC No	0V	+5V	TYPE No
1	14	28	27128
2	14	28	27128
3	8	16	74HCT139

Econet module circuit diagram

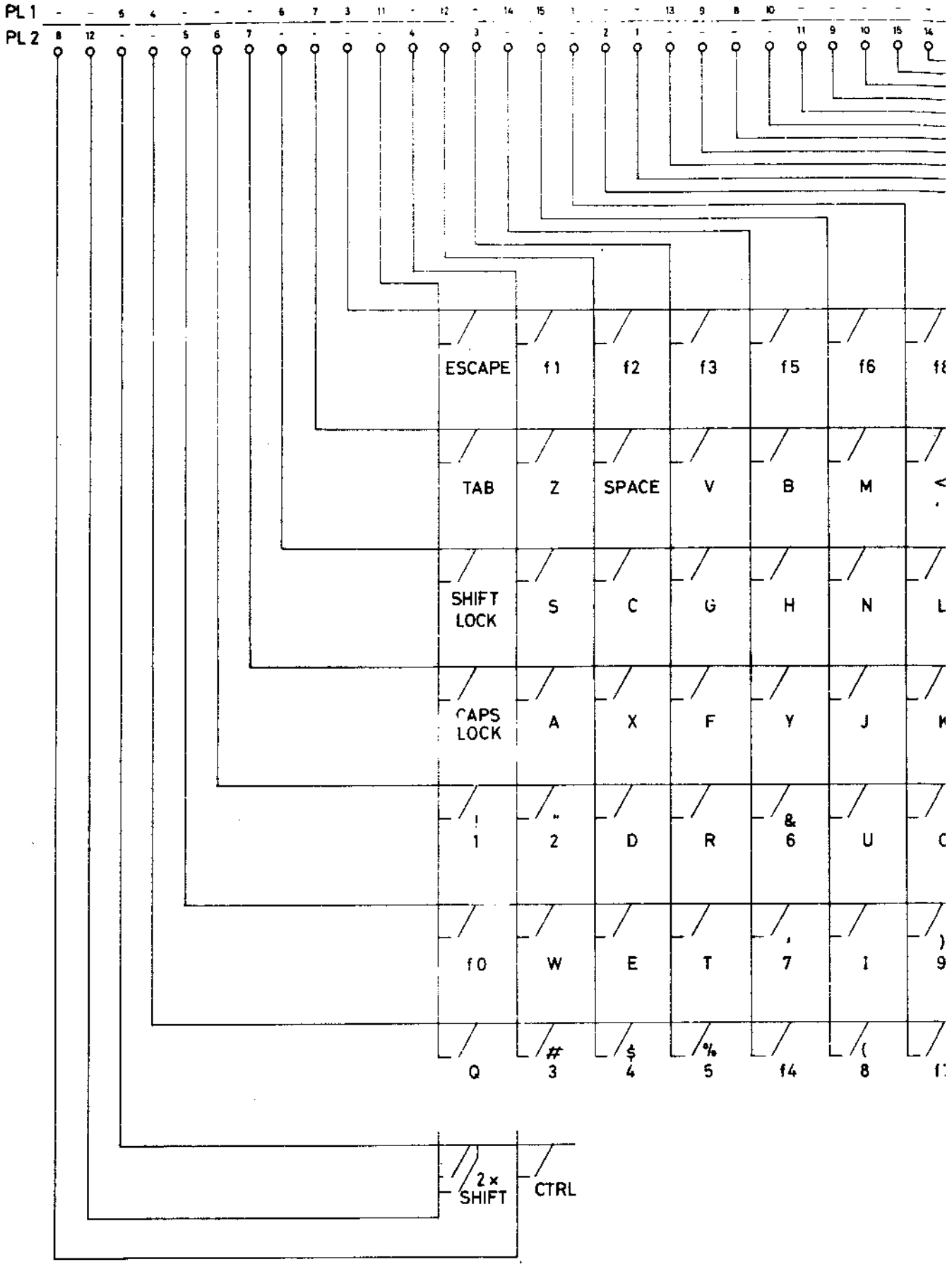


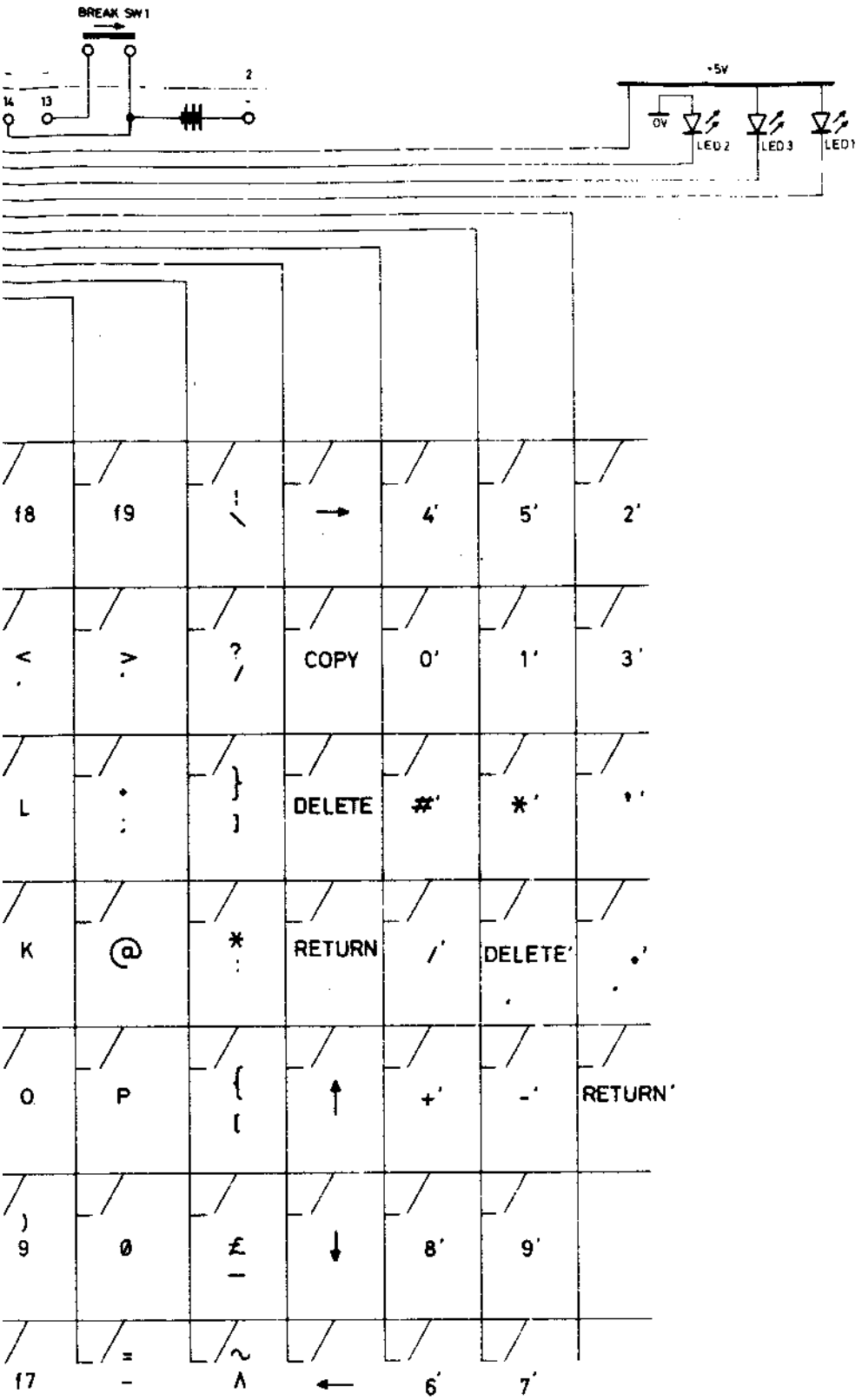
IC No	0V	+5V	TYPE No
IC1	1	14	MC68B54
IC2	8	16	74LS123
IC3	5,8	1	AM26LS30
IC4	6	11	LM319


+5V
R6
220K
C4
47µF
TANT
0V
N.C.
N.C.
N.C.
AM26LS30
RCX
CLR
CX
Q
IC2
74LS123
A
N.C.
N.C.
N.C.
R4
1M5
IC4
LM319
R12
100K 2%
R13
100K 2%
SK2
+DA
-DA
0V
+CK
-CK
R5
1M5
IC4
LM319
R14
100K 2%
R15
100K 2%
R7
10K
2%
R8
10K
2%
R9
10K
2%
R10
10K
2%
+5V
R16
1K5 2%
C3
10µF
6V3
R11
1K
2%
0V

+5V
+5V
C5
22µF
16V
4x
33nF/47nF
0V
0V

Keyboard circuit diagram





1 POWER ON
2 CAPS LOCK
3 SHIFT LOCK

NOTE - ALL PRIMED KEYS ARE ON NUMERIC KEY-PAD